50nm T-gate lattice-matched InP HEMTs with f_T of 430GHz using a non-annealed ohmic contact process

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Abstract — **A 50nm T-gate lattice-matched InP HEMT technology is presented with which devices with figures of 1600mS/mm for DC transconductance and 430GHz for cutoff frequency f_T have been realised. This performance can be attributed to the use of a non-annealed/non-alloyed ohmic contact process which acts to reduce parasitic access resistances to the device. To the best of our knowledge, these performance figures are the highest reported to date for a HEMT device fabricated from a lattice-matched InP material system.**

I. INTRODUCTION

With the reduction of device dimensions with modern III-V HEMT technology in an attempt to increase device performance, the role of the parasitic elements external to the intrinsic device becomes accentuated for such ultra-short gate length systems [1]. Beyond improving the intrinsic device operation through increased carrier velocities beneath the gate with different channel materials, or reducing carrier transit times beneath the gate with shorter gate lengths, the external device elements must then be considered for optimum operation. Such parasitic elements include access resistances to the intrinsic device as well as fringing capacitances between the gate and source/drain regions. One recognised method of reducing such access resistances is through a self-aligned gate process, with which the source and drain contact separation is reduced from that using a standard process flow [2]. This however has the side effect of increasing gate fringing capacitances, as the separation between the ohmic contacts and gate is reduced. As the magnitude of fringing capacitances can be comparable with that for the intrinsic gate capacitance for shorter gate lengths, the adoption of a self-aligned gate process can begin to degrade device performance at these gate lengths. Although originally developed for use with a self-aligned process [3], the non-annealed/non-alloyed ohmic technology presented in this work reduces the magnitude of parasitic access resistances compared with a standard annealed/alloyed process. Adoption of this process at the 50nm node then allows for a reduction in the access parasitic resistances with a standard (non-self-aligned) device geometry and with minimal gate fringing capacitance.

II. METHOD

In a typical III-V HEMT process flow, the formation of the source and drain ohmic contacts relies on the annealing/alloying of the ohmic metals following their deposition, to encourage their diffusion into the semiconductor heterostructure. This acts to reduce the magnitude of the potential barriers through the structure and promote better vertical conduction between the ohmic metal and device channel. Using a self-aligned gate process, it is necessary to minimise the temperature at which the contacts are annealed to reduce degradation of the gate contact, which is formed prior to the ohmic contacts [4]. Using a non-annealed ohmic process provides a route to the realisation of self-aligned gate devices without concern for degradation of the gate contact due to high temperature processing.

The non-annealed ohmic technology presented in this work relies on the tailoring of the band structure vertically through the material structure with selectively located delta-doping. The magnitude of the potential barriers that arise through the structure are then reduced, minimising the resistance between ohmic metal and channel without the need for diffusion of the ohmic metals into the heterostructure. Fig. 1 shows the material layer structure used for this work.

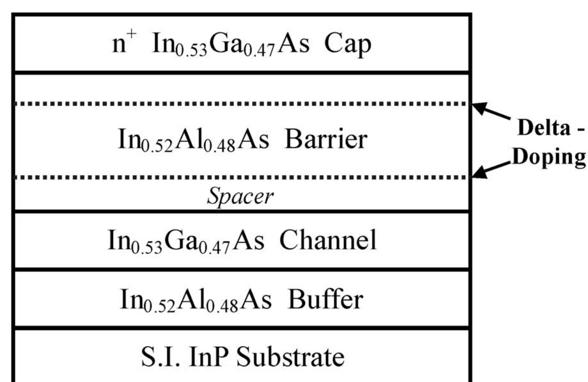

Fig. 1. Lattice-matched InP material with double delta-doping.

The second plane of delta doping situated close to the cap/barrier interface, reduces the magnitude of the conduction band discontinuity formed by the barrier layer. The effective resistance as seen by an electron moving from cap to channel layer or vice versa is then reduced compared to the standard single doped structure. The effective resistance across the Schottky contact between the ohmic metal and cap layer is also minimised by using a heavily doped cap.

Using the structure shown in Fig. 1 as scaled for 50nm device operation, a vertical contact resistance of 0.1Ω.mm was extracted by recessed transmission line matrix (TLM) measurements, which is comparable with standard annealed contact figures. The benefits of the non-annealed process are seen however, when the processes of conduction through the access regions are considered for both cases. This process is shown in Fig. 2:

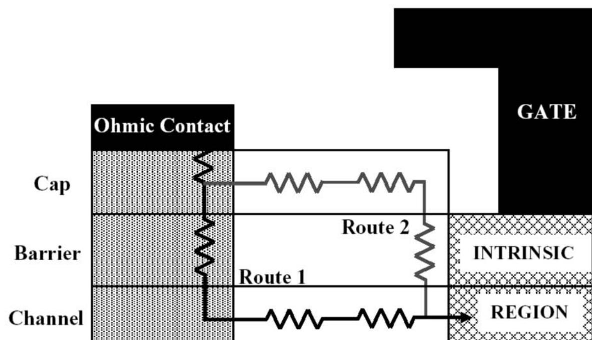

Fig. 2. Current paths through source region with annealed ohmic process (Route 1) and non-annealed process (Route 2).

Using a standard annealed ohmic process, the vertical conduction through the area beneath the ohmic contact is increased due to diffusion of the ohmic metals. Current flowing into the device will flow vertically through this ohmic region and then horizontally through the device channel into the intrinsic device region. Although current can flow horizontally through the cap layer, the vertical resistance across the barrier layer outside the ohmic contact region is typically too large to promote significant conduction across it with a standard InP structure. Therefore the majority of current will flow through Route 1 as depicted in Fig. 2. By introducing the additional delta doping with the non-annealed process, the resistance across the barrier layer is minimised outwith the ohmic contact region. Conduction between the ohmic metal and intrinsic device can then occur through the cap layer and across the distributed resistance of the barrier layer into the channel as denoted by Route 2 in Fig. 2. Parallel conduction then acts to reduce the horizontal resistance through the material between the ohmic region and intrinsic device, significantly lowering the total access resistance.

III. Device Fabrication

Fabrication of the 50nm gate length devices was performed as follows: Each level of the process was defined using a Leica EBPG5-HR 100 electron beam lithography tool operating at 50keV, with the exception of the gate level which was patterned at 100keV. Initially the device and test pattern geometry was defined by non-selective wet mesa etching using an orthophosphoric acid based solution and the etch depth verified through AFM profiling. In reverse from a standard HEMT fabrication flow, the gate level was performed next, prior to the ohmic level. The 50nm T-gate profile was patterned into a PMMA/LOR/UVIII resist stack. A combination of succinic acid and orthophosphoric etch steps were used to produce a double recess etch profile before metallisation of the Ti:Pt:Au gate onto the InAlAs barrier layer. A scanning electron microscope (SEM) cross section image of a 50nm gate and recess is shown in Fig. 3. Following the gate level, deposition of the Au:Ge:Ni ohmic metallisation formed the source and drain ohmic contacts at a separation of 1.6μm with the gate pre-aligned between them. By defining the gate before the ohmic contacts, variations in the gate geometry often observed at such short gate lengths, and which result from fluctuations in the resist thickness as spun between the ohmic contacts, are avoided [5]. The definition and metallisation of large probe contact pads completed the process flow and allowed the on-wafer characterisation of the completed devices.

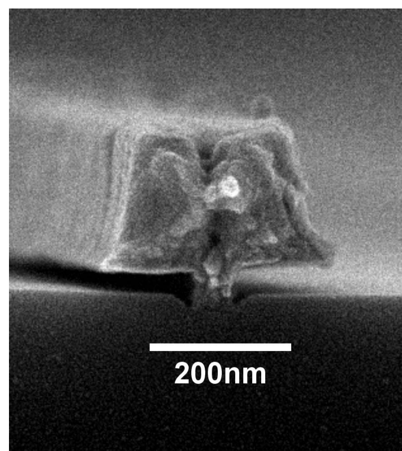

Fig. 3. SEM image of 50nm T-gate with double recess from completed devices.

IV. Device Reults

Characterisation of the 50nm devices at DC was performed using an Agilent 4155 semiconductor parameter analyser and Picoprobe high frequency probes. Typical output characteristics from a 50nm device are shown in Fig. 4.

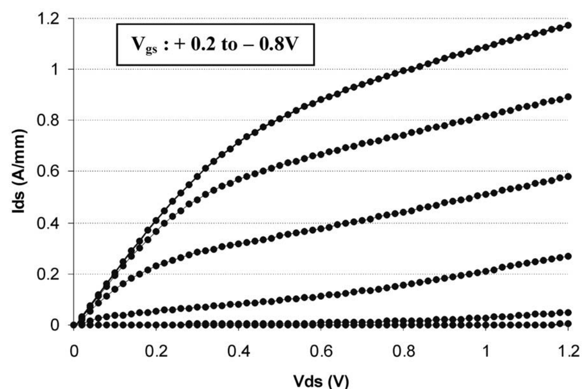

Fig. 4. Normalised output (I_d/V_{ds}) characteristics from a 2x25μm wide device with source-drain voltage swept from 0 to 1.2V and gate bias stepped from +0.2 to -0.8V.

The uniformity of device performance and yield was excellent as a result of using the non-annealed ohmic process and performing the gate level prior to the ohmic level. A device yield of 90% was achieved and across these operational devices a uniform threshold voltage of -0.63 ± 0.04V V_{gs} was measured. Operational devices also uniformly demonstrated a saturation current I_{dss} in the range 800 mA/mm.

The device transfer characteristics also demonstrated excellent performance including a peak extrinsic transconductance figure g_m of 1.6 S/mm. Device transfer and g_m characteristics are shown in Fig. 5.

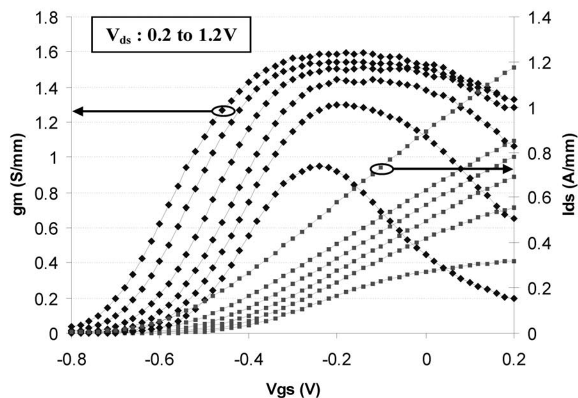

Fig. 5. Transfer (I_d/V_{gs}) and transconductance (g_m/V_{gs}) device response with V_{gs} swept from +0.2 to –0.8V and V_{ds} stepped from 0.2 to 1.2V.

High device linearity is observed in Fig. 5. as demonstrated by the wide transconductance peak at higher source-drain bias and across a wide gate voltage range. This linearity can be attributed to a combination of the double-delta doping within the material and the double gate recess etch.

Multi-bias S-parameter measurements of the devices from 40MHz to 60GHz were taken using an Anritsu 360B vector network analyzer to characterise devices at RF and extract figures for the cut-off frequency f_T and the maximum frequency f_{max}.

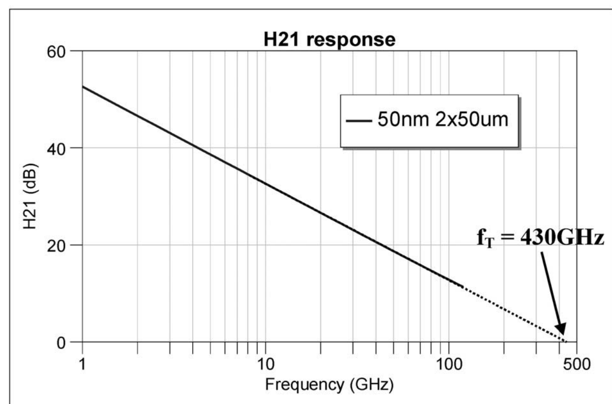

Fig. 6. H21 response from a 50nm gate length 2x50µm wide device as generated by de-embedded device circuit. An f_T figure of 430GHz is extracted.

Generation of an equivalent device circuit and subsequent removal of the probe pad parasitic elements allowed the generation of device de-embedded H21 and MAG responses. These are shown in Fig. 6. and Fig. 7. respectively.

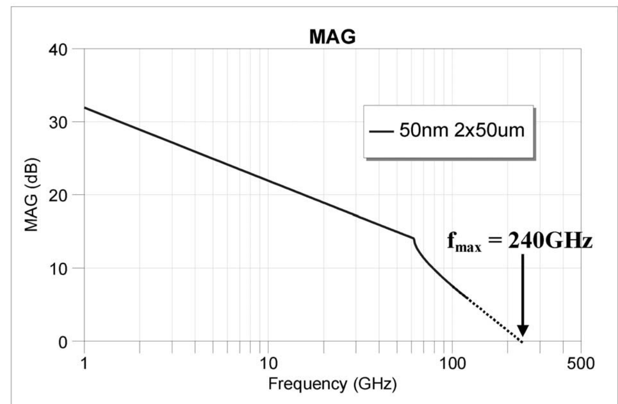

Fig. 7. MAG response from a 50nm gate length 2x50µm wide device as generated by de-embedded device circuit. An f_{max} figure of 240GHz is extracted.

An f_T figure of 430GHz is extracted from the H21 response assuming a decay rate of 20dB/decade as shown in Fig. 6. Similarly for the 2x50µm wide device, the MAG response produces an f_{max} figure of 240GHz. It should be noted however that due to the scaling of the gate resistance with device width, the figure for f_{max} will be device width dependent and decrease with increased width. This process is observed with f_{max} figures of up to 340GHz for 2x12.5µm devices.

V. CONCLUSION

A non-annealed/non-alloyed ohmic contact technology has been developed and adopted for the fabrication of 50nm gate length $In_{0.53}Ga_{0.47}As/In_{0.52}Al_{0.48}As$ HEMT devices. With the incorporation of the non-annealed ohmic process, the parasitic access resistances to the intrinsic device are reduced compared to an equivalent conventional annealed ohmic process. This provides an increase in device performance without the use of a self-aligned gate architecture with inherently large parasitic fringing capacitances.

Measurement and characterisation of the 50nm devices indicated performance figures of 1600mS/mm for the extrinsic transconductance and 430GHz for the cut-off frequency. These figures are believed to be the highest reported for a lattice-matched InP HEMT.

In addition to the performance benefits associated with the non-annealed ohmic process, the ability to define the gate before the ohmic contacts in the fabrication process flow improves the uniformity of the gate lithography, particularly for smaller gate features. This stems from the ability to define the gate onto a planar surface instead of between the source and drain ohmic metallisation with which resist thickness fluctuations can negatively impact on the gate lithography.

Following the success of adopting the non-annealed ohmic technology into a 50nm lattice-matched InP fabrication process, the potential of this technology will be examined further, with a higher indium content pseudomorphic system combined with a sub50nm T-gate process considered.

ACKNOWLEDGEMENT

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