An Array-Based Design Methodology for the Realisation of 94GHz MMMIC Amplifiers

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Abstract — **In this paper we report an array-based design methodology for the realisation of monolithic millimetre-wave integrated circuits (MMMICs). This work focuses on the realisation of a 94GHz MMMIC amplifier using an array-based approach by integrating high performance 50nm T-gate InP-HEMTs with an f_T of 480GHz and a Si_3N_4 Metal Insulator Metal (MIM) capacitor technology formed using room temperature inductively coupled plasma chemical vapour deposition (ICP-CVD) nitride deposition together with a range of more conventional coplanar waveguide-based passive components. A single stage amplifier, predicted to have a gain of 8 dB and return loss of better than –10dB at 94 GHz, demonstrated experimentally a gain of 8dB and a return loss of better than -6dB across a bandwidth of 7GHz from 89GHz to 96GHz at the designed bias point . The use of a room temperature nitride deposition process allows all passive components to be realised *after* active device realisation, and enables a mm-wave "sea-of-gates" array-based design methodology.**

I. INTRODUCTION

Although relatively low volume at present, a significant and growing high added value market exists for mm-wave imaging and sensing applications, the key component of which is the front-end low-noise amplifier in the receiver.

System sensitivity is ultimately determined by the performance of the front end amplifier which should possess outstanding high frequency characteristics. The acknowledged device of choice for front end amplifier realisation is a short gate length, InP-based HEMT[1] such as the technology described in this paper.

While performance is a key metric for successful adoption of a technology, time-to-market is becoming an equally important contributor to market growth. To improve product time-to-market, a range of strategies, in particular array-base design are being adopted. Array-based design, which has been hugely successful in the digital field, has not been embraced by the microwave and mm-wave community to date due to perceptions of design, performance and process flow limitations arising from this approach.

The amplifiers reported in this worked are realised using an array-based methodology in which a relatively sparse matrix of high performance 50nm gate length InP HEMTs is first defined on a grid optimised to enable the realisation of a range of mm-wave components. Following the identification of known good active devices by in-line DC and RF testing, the MMMIC's, in this case amplifiers, are completed by passive device realisation. This design concept and process flow is enabled by the low temperature nitride deposition technique described in the paper.

The successful realisation of MMMIC's using the approach described in this work paves the way for further investigation, optimisation and ultimate incorporation of array-based design methodologies in the mm-wave arena.

II. DISCUSSIONS AND RESULTS

Key Components in mm-wave Array Based Design

A. ICP-CVD MIM Capacitors

A thin layer of Si_3N_4 is an essential element in realising MMMICs. Passive components requiring Si_3N_4 such as MIM capacitors are widely used for filtering, dc blocking, matching circuits, and biasing circuits in MMMIC technologies [2]. Si_3N_4 is also used for passivation and planarisation, and reducing the effective length of transmission lines [3- 4]. Therefore Si_3N_4 thin film deposition conditions, reliability and reproducibility are important issues for MMMICs viability.

Currently, Si_3N_4 used in MMMIC realisation is based on PECVD deposited at 300°C. This process has proven to be reliable but has the disadvantage of a high temperature deposition environment. The high temperatures may result in active layer damage or ohmic contact and Schottky contact degradation, and therefore Si_3N_4 layer deposition must be performed early in the overall process flow, reducing the flexibility of the fabrication process cycle.

Low temperature deposition gives an extra freedom to use MIM capacitors on substrates sensitive to high temperature or the flexibility to realise passive elements fabricated after active devices have been completed, leading to "sea-of-gates" possibilities for mm-wave applications. During Si_3N_4 MIM capacitors level realisation the active devices are covered by resist to avoid deposition and then the etching damage to the transport properties of the active layer.

The performance of the Si_3N_4 capacitor deposited at 22°C using ICP-CVD techniques is found to be similar to that based on capacitors with a PECVD Si_3N_4 Insulator deposited at 300°C as shown in Figure 1. From figure 1 we observe that a breakdown electric field of greater than $3x10^6$ Vcm^{-1} was achieved using the room temperature

deposited Si_3N_4. Further reduction in the thin film of Si_3N_4 for a 200μm^2 area capacitor deposited at 22°C using ICP-CVD to only 5nm resulted in a leakage current of less than 50nA at 2V. This indicates both high quality films with low pin-hole density, and good conformal coating as the nitride film has successfully covered a step of 150nm, the thickness of the lower capacitor plate, without significant additional leakage.
Capacitance values were extracted from RF measurements up to 60GHz as shown in Figure 2 which shows the extracted capacitance and the equivalent circuit model used for series capacitors of 5nm and 120nm thick Si_3N_4 deposited at 22°C using ICP-CVD. The capacitance of the 5nm thick Si_3N_4 showed an increase of more than thirteen fold in value, it also showed less inductance and RF loss. From the data in Figure 2, a relative permittivity of 7.5 was extracted for the low temperature deposited nitride films.

B. 50 nm T_gate InP HEMTs

High performance, high yield (85%) 50μm gate width 50nm T-gate InP HEMTs with an f_T of 480GHz and f_{max} of 420GHz, gm of 1150ms/mm and Idss of 600mA/mm were fabricated using an e-beam lithography UVIII/LOR/PMMA resist stack [5] and a selective wet gate recess etch. Figure 3 shows a SEM image of a 50nm T-gate profile of the device after metallisation and lift-off. Figure 4 shows the output characteristics and the transfer characteristics of the device. This device exhibits an intrinsic gain of 14.0dB at 94GHz and a f_T of 480GHz, the highest reported for a 50nm gate length as shown in Figure 5

C. 94 GHz Amplifier Response

Figure 6 shows a schematic diagram of the designed single stage amplifier. A reactively matched amplifier designed is used to enhance the noise performance. λ/4 open single stubs are used to centre the operation of the amplifier at 94GHZ. 50Ω/□ NiCr resistors and room temperature deposited ICP Si_3N_4_MIM capacitors are used at the biasing circuits for stability. The amplifier was designed to operate at Vds of 1.0V and Vgs of -0.2V. Figure 7 shows the performance of the modelled and measured one-stage w-band amplifier. The unconditionally stable single stage designed amplifier exhibits a gain of ~8dB and a return loss of better than -6dB across a bandwidth of 7GHz from 89GHz to 96GHz. The biased operating point of the amplifier is Vd of 1.0V and Vg of -0.2Vpoint, with an output current of 39mA. The measured performance is very well in agreement with the model.

III. Conclusions

In line characterisation of a sparse matrix of 50 nm T-gate InP HEMTs designed to enable an array-based approach to MMMIC design have demonstrated excellent performance merits including f_T of 480GHz and f_{max} of 420GHz, gm of 1150ms/mm and Idss of 600mA/mm. These devices are used for MMMIC realisation by integration with Metal Insulator Metal (MIM) capacitors formed from Si_3N_4 deposited by ICP-CVD at room temperature. In comparison with existing 300°C PECVD Si_3N_4 processes, the new approach offers reduced thermal budget and therefore the flexibility to realise all passive elements ***after*** active devices have been completed, leading to "sea-of-gates" array-based design methodologies for mm-wave applications,

Using this approach, a 94GHz MMMIC one-stage amplifier with a gain of ~8dB and a return loss of better than –6dB across a bandwidth of 7GHz has been designed and fabricated. The model and the measured performance are in agreement.

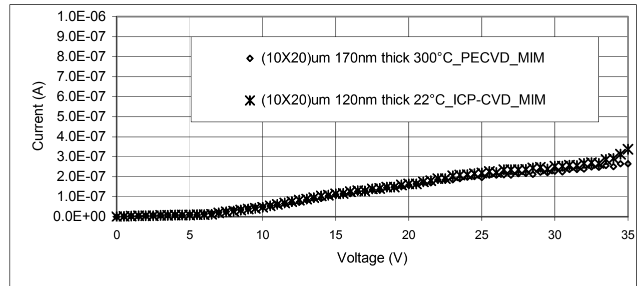


Fig. 1. Leakage current of a 200μm^2 120nm thick Si_3N_4 capacitor deposited at 22°C using ICP-CVD compared to that of a 170nm PECVD deposited at 300°C

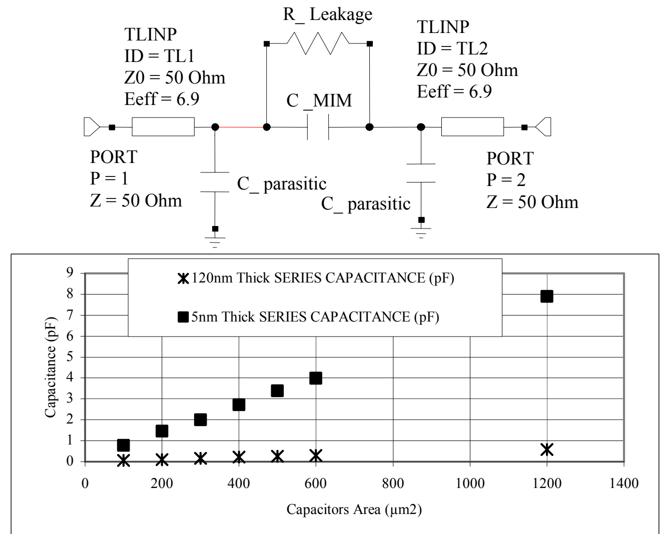
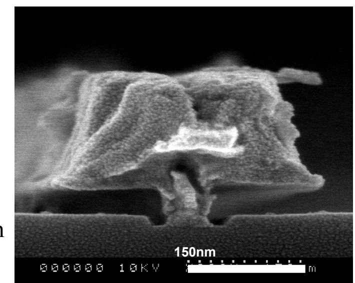


Fig. 2. Capacitance values as a function of capacitors area extracted from RF measurements of a 5nm and 120nm thick Si_3N_4 deposited at 22°C using ICP-CVD, equivalent circuit model is also shown

Fig. 3. 50nm T-gate profile after metallisation and lift-off



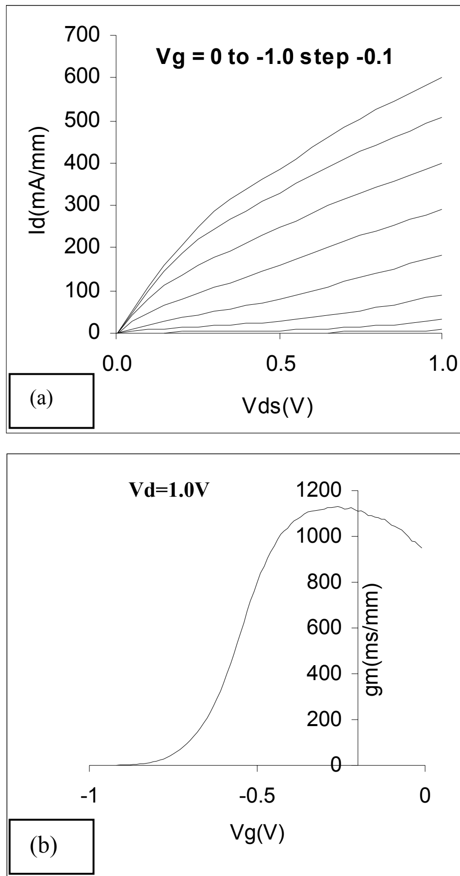


Fig. 4 DC performance of a 2 finger 50µm gate width with a 50nm gate length T-gate InP-HEMT (a) Output characteristics of the active device (b) transfer characteristics of the active device biased at Vd=1.0V

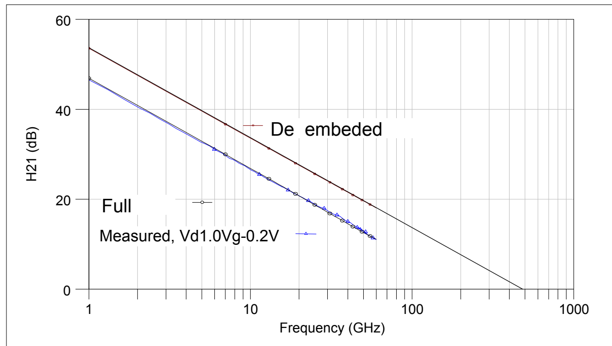


Fig. 5. RF performance of a 2-finger 50µm gate width with a 50nm gate length T-gate InP-HEMT. Measured RF, full model and de-embeded model, the device showed a superior f_T of 480GHz

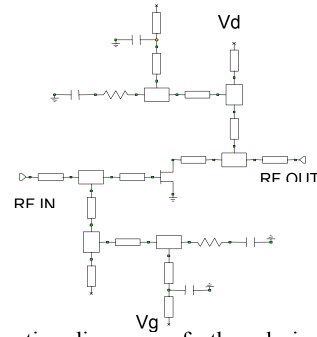


Fig. 6. Schematic diagram of the designed single stage amplifier

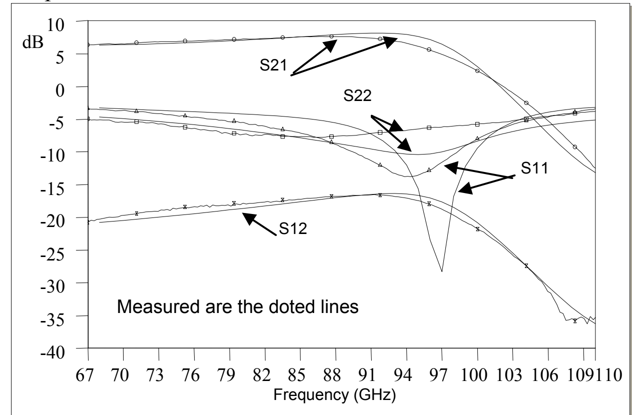


Fig. 7 Model and measured response of a 94GHz one-stage amplifier based on the equivalent circuit model of the 2-finger 50µm gate width with a 50nm gate length T-gate InP-HEMT. The designed and measured response of the one-stage amplifier exhibits a gain of 8dB and a return loss of better than –6dB across a bandwidth of 7GHz from 89GHz to 96GHz and are well in agreement. The biased operating point of the amplifier is Vd of 1.0V and Vg of -0.2Vpoint, with an output current of 39mA

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