Improved Performance of Flip Chip assembled MMIC Amplifiers on LTCC using a Photonic Bandgap Structure

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Abstract — **Further cost reduction in today's microwave frontends is strongly related to assembly technology as well as module technology. Depending on the particular mix of technologies, specific problems and chances can be addressed. In case of flip-chip on LTCC, various effects of performance degradation of the MMICs can be observed, some of which can be related to unwanted internal coupling of the microstrip IC due to the floating groundplane. For some MMICs a periodic structure below the chip can help to improve the characteristics of the assembled chip due to its ability to suppress a particular class of unwanted modes between the chip groundplane and the module ground. The periodic structure is proposed and measured results are given and discussed.**

I. Introduction

One of the main objectives of microwave packaging for MMICs is the conservation of the desirable RF properties. In case of amplifier MMICs the most critical properties with respect to packaging are forward gain, input match, reverse isolation, gain flatness and stability.

LTCC based approaches are an interesting choice for packaging MMICs. The ceramic carrier forms a bondable substrate for wire bonding as well as flip-chip and can be used to integrate high quality passives. Integrated blocking capacitors can reduce assembly cost and additional features such as RF filtering and protection against electrostatic discharge can be implemented at low extra cost [4].

For die attach, flip-chip has drawn attention due to the good electrical reproducibility and low parasitic inductance of the flip-chip transition. However, in practice it can be seen, that flip-chip also requires to handle particular parasitic effects that do not occur when mounting the chip upside up on a metal surface such as done in most wirebonding approaches [3][5].

When using flip-chip, the effect of detuning the chip performance due to the proximity of the ceramic substrate is to be mentioned. It can be explained as the impact of disturbation of the transmission lines on the MMIC. The high dielectric constant of the ceramic material just below the chip shifts the line impedance on chip towards lower values. At the same time, wavenumbers increase. The lines that connect the individual stages within the chip and those used in the matching circuitry however are vital for the chip performance, which therefore may be impaired in flip-chip assemblies by some degree.

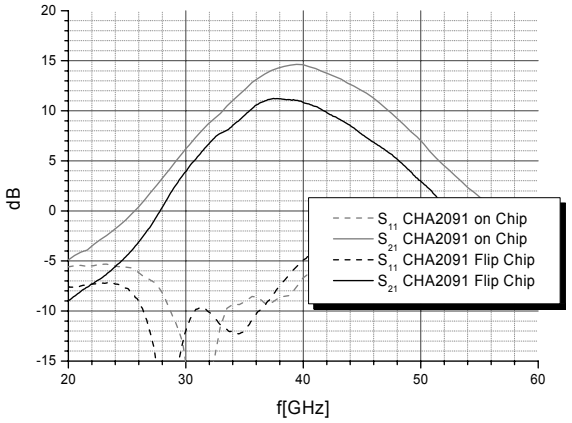

Fig. 1. UMS CHA2091: Performance Coplanar flip-chip without groundplane vs. on-Chip Performance

Another point in MMIC packaging is ground impedance. From practical experience it is known, that quality and reproducibility of ground contact is crucial for most microwave components. From linear circuit theory is known, that an ideal amplifier loses backward isolation by inserting an impedance in the ground connection. In practical designs this effect is sometimes used for achieving instability in transistors for oscillator design.

An example is given in [2]. In this presentation, the influence of ground inductance in a 40 GHz microwave package has been shown.

In case of flip-chip assembled devices, quite a similar effect can be observed. The floating of the MMIC groundplane introduces coupling paths within the amplifier network and leads to gain and phase ripple.

There are MMIC amplifiers where detuning of the MMIC transmission lines appears to be most influential on flip-chip performance. As an example, UMS's CHA 2091 can be given. Fig. 1 shows the measured on-Chip and flip-chip performance. In flip-chip assembly, the performance appears to be reduced over the whole frequency range of operation by a more or less constant 2-3dB in forward gain. The frequency response appears to remain qualitatively unimpaired. A behavior like this is observed when transmission line impedances in an amplifier model are shifted.

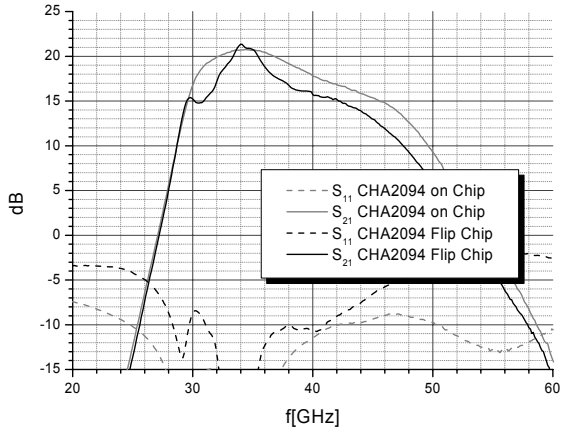

Fig. 2. UMS CHA2094: Performance of Coplanar flip-chip without groundplane vs. on-chip Performance

II. PERFORMANCE DEGRADATION THROUGH PARASITIC COUPLING

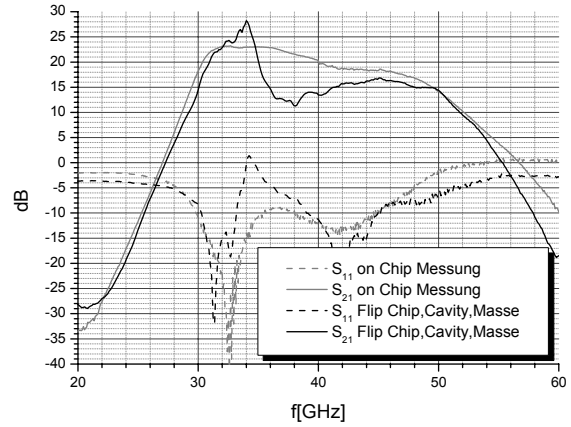

Fig. 3. UMS CHA2094: Performance flip-chip with groundplane, 260 micron substrate, cavity below chip

The second effect of internal parasitic coupling is likely to be the dominant reason for the specific flip-chip behavior seen in UMS's CHA 2094. Fig. 2 shows, that the qualitative behavior of the MMIC is changed after assembly and a change in electrical structure has to be taken into account for modeling this effect. The chip is a three stage amplifier with significantly more gain, which might be the reason for internal coupling now being the most influential factor in performance degradation.

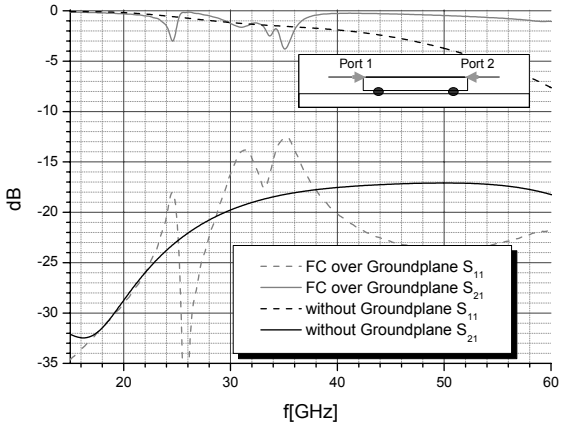

Fig. 4. MMIC Groundplane transmission between 50 Ohm ports. The active Chip circuitry has not been included in the simulation

An even severe impact on the performance is observed when a groundplane is introduced into the configuration, as might be necessary for shielding within an LTCC multichip module. In this particular case, the Chip not only suffers from gain degradation but also exhibits near

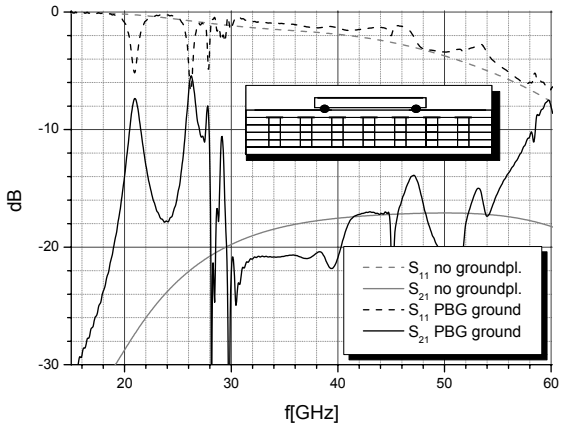

Fig. 5. MMIC Groundplane transmission. The Substrate ground has been replaced by a PBG structure

instable behavior, as can be seen in raised input reflection of more than 0dB at 34 GHz. This kind of behavior has previously been reported in [3] and has been attributed to parallel-plate modes in a resonance condition between the groundplanes of chip and module.

III. Backside Transmission Analysis

To get a quantitative understanding of the parasitic coupling mentioned above, the transmission properties of the potentially floating MMIC backside metallization has been compared using electromagnetic simulation. The simulation has been performed as indicated in the inlay in Fig. 4. The MMIC backside has been excited by two discrete ports at the positions of the RF input and output. Fig. 4 shows, that in between 30-40 GHz strong transmission occurs. This is due to modes of the parallel plate type between the MMIC groundplane and the groundplane in the substrate. With the substrate groundplane removed, the transmission is lower with a smoother frequency behavior.

By further simulations evidence for the general scheme of parasitic coupling given in Fig. 6 has been gained.

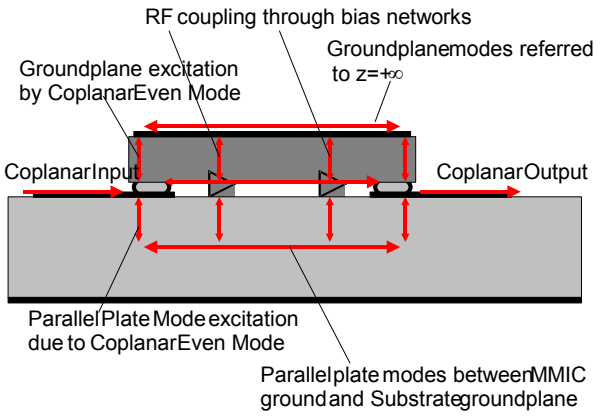

Fig. 6. Coupling Scheme for Microwave MMICs. Possible coupling paths and mechanisms are sketched as arrows.

It turns out, that among the possible coupling paths, the input and output transitions exhibit the tightest coupling to the MMIC backside metal on the configurations observed in this paper. With microstrip LTCC as chip-carrier for example, the center conductor of the coplanar chip input is connected to the microstrip line on the LTCC-module by means of a stud bump. Ground vias have to be used in order to connect the coplanar ground pads with the microstrip ground on the substrate side. These vias have to be staggered with respect to the corresponding stud bumps for technological reasons and contribute to significant ground inductance which is responsible for even mode excitation on the coplanar chip input. The even mode component however directly excites modes of the parallel plate type.

IV. The PBG Structure

In cases where the corelation between MMIC backside transmission and MMIC Performance degradation is shown, measures taken to reduce backside transmission should also bring a positive impact on flip-chip performance. In [3] parallel-plate modes have been suppressed using lossy silicon substrates below the chip. The LTCC equivalent could be the application of resistive films on top layer or within buried layers of the LTCC. However, this measure is not feasible in many LTCC processes. In this paper, a periodic structure implemented below the MMIC within submerged layers of the LTCC carrier is discussed.

The inlay in Fig. 5 shows the Structure, which can be compared to the so called Sievenpieper PBG, in more detail. It has been proposed and discussed in [1]. In LTCC it can conveniently be realized by stacks of vias on the bottom groundplane. The stacks are arranged in a regular quadratic lattice. These stacks present a so called high impedance surface to the Flip-Chip MMIC in the range of 30-40GHz. This high impedance property is the reason that parallel plate resonances in between the lower groundplane and a metal patch such as a MMIC groundplane cannot occur. Considering the MMIC groundplane as transmission line gives reduced coupling therefore as shown in Fig. [5]

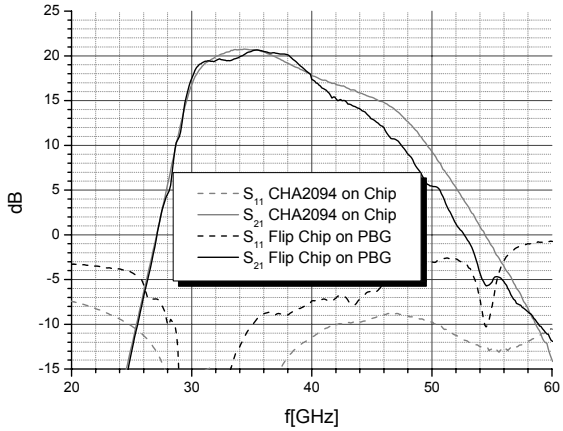

Fig. 7. MMIC over periodic high impedance surface.

In Fig. 7 the measured MMIC performance shows a significant improvement compared to Fig. 2 and Fig. 3.

V. Conclusion

flip-chip assembly of amplifier MMICs often suffer from performance degradation due to coupling over the floating groundplane. This coupling has the most severe impact when the chip carrier contains a second groundplane. In these configurations parallel plate mode resonances can occur in between the assembled chip and its carrier.

Using a Periodic Bandgap Structure (PBG) between those groundplanes, this coupling has been successfully reduced.

The periodic Structure has been integrated into the LTCC-Carrier and relies only on standard LTCC features, in this case via stacks and screen printed metal patterns. The application of lossy materials for mode suppression would be difficult in LTCC environments and has been avoided by this measure.

The resulting flip-chip performance is comparable to the on-chip performance for the investigated MMIC circuit and a broad variety of shielding requirements can be addressed.

Acknowledgement

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