Performances of AlGaN/GaN HEMTs in Planar Technology

M. Werquin, N. Vellas, Y. Guhel[1], D. Ducatteau, B. Boudart[1], J.C. Pesant, Z. Bougrioua[2], M. Germain[3], J.C. De Jaeger and C. Gaquière

IEMN-TIGER, av Poincaré, BP 69, 59652 Villeneuve d'Ascq, France
[1] EIC-LUSAC, cite universitaire, BP 78, 50130 Cherbourg Octeville, France
[2] CRHEA-CNRS, rue B. Gregory, Sophia Antipolis, 06560 Valbonne, France
[3] IMEC, Kapeldreef, 75, B-3001 Leuven, Belgium

Abstract — **The advantage of planar technology for the AlGaN/GaN HEMTs realization is demonstrated in this paper. A breakdown voltage closed to 100 V and an output power density of 4 W/mm at 4 GHz have been measured on a 2x25x1.5 µm² HEMT on sapphire substrate. These results are very promising because the devices have not been passivated, and no T gate has been achieved. Moreover, planar technology offers the advantage of a better reliability. At present time, it is the best power result obtained with an isolation by argon implantation.**

I. Introduction

The GaN has physical properties very interesting for power applications at microwave frequencies like a large band-gap, a high saturation velocity and a good thermal and chemical stability. However, to obtain powerful microwave devices, a good isolation between them is necessary in order to obtain a low leakage current. Today, the best power results are obtained on AlGaN/GaN HEMT structures on SiC substrate, but the fast progress of the other substrates are very promising: on SiC substrate P_{SAT} = 30 W/mm at 8 GHz [1], on Al_2O_3 substrate P_{SAT} = 12 W/mm at 4 GHz [2] and on silicon substrate P_{SAT} = 12 W/mm at 2 GHz [3].

The aim of this work is to demonstrate that the planar devices present good electrical characteristics and that, with an easier process. In a first time, the technological steps of planar GaN HEMTs realization will be presented. In a second time, the main DC and small signal parameters will be summarized. Then the first power results in constant wave (CW) mode at 4 GHz under probes will be shown.

II. Devices Description

The epitaxial layer has been carried out by LP-MOCVD (Low Pressure - Metal Organic Chemical Vapor Deposition) on sapphire substrate with NH_3, TMGa (Trimethylgallium) and TMAl (Trimethylaluminium) as precursors [4]. After the low temperature deposition of a thin nucleation layer, the sample is brought up to high temperature in order to recristallize. The growth of a 4.5µm nid GaN layer is then carried out under a pressure and a temperature of 100 Torr and 1200 °C respectively. The $Al_xGa_{1-x}N$ barrier layer is then deposited at low pressure with a 28 % aluminum rate and a thickness of 210 Å.

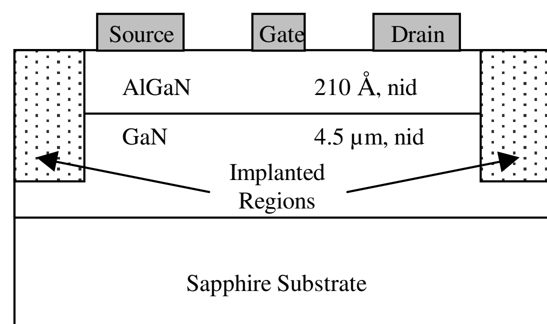


Fig. 1. Structure of an AlGaN/GaN planar HEMT. The isolation by implantation has been achieved with argon incorporation.

The transistors are carried out on the layer presented figure 1. First of all, a surface cleaning is achieved with a HCl solution (2/3 HCl, 1/3 H_2O) during 2.5 min. This step is followed by a treatment of argon plasma during 90 s with an energy of 150 eV, in the reactor, just before metal deposition. The ohmic contacts are achieved with the metal sequence Ti/Al/Ni/Au and the respective thickness are 150/2200/400/500 Å. An annealing at 900 °C during 40 s under nitrogen atmosphere is finally carried out.

Then, the isolation step has been achieved with the implantation of argon ions [5]. The aim of this technique is to obtain an insulating layer, between the components, by generating a very strong concentration of defects. In order to define the density of implanted ions, measurements of the resistance between two ohmic pads separated by 5 µm have been carried out. Figure 2 presents the evolution of the resistance value between the pads versus the implanted argon dose. The reference sample (not implanted) shows a resistance value of 600 Ω. In the implanted range $3x10^{12}$ up to $3x10^{14}$ atoms/cm², the resistance increases from $5x10^{7}$ to $1x10^{16}$ Ω, which is attributed to the increase of impurities and crystalline defects. For higher dose, a brutal decrease of the resistance is noted. This behavior could be explained with a hopping conduction between the defects. Then, in order to obtain an optimal isolation

the implanted argon dose has been fixed at $3x10^{14}$ atoms/cm².

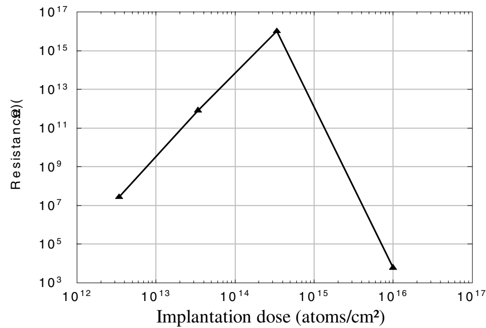


Fig. 2. Resistance evolution between two ohmic contact pads separated by 5 µm versus the implanted argon density.

A favor of the implantation method, in comparison with MESA isolation, resides in the improvement of the component reliability [6]. It has been shown that dry etching can create an enhancement of the surface conductivity providing leakage current [7], especially in high bias conditions. For the first time, to our knowledge, results on AlGaN/GaN HEMTs isolated by argon implantation are presented.

The rectangular gate contact has been achieved with the metal sequence Pt/Au (100/2000 Å). Before metal deposition, a surface cleaning is carried out under the same conditions as for the ohmic contact.

III. Static And Small Signal Results

Figure 3 presents the static $I_D(V_{DS})$ characteristics for a transistor with a 2x25x1.5 µm² geometry. The drain-source spacing is 3.5 µm and the gate is centered in this spacing.

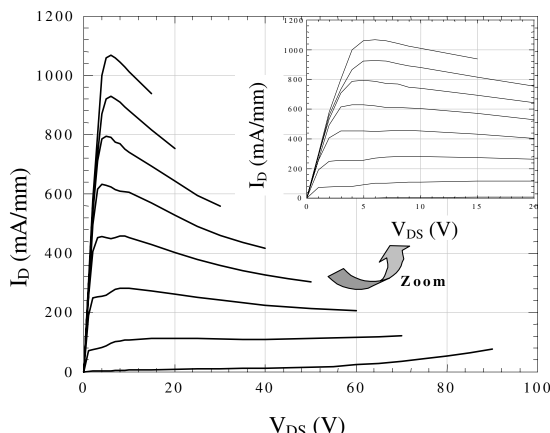


Fig. 3. Static $I_D(V_{DS})$ characteristics measured on a transistor geometry of 2x25x1.5 µm². A zoom is shown too (V_{GS} = -5 V to 2 V, 1 V step).

Breakdown voltage is closed to V_{DS} = 100 V in B class. A maximum drain current density of 1.05 A/mm is measured at V_{GS} = 2 V and V_{DS} = 5 V, this value is very promising if we consider the gate length (1.5µm). The negative drain conductance G_D can be attributed to thermal and/or trap effects. Indeed, the temperature increase due to the high dissipated power and to the poor thermal conductivity of the sapphire substrate could induce a decrease of the carrier mobility, and consequently a decrease of the drain current when the drain-source bias voltage increases.

Small signal CW measurements have been achieved on a 2x25x0.5 µm² device in order to extract the electrical model [8] and the current gain, maximum available gain and unilateral gain cutoff frequencies, f_T, f_{MAG} and f_{MAX} respectively. The cutoff frequencies have been extracted from Sij parameters at V_{DS} = 15 V and gate voltages between -7 V and +2V. The maximum value of the cutoff frequencies has been obtained for V_{GS} = -4 V, with f_T = 22 GHz, f_{MAG} = 47 GHz and f_{MAX} = 50 GHz, what is very promising in comparison with the state of the art, knowing that the gate does not present a T topology and that no field plate has been achieved. Figure 4 presents the evolution of these gains versus frequency.

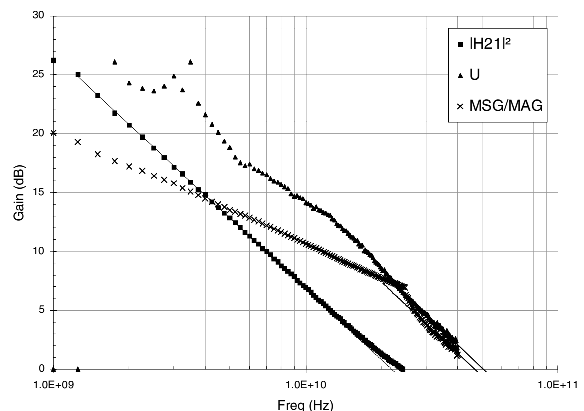


Fig. 4. Evolution of the various gain and visualisation of the cutoff frequencies of these gains for V_{DS} = 15 V and V_{GS} = -4 V.

The usual small signal electrical model has been used to extract the elements of the equivalent scheme of the device. Then the usual method to extract the parasitic elements has been used to determine the intrinsic parameters at V_{DS} = 15 V versus V_{GS} [8]. Figure 5 presents the evolution of C_{gs} and C_{gd} capacitances, g_m transconductance and g_d output conductance versus gate voltage. At V_{GS} = -4 V, the values of the intrinsic transconductance and the gate-source capacitance are 190 mS/mm and 860 fF/mm respectively. Starting from the equivalent scheme, extracted from S parameters measurements, cutoff frequencies are calculated. They are equal to 35, 29 and 22.5 GHz for F_C, F_{Tint} and F_{Text} (considering Rs) respectively. These results are in good agreement with the cutoff frequencies obtained from small signal measurements.

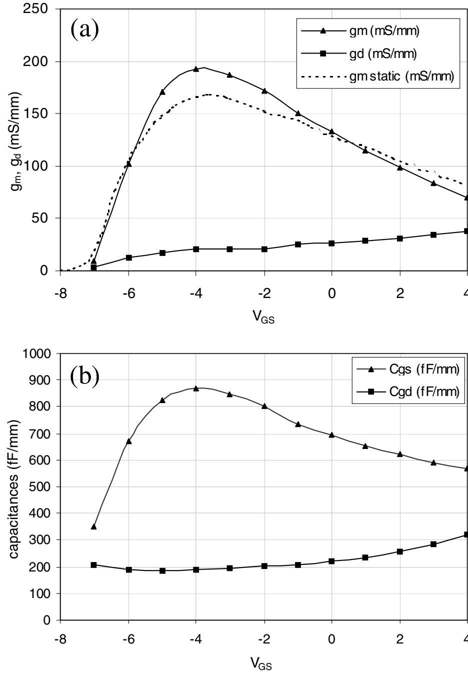
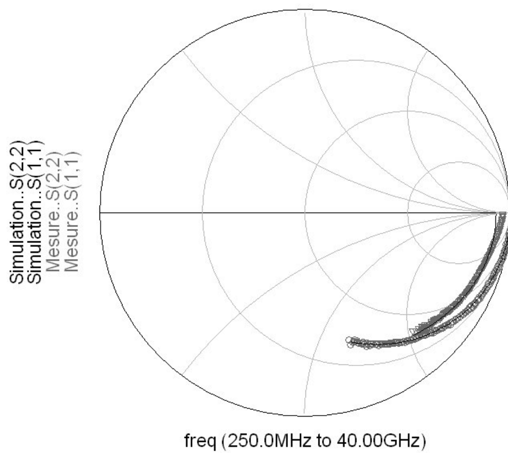


Fig. 5. Evolution of the intrinsic transconductance (g_m) and output conductance (g_d), and the extrinsic transconductance in DC mode versus the extrinsic V_{GS} voltage (a). Evolution of the intrinsic C_{gs} and C_{gd} capacitances versus the extrinsic V_{GS} voltage (b). V_{DS} = 15 V.

The evolutions of the measured Sij parameters have been compared with the Sij simulated. A good correspondence between simulation and measure is obtained in the entire V_{GS} range. Figure 6 illustrates this agreement, where the frequency evolution of the measured and simulated Sij parameters at a V_{GS} voltage of -4V and a V_{DS} of 15 V are presented. So the usual electrical model, associated with the usual electrical element extraction methods, permit to represent with a good approximation the small signal behavior of a GaN HEMT in planar technology.



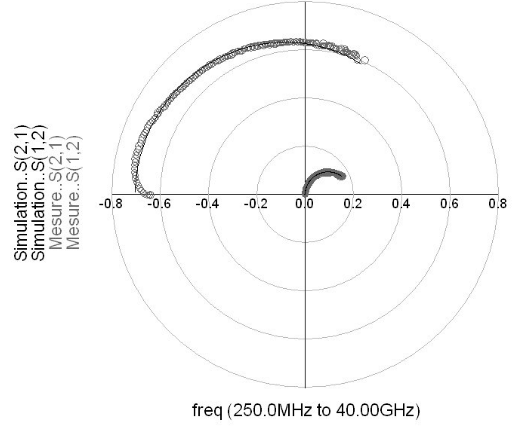


Fig. 6. Evolution of the simulated and measured S-parameters at V_{DS} = 15 V and V_{GS} = -4 V. The device geometry is 2x25x0.5µm^2 and the frequency range is 250MHz – 40GHz.

IV. Power Results

The 2x25x1.5 µm² transistor has been measured at 4 GHz with a passive load pull system under microwave probes.

The component matching has been done using a double slug tuner in order to obtain a maximum output power at V_{DS} = 30 V and V_{GS} = -3 V. Figure 7 presents the evolution of output power, power added efficiency and power gain versus absorbed input power for the optimal load impedance (Z_{load}= 910 + j162 Ω). The real part of this impedance has been determined from the DC characteristics, and the imaginary part has been tuned in order to reach the maximum output power.

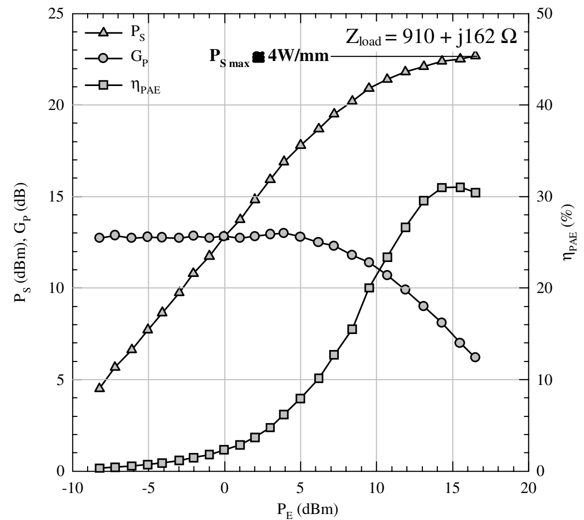


Fig. 7. Evolution of output power, power added efficiency and power gain versus absorbed input power for the optimal load impedance (Z_{load} = 910 + j162 Ω).

The maximum output power reaches 4 W/mm, the respective power gain is about 6 dB (the linear power gain is 13 dB) and the associated power added efficiency is 32 %. These results represent to our

knowledge the state of the art for GaN HEMT on sapphire substrate isolated by argon implantation. Therefore, the output power density expected from the DC characteristics ($P_{DC} = \Delta I_{DS} \times \Delta V_{DS} / 8 = 6.8$ W/mm) is not reached. This difference can be due to trap effects like it has been previously demonstrated [9].

V. Conclusion

Static and small signal CW frequencies measurements shown very promising performances like a high drain current density and good cut-off frequencies. The usual small signal model and the extraction method of the elements have permitted to calculate the cutoff frequencies of various gains. The calculated and the measured cutoff frequencies values are in good agreement. That permits to valid the model and the extraction method. Measurements in large signals regime demonstrate a maximum output power density of 4 W/mm at 4 GHz. This result shows the high potential of GaN HEMT in planar technology. There is still a weak difference between the output power density expected and the measured one. This phenomenon (trap effects) can be reduced by a passivation process.

Acknowledgement

The authors wish to acknowledge the DGA (french army) for his support, by the contract n° 01.34.050.

References

[1] Y.F. Wu, A. Saxler, M. Moore, R.P. Smith, S. Sheppard, P.M. Chavarkar, T. Wisleder, U.K. Mishra, and P. Parikh, "30-W/mm GaN HEMTs by Field Plate Optimization," *IEEE Electron. Dev. Lett.*, March 2004, 25, (3), pp 117-119.

[2] A. Chini, D. Buttari, R. Coffie, S. Heikman, S. Keller, and U.K. Mishra, "12W/mm power density AlGaN/GaN HEMTs on sapphire substrate," *IEE Electron. Letters*, 40, (1), Jan 2004, pp 73-74.

[3] J.W. Johnson, E.L. Piner, A. Vescan, R. Therrien, P. Rajagopal, J.C. Roberts, J.D. Brown, S. Singhal, and K.J. Linthicum, "12 W/mm AlGaN-GaN HFETs on Silicon Substrates", *IEEE Electron. Dev. Lett.*, July 2004, 25, (7), pp 459-461.

[4] Z. Bougrioua, I. Moerman, N. Sharma, R.H. Wallis, J. Cheyns, K. Jacobs, E.J. Thrush, L.Considine, R. Beanland, J.-L. Farvacque, C. Humphreys, "Material Optimization for AlGaN/GaN HFET applications", *J. Crystal Growth,* vol. 230, pp 573-578, 2001.

[5] B. Boudart, Y. Guhel, J. C. Pesant, P. Dhamelincourt and M. A. Poisson, "Raman characterization of Ar^+ ion-implanted GaN", *Journal of Raman Spectroscopy*, vol. 33, pp. 283-286, 2002.

[6] J. Wurfl, V. Abrosimova, J. Hilsenbeck, E. Nebauer, W. Rieger and G. Trankle, "Reliability considerations of III-nitride microelectronic devices", *Microelectronics Reliability*; vol 39, pp. 1737-1757, 1999.

[7] F. Ren, J.R. Lothian, S.J. Pearton, C.R. Abernathy, C.B. Vartuli, J.D. Mackenzie, R.G. Wilson and R.F. Karlicek, "Effect of dry etching on surface properties of III–nitrides", *J. Electron. Mater.* , vol 26, pp. 1287-1291.

[8] G. Dambrine, A. Cappy, F. Heliodore and E. Playez, "A new method for determining the FET small-signal equivalent circuit", *IEEE Trans. On Microwave Theory and Techniques*, 1988, vol. 36, (7), pp 1151-1159.

[9] N. Vellas, C. Gaquiere, F. Bue, Y. Guhel, B. Boudart, J.C. De Jaeger, and M. A. Poisson, "Load Impedance Influence On The $I_D(V_{DS})$ Characteristics Of AlGaN/GaN HEMTs In Large Signal Regime At 4GHz", *IEEE Electron. Dev. Lett.*, vol. 23, No 5, pp 246-248, May 2002.