# A InGaP/GaAs HBT WLAN Power Amplifier with Power Detector

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***Abstract* —A two-stage InGaP/GaAs heterojunction bipolar transistor (HBT) power amplifier is developed for WLAN 802.11b application. This is integrated with power detector that senses input power of power stage in order to decrease output power loss of detecting. The power amplifier delivers up to 26dBm output power with the maximum power-added efficiency (PAE) of 31% including consumption of the power detector under the supply voltage of 3.3V**

## I. INTRODUCTION

In wireless systems, the power amplifier (PA) is one of the highest energy-consuming components. The efficiency of the power amplifier is the key requirement [1]. To improve power added efficiency (PAE), an RF power amplifier can be operated in high efficient modes such as class-B, class-E, and class-F. However, these high efficiency amplifiers have nonlinearity, which result in unacceptable adjacent channel power ratio. In order to satisfy the linearity requirement, power amplifiers are typically operated in linear Class-A or Class-AB configurations [2]. But these power amplifiers have low power efficiency. The gain should be increased to improve PAE in the same supply voltage. To increase the overall power amplifier gain, the number of stages in PA must be increased. This increases the chip size, as well as idle bias currents. If the gain of each stage power transistor is quite high, two-stage configuration achieves the enough gain. A method to increase gain in a power transistor is to use a split R/C ballasting power transistor [3]. A power detector to measure the RF output power is the key requirement for power control. Usually, output power is monitored at output load, which causes the degradation of output power [4-5].

In this paper, the input power of power stage is sensed, and the power level is indicated by the output voltage of power detector. The two-stage power amplifier, which comprises of high gain power transistors, is presented.

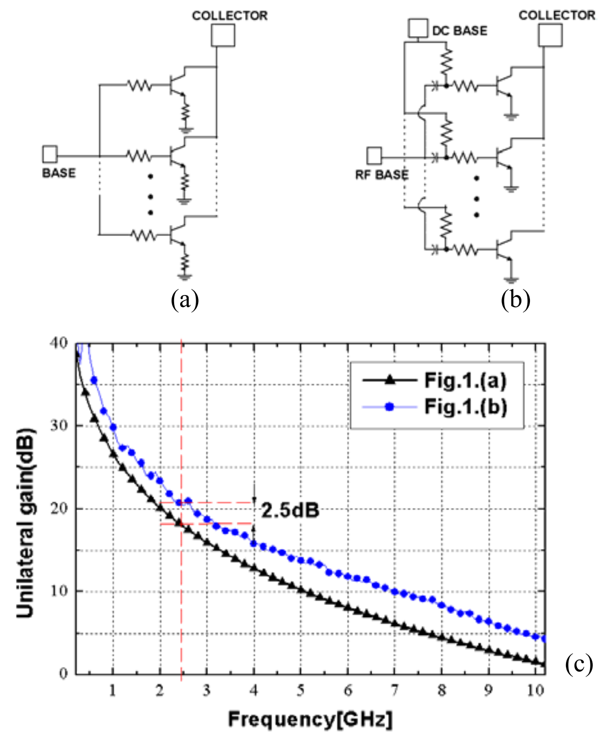


Fig.1. (a) Base & emitter ballasting (b) Split R/C ballasting (c) Measured unilateral gain of two structures at same bias condition. (The emitter size is 1920um$^2$)

## II. DEVICE CHARACTERISTICS

As in Si BJT, HBT exhibits thermal instability-related failures when operated under large dc or RF drive conditions. Thermal instability can be reduced by use of ballast resistors in series with each emitter or base as shown in Fig 1. (a) [6]. But a major problem with this ballast resistance is RF gain degrading. To solve the problem, the power transistor is designed with split R/C ballasting. Fig.1 (b) illustrates the scheme of the split R/C ballasting. The DC ballast resistors have no effect on RF gain performance. This structure shows improvement of

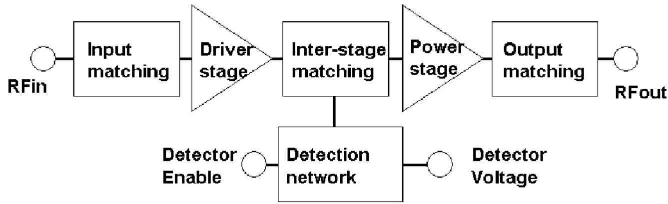


Fig. 2. The topology of the power amplifier with proposed power detector.

about 2.5dB unilateral gain compared with base and emitter ballasting in 2.45GHz at same bias condition as shown in Fig 1. (c). Power transistor is modeled including self-heating and ambient temperature effects [7].

## III. 2-STAGE POWER AMPLIFIER WITH POWER DETECTOR

The topology of the power amplifier with proposed power detector is described in Fig. 2.

### *A. Power detector*

So far, power detection by diode and log amp at power stage output is a simple method that detects power delivered to the load [8]. However, these detection methods decrease output power, directly. The output power is related to emitter area of power stage. To get same output power, the power transistor needs the more emitter area.

The power detection at the input of the power stage is good approach to decrease output power loss. Because input power of power stage does not follow power stage output characteristics, the detection amplifier is needed to follow power stage output. A similar structure is seen by [9]. A part of detection is integrated in [9], which needs additional circuits to get power detector voltage. Also, it uses common bias circuit with power stage, power detector is always turned on. Considering detector transistor operation current in detection circuit, detector on/off is needed for not working detection. In this paper, a simple structure is integrated which get power detector voltage and turn on/off the power detection.

As shown in Fig 3., because the detector amplifier of power detection is designed to follow power stage characteristics, it has some PAE degradation. To get less degradation, the detector amplifier is working in low bias region. It makes input of diode decreased, output detector voltage has low dynamic range. To compensate this effect, diode has $V_{DYNAMIC}$ .In measurement result, detector voltage of power detector has 0.2 to 1.2V as output power sweep 0 to 24dBm.

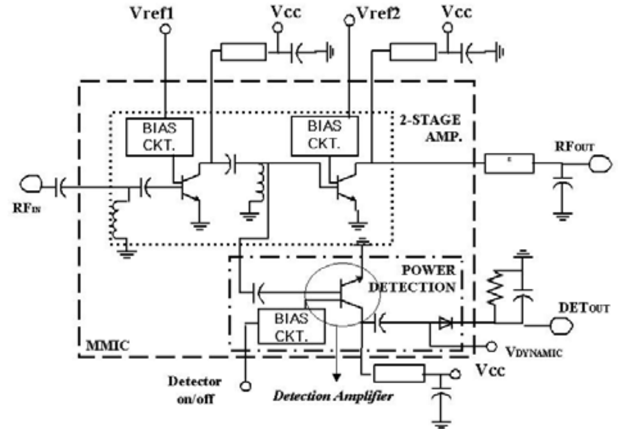


Fig. 3. Schematic diagram of the fabrication InGaP/GaAs power amplifier with power detector.

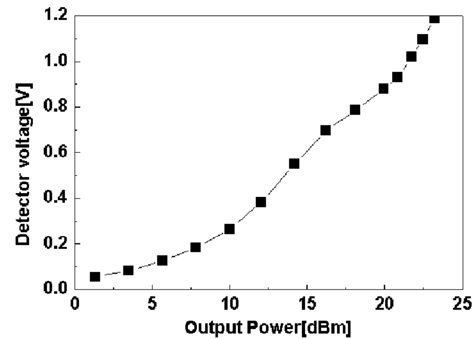


Fig. 4. Measured detector voltage

### *B. Power amplifier*

The two-stage power amplifier was implemented with InGaP/GaAs HBT technology. The emitter sizes of the first stage and second stage HBT were $480um^2$ and $1920um^2$. The detail schematic diagram of the circuit is displayed in Fig. 3. The power amplifier has an integrated input and interstage-matching network. The optimum input and output impedance of the HBTs are determined by large-signal models [7].

Bias circuits are completely on-chip except the collector circuitry of the output stage. This part is off-chip to minimize power loss. The bias current level can be tuned to a desired value by controlling the reference voltage (Vref) in the bias circuit.

## IV. MEASUREMENT

Fig. 5. is photograph of the power amplifier with integrated power detector. The chip size is 1.2mm× 1.0mm. Fig. 6, 7, 8 shows the measured results of the power amplifier at 2.45GHz. The bias current is set to 37mA and 83mA for driver and power stage with a supply voltage of 3.3V.

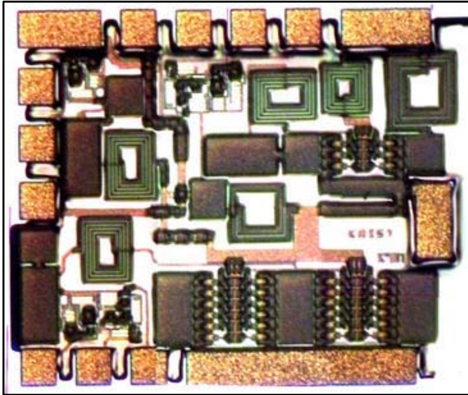

Fig.5. Photograph of power amplifier

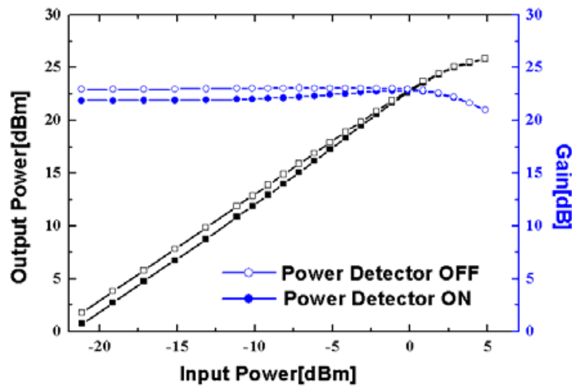


Fig.6. Measured output power and gain of power amplifiers

When power detector is on, power amplifier achieves $P_{1dB}$ of 26 dBm and a gain 22 dB. The power added efficiency is over 31%. $P1_{dB}$ is not degraded, as was expected. The gain is degraded about 1dB.IMD is measured as –20dBc at 24dBm in ±500KHz offset frequency. In simulation result the IMD is –27dBc at 24dBm, the difference is presented by in accurate measurement setup.

## V. Conclusions

A two-stage InGaP/GaAs HBT power amplifier with integrated power detector for wireless LAN application is presented. The output voltage of power detector indicates the power level. The power amplifier has 31 % PAE at 26 dBm output power with 22 dB gain at 2.4 to 2.5 GHz. Power detector consumes 0.4dB of output power at $P1_{dB}$.


## Acknowledgement

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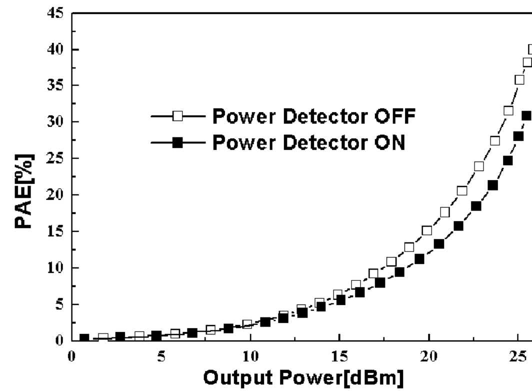


Fig.7. Measured PAE.

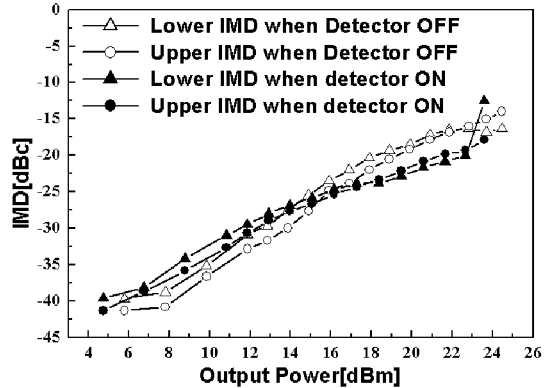


Fig.8. Measured IMD.

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