Low Phase Noise, Very Wide Band SiGe Fully Integrated VCO

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***Abstract* — This paper presents a fully integrated, low phase noise SiGe voltage-controlled oscillator with very wide band for digital radio link applications. The VCO has been fabricated using IBM 0.5µm SiGe5AM process. A measured 38.5% tuning range around 5.2 GHz and a single-sideband phase noise varying between –100 and –96 dBc/Hz at 100kHz offset from carrier have been achieved. The oscillator's core draws 9 to 17mA from a 3V supply voltage.**

I. Introduction

Silicon germanium (SiGe) technologies allow to achieve optimum performance in analog applications and at the same time to integrate in one single device all the digital functions for a phase locked loop (PLL) circuit, thus allowing to shrink the system's size. This has always been vital for handsets, but it is becoming more and more important for any system to reduce costs. Within this picture, besides aiming at a low phase noise specification, an important target is to design a single frequency generating device able to cover the whole required frequency range (including process spreads). That leads to a very low cost solution: one part number for higher volumes.

SiGe has already been proved to be a suitable technology for low phase noise VCO implementations [1]. However, our specific application imposes tight requirements for both phase noise performance (-103 dBc/Hz @ 100kHz) and tuning range (40% around about 5GHz). Hence, a design methodology aimed to achieve the best trade-off between very wide tuning range and low phase noise must be developed and it will be here presented. Moreover, it must be pointed out that at frequencies around 5GHz the importance of accurate distributed components models and/or electromagnetic simulations becomes relevant. These two kinds of analysis were jointly used during the design.

II. Oscillator's Core Design

The tight phase noise requirements make it necessary to choose a SiGe BiCMOS technology instead of a standard CMOS technology, in order to reduce flicker noise contribution to close-in phase noise.

A classical differential topology was used as a basis for the VCO core design (Fig. 1). The starting point for the phase noise minimization is the well-known formula relating the Single-Sideband to Carrier Ratio (*SSCR*) to circuit parameters [2]:

$$SSCR(\omega_m) = \frac{2kT}{C} \cdot \frac{\omega_0}{Q} \cdot \frac{1+F}{A_0^2} \cdot \frac{1}{\omega_m^2} \qquad (1)$$

where C is the total tank capacitance in parallel with the inductance L, Q is the LC tank quality factor, ω_0 is the oscillation frequency, F is the noise factor taking into account noise from the active circuitry and A_0 is the differential oscillation amplitude.

Two are the main targets in the design of the oscillator's active circuitry: the maximization of the oscillation amplitude and the minimization of the noise factor. The oscillation amplitude is often a limiting factor in bipolar realizations, since A_0 has to be kept low enough to avoid the base-collector junctions of the differential pair's transistors Q_1 and Q_2 being forward-biased during the oscillation peaks. In order to increase the maximum oscillation amplitude, two design techniques are here adopted. First, the bases of the transistors are dc-biased at a voltage V_B lower than V_{DD} through two bias resistors R and ac-coupled to the oscillator's outputs by the capacitors C_1. The voltage V_B is set to the lowest value compatible with the required tail current generator voltage headroom.

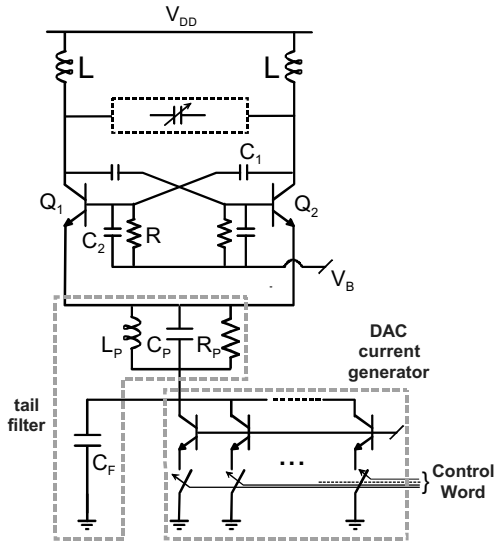

Fig. 1. Oscillator simplified schematic.

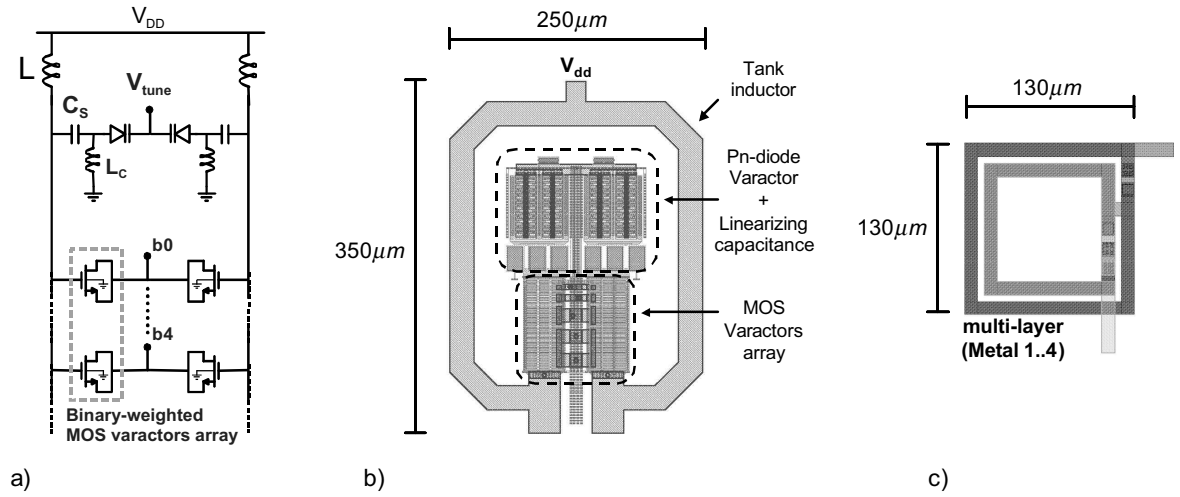

Fig. 2. a) LC tank structure. b) LC tank layout. c) Stacked multi-layer choke inductor layout.

The second technique is based on the use of two capacitors C_2 which attenuate the signal across the bases of the transistors Q_1 and Q_2 by a factor $n = C_1/(C_1 + C_2)$. That allows to further increase the oscillation amplitude without forward-biasing the base-collector junctions. However, reducing the amplitude of the signal driving the differential transconductor has several drawbacks. First, the oscillator's open loop gain is reduced by the same factor n, leading to potential start-up problems. Second, due to the smaller input signal, the active transconductor works in the linear region for a longer time interval within the oscillation period. Since noise from the transistors Q_1 and Q_2 is injected into the tank only when the differential pair works in the linear region [3], that leads to a higher noise factor F. In the proposed design, a factor $n = 3$ has been chosen as a good compromise between oscillation amplitude and noise factor degradation. With a supply voltage $V_{DD} = 3\text{V}$ and $V_B = 1.6\text{V}$, the maximum oscillation amplitude is approximately $A_0 = 2.5\text{V}$.

Due to the large required tuning range, an amplitude calibration mechanism has to be implemented in order to keep the oscillation amplitude always at its maximum. In the current-limited regime, A_0 is given by:

$$A_0 = \frac{4}{\pi} I_B \cdot \omega_0 L Q \qquad (2)$$

Therefore, oscillation amplitude shows a strong dependence on the output frequency, which has to be compensated by varying the bias current I_B. A current DAC has been designed as tail generator (Fig. 1). Using this DAC, a digital amplitude control system can be easily implemented [4].

The noise from the tail generator can be a relevant source of phase noise, since noise around the even harmonics of the output frequency is down-converted around ω_0 by nonlinear mechanisms [2]. A second-harmonic tail filter [5] has been designed in order to eliminate this contribution. A filter capacitor C_F shunts current noise around the even harmonics of ω_0, while a parallel resonant network L_P-C_P tuned at $2\omega_0$ presents a high-impedance to the sources of the differential pair Q_1-Q_2. A parallel resistor R_P has been inserted in order to enlarge the filter's bandwidth up to the oscillator's tuning range.

III. LC TANK DESIGN

From (1) it is evident that, as the tank capacitance C is enlarged, phase noise improves. Since the inductance L must be correspondingly reduced, it follows from (2) that the current I_B has to be increased in order to keep the same oscillation amplitude. Therefore, the noise-power product is unchanged.

However, practical considerations impose an upper limit to the value of the tank's capacitance. First, the inductance value can be too small to be practically implemented as it becomes comparable to the interconnections' parasitic inductance. Second, the tank capacitance C can cover an area even larger than the inductor's one, leading to a very troublesome layout and longer connections for the inductor. Moreover, a large capacitance and a small inductance lead to a high sensitivity of the tank's quality factor to interconnections' parasitic resistance, thus limiting the maximum achievable Q.

A value of $L = 260\,pH$ has been chosen as a good compromise between phase noise and robustness against parasitics. The low inductance value allows the use of a single-turn inductor, which intrinsically has a higher quality factor due to the reduction of current-crowding effects typical of multi-turns inductors [6] and a much lower parasitic capacitance thanks to the absence of inter-winding capacitances. A full-custom single-coil center-tapped inductor has been designed using the available thick top metal in order to maximize the quality factor. Commercial 3D EM simulators have been employed to optimize the inductance geometry, and the simulated quality factor is about 25-30 in the 4-6GHz range.

The design of the tank's capacitance entails a fundamental trade-off between quality factor and tuning range. A wide tuning range requires varactors with high C_{MAX}/C_{MIN} ratio . As an example, in MOS varactors this

ratio rises as the MOS channel length is increased, since C_{MIN} becomes less affected by parasitics (overlap gate capacitances and source-drain parasitic diodes). However, the varactor's quality factor is inversely proportional to the square of the channel length [7].

A similar trade-off is also encountered if switched metal-insulator-metal (MIM) capacitors are used [8]. In fact, to reduce the on-resistance and improve the quality factor, the MOS switch width must be enlarged, thus increasing the parasitic capacitance and decreasing the overall capacitance variation.

The low flicker noise up-conversion requirement [9] pushes toward a mixed analog/digital frequency control, in order to cover a wide tuning range while keeping a low VCO gain. A binary-weighted array of five inversion-mode nMOS varactors (Fig. 2.a) has been used due to their higher C_{MAX}/C_{MIN} ratio compared to the available pn-diode varactor. The MOS varactors are biased either in the depletion or in the inversion mode through binary control signals $\{b0..b4\}$. In our 0.5µm technology, a non-minimum channel length of 1µm has been chosen in order to guarantee the required 40% VCO tuning range. That leads to a low quality factor: VCO measurement results show that a Q below 7 at 5GHz has been obtained. As will be discussed in Section IV, the poor quality factor of the MOS varactors greatly affected phase noise performance.

Fine-tuning is achieved through a pn-diode varactor. The varactor is linearized through a series capacitor C_S, thus reducing the VCO sensitivity (60 MHz/V average).

The varactors' cathode is biased to ground using two choke inductors L_C instead of two resistors, thus avoiding additional noise sources. However, choke inductor's losses can degrade the tank's quality factor, since the inductance L_C is in parallel to the tank's inductance L, neglecting the effect of the capacitive voltage divider composed by the linearizing capacitance C_S and the pn-diode capacitance. In order to keep the equivalent parallel loss resistance of the choke inductor much higher than the one of the LC tank, the following relationship has to be satisfied:

$$\omega_0 L_C Q_C > \omega_0 L Q \tag{3}$$

where Q_C is the choke quality factor. Therefore, a high $L_C \cdot Q_C$ product is required, i.e. a high inductance value with a high self-resonant frequency. Achieving these two goals at the same time is a challenging task. A variant of the multi-layer stacked inductor, already proposed in [10], has been recognized as the best solution and designed with the help of EM simulators. An inductance of 5nH, with a quality factor of about 2 and a self-resonant frequency well beyond 5GHz has been obtained with a significant area reduction (about 75% if compared to a classical single-layer spiral inductor). The layout of the designed choke inductor is depicted in Fig. 2.c.

The LC tank layout is reported in Fig. 2.b. As already discussed, the sensitivity of the overall quality factor to interconnections' parasitic resistances is very high due to the low inductance value and the big tank's capacitance. Hence, the tank's varactors have been laid out inside the inductor coil, in order to minimize the parasitic series resistances and inductances. The presence of metal structures inside the inductor coil potentially leads to an increase of losses and a decrease of the actual inductance value. Therefore, the entire structure has been re-simulated in order to consider electromagnetic coupling effects.

IV. Measurement Results

The proposed oscillator has been fabricated in IBM SiGe5AM BiCMOS process. The chip microphotograph is reported in Fig. 3.

The measured tuning characteristic is plotted in Fig. 4. A 38.5% tuning range around 5.2GHz has been obtained, partitioned into 32 overlapping frequency bands. The oscillator can be used within a phase-locked loop implementing a mixed signal frequency control [11].

Measured phase noise near the two edges of the tuning range is reported in Fig. 5. A SSCR varying from –100 to –96 dBc/Hz @ 100kHz has been achieved. A flicker noise frequency corner well below 100kHz is observed, thanks to the reduction of AM/PM conversion effects through the mixed A/D frequency control. The VCO core current consumption varies from 17mA at the lower edge of the tuning range to about 9mA at the upper edge.

Observed phase noise is about 10dB higher than that expected from simulations, both in the $1/f^2$ and in the

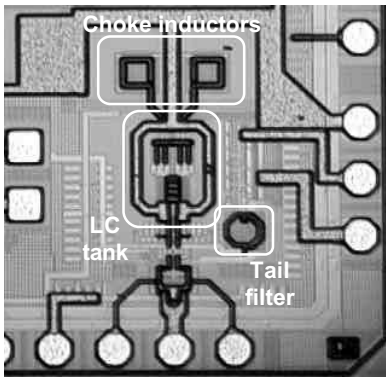

Fig. 3. Chip microphotograph. The VCO core area, including choke inductors, is about 1mm^2.

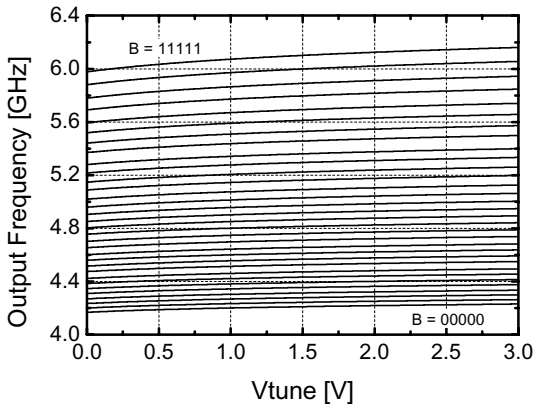

Fig. 4. VCO tuning curves vs tuning word $B=\{b0..b4\}$ and tuning voltage V_{tune}.

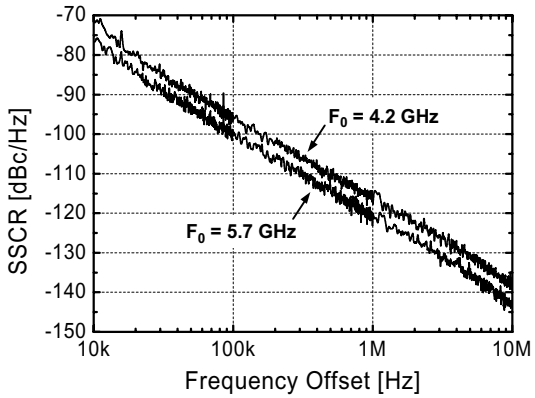

Fig. 5. Measured phase noise near the two edges of the tuning range

$1/f^3$ region. First, the quality factor of the MOS varactors used as switched capacitors, extrapolated from phase noise measurements, is much lower than expected (below 7 at 5GHz). That leads to an overall Q degradation and oscillation amplitude reduction, which strongly affects phase noise performance. Unfortunately, an accurate RF model of inversion-mode MOS varactors taking resistive losses into account was not available during the design. Second, flicker noise of bipolar devices has been measured using a separate test-structure integrated in the same die. Measurement results have been compared with the device model prediction (Fig. 6). Measured flicker noise is about 10dB higher, in accordance to the observed phase noise degradation in the $1/f^3$ region.

Nevertheless, the achieved oscillator Figure-Of-Merit (FoM), defined as:

$$FoM \triangleq \left(\frac{\omega_0}{\omega_m}\right)^2 \cdot \frac{1}{SSCR(\omega_m)\cdot P_{diss,mW}} \qquad (4)$$

varies between 175 and 177dB and it is quite good compared to recently published results [12], especially considering that the FoM definition does not take into account the VCO tuning range, which has to be traded against the obtainable SSCR and the available technology limitations.

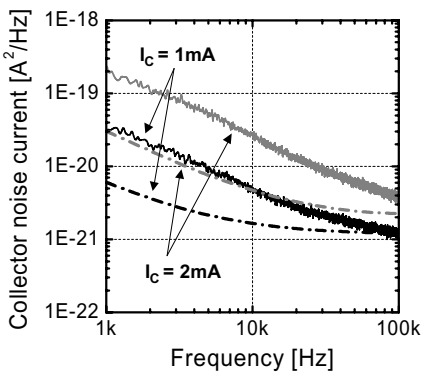

Fig. 6. Measured flicker noise of bipolar devices (emitter area 2.5μm^2) for two different values of bias current. Simulation results are also plotted (dash-dotted lines).

V. Conclusion

A low cost, very wide tuning range, low phase noise VCO has been fabricated using IBM SiGe5AM 0.5μm BiCMOS technology. The design steps followed to optimize the phase noise performance over a very wide tuning range have been illustrated. The main design issues, such as oscillation amplitude maximization, noise factor minimization and the trade-off between phase noise and tuning range have been highlighted. The importance of high frequency EM analysis for careful evaluation of custom inductors has been also discussed.

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