A Method for PA-Patch Antenna Design Optimisation Oriented to Maximum Efficiency

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***Abstract* — The integrated design of a high-efficiency stage and an antenna patch is presented. Moving from the optimality conditions regarding efficiency of the power amplifier designed according to harmonic tuning strategies, the antenna patch is optimized to present the so obtained loading impedances. The resulting assembly is featured by high efficiency, compactness and a reduced level of spurious frequencies emissions.**

I. INTRODUCTION

In wireless communication systems many research efforts are devoted to the design of lightweight, compact, low cost and low-power dissipation transmitters. For this reason, design of high efficiency power amplifiers and its integration with the antenna system, become a very interesting design challenge.

Recently, the combination of integrated antennas and high-efficiency power amplifiers (PAs), resulting in additional functionality and reduced complexity and size have been proposed in literature [1, 2, 3].

Nevertheless, such active systems usually are not the results of a fully integrated approaches, being the product of the combination of 50 Ω output matched amplifier with an integrated antenna (patch), exhibiting different load impedance values. In particular, usually the PA and the IA are separately optimised and designed, while a passive two-port network is designed afterwards to realise the required impedance transformation and the transition between the different guiding structures and materials usually adopted.

In this paper a fully integrated active antenna design approach is proposed, in which the antenna and the amplifier are *simultaneously* designed and optimised, while minimising the radiation at the harmonic frequencies

II. ACTIVE PATCH DESIGN APPROACH

The design of a power amplifier implies the synthesis of both input and output networks, following different criteria. The input network is designed to assure the conjugate matching condition, i.e. maximum power transfer between the external source and the active device. The output network is designed to maximise output power delivered to the load (in the present case the antenna), maximising at the same time the efficiency and reducing power dissipation.

This result is obtained by a proper shaping of voltage and current waveforms, through an active device switching mode operating condition [**4**] or suitable harmonic load impedance synthesis [**5**]. In the latter case, more suitable for high frequency applications, a design theory proposed in the past [**6**] suggest the optimum ratios between harmonics and fundamental voltage components, according to the number of harmonics that can be effectively controlled.

If a patch antenna is the load of the power amplifier, taking into account the improvements achievable and the circuit complexity, a suitable design approach results in the use of a 2nd and 3rd harmonic tuning.

Thus, the active array design criteria can be summarised in the following 3 steps:

I) find the optimum harmonic load impedances, both at the input and output ports of the active device, by means of a simulated "harmonic load pull" of the power stage;
II) design an integrated antenna whose impedance levels are "close" to the above optimum impedances;
III) design the power stage input network to satisfy the conjugate matching condition and the output network to transform the patch antenna impedance levels to the necessary harmonic tuning ones, found at point I), by a compact matching network.

A. Power Stage Optimum Load Impedances

The active device used is a medium power MESFET by Alenia Marconi Systems (AMS) with a Class AB bias ($I_{dc}=I_{dss}/3\approx80$mA; $V_{DD}=5$V.) and 1-mm gate periphery. The device has been modelled in-house by a full nonlinear model, extracted using multibias S-parameter and pulsed-dc measurements. The fundamental operating frequency is 5 GHz. Both the input (Z_s) and the output (Z_L) impedances have been tuned to the optimum values, in order to realise a 2nd Harmonic Tuned (HT) amplifier. The optimum load values obtained are graphically depicted in fig. 1 and summarised in table 1.

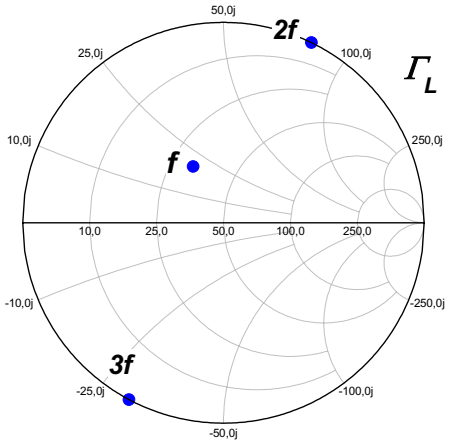


Fig. 1. Optimum output load termination for 2nd HT power stage.

TABLE 1. Optimum harmonic load impedances for a 2nd HT power amplifier

	2nd HT amplifier	
	INPUT (Zs)	OUTPUT (ZL)
f (5 GHz)	13+j18	32+j20
2f (10 GHz)	Short	j80
3f (15 GHz)	Short	-j30

B. *Integrated Antenna Design*

When the antenna is used for harmonic tuning, the input impedance at the operating frequency and at the first two harmonics must be chosen to maximize the amplifier performances while preserving reasonable radiation features.

A microstrip-fed rectangular patch has been considered as basic radiator, though different configurations could be adopted [2].

The antenna should be designed in order to synthesize input impedance values close as much as possible to the values obtained during power stage optimization (step I), minimizing unwanted radiation which could cause electromagnetic interference, degrading overall system performances. Since in a rectangular patch antenna resonant modes are excited close to multiples of the fundamental resonance, the antenna shape and feed interconnection need to be properly designed to minimize the excitation of the TM_{02} and TM_{03} modes, while preserving the fundamental TM_{01} mode.

The geometry adopted is shown in fig 2. With reference to modal field oscillations within the patch, the TM_{02} mode is eliminated by inserting a row of shorting pins along the center line of the patch [2], where the TM_{02} peaks while the TM_{01} is short circuited. Ideally, the TM_{03} mode could be suppressed if the source is placed at a TM_{03} null which roughly occurs at a distance of L/6 (L being the resonant patch side) from the patch edge.

The patch optimization procedure has been the following:

- design L for TM_{01} resonance at f_0
- choose the pin position (u) to minimize the input resistance at $2f_0$
- re-tune (L) the patch at f_0
- starting from ℓ=L/6, optimize the inset length (ℓ) to minimize input resistance at $3f_0$

The antenna geometry has been modeled by a standard Moment Method tool, and the computed input impedance and reflection coefficient are shown in fig 3.

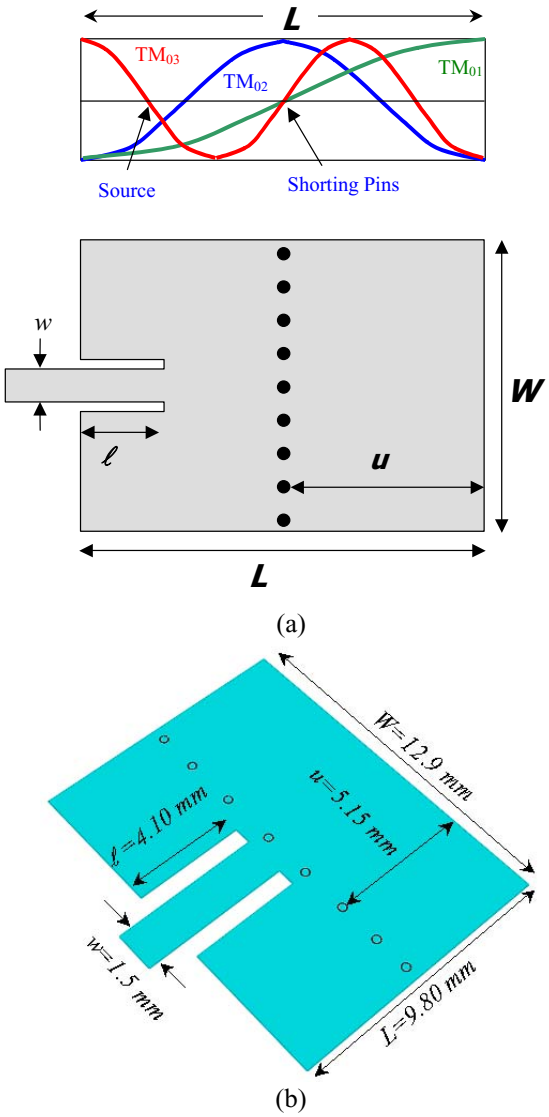
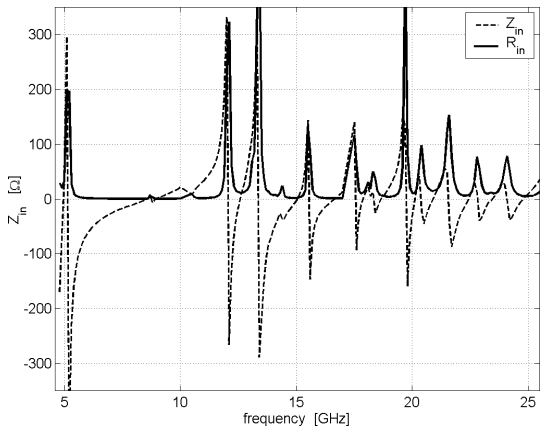


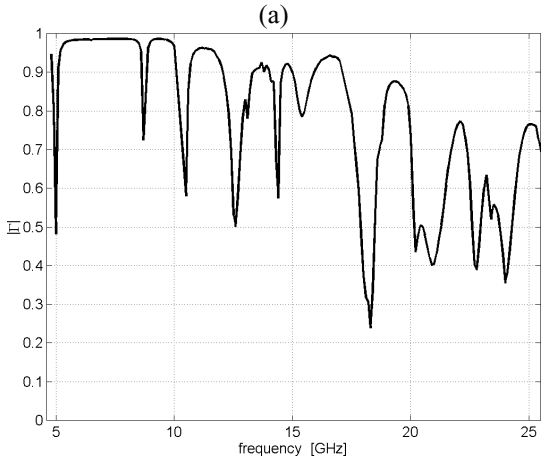
Fig. 2. (a) The oscillation of electric field along the patch resonant length L and the modified rectangular patch geometry adopted for higher harmonic control. (b) the optimised patch array

As expected by the position of the microstrip interconnection close to the patch center, a low input impedance (30Ω) at fundamental frequency has been obtained, as required for amplifier performance optimization. Moreover, the resonance at 10GHz and at 15GHz have been suppressed while the input impedance at higher harmonics result to be $Z_{in}(10GHz)=0.8+j20\Omega$ and $Z_{in}(15GHz)=1.7+j3.5\Omega$, respectively. As it can be noted, input resistance is nearly negligible in both cases.

The maximum directive gain at the operational frequency is 3.5 dB which is slightly lower than a conventional patch without higher harmonic suppression.



(a)



(b)

Fig. 3. Input impedance (a) and reflection coefficient (b) for the optimised patch.

C. Active Array Design

The reflection coefficients of the designed integrated antenna are depicted in fig. 4 on a Smith chart (stars) and compared with the optimum load impedance values (filled circles) that the 2nd HT amplifier requires to the output port, for the first three harmonics (i.e. 5, 10 and 15 GHz).

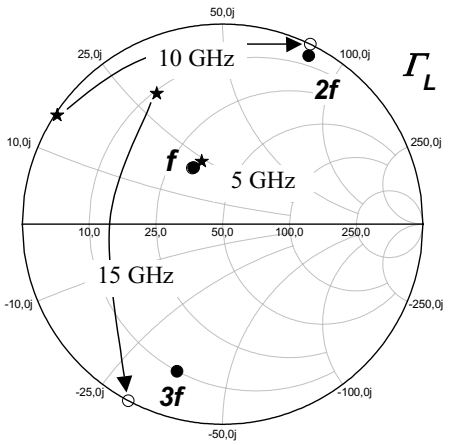


Fig. 4. Reflection coefficient of the designed patch (cross points) compared with the optimum 2nd HT amplifier output load impedance values (filled circle points). The reflection coefficients obtained at the end of matching network design procedure are represented by empty circle point.

Thus, the output matching network has been designed to perform the impedance transformation, i.e. to move the stars points toward the filled circle ones, obtaining at the end the empty circle points shown in fig. 4.Finally, the layout of the overall power stage is shown in fig. 5, including the input network, while the simulated performances are plotted in fig. 6.

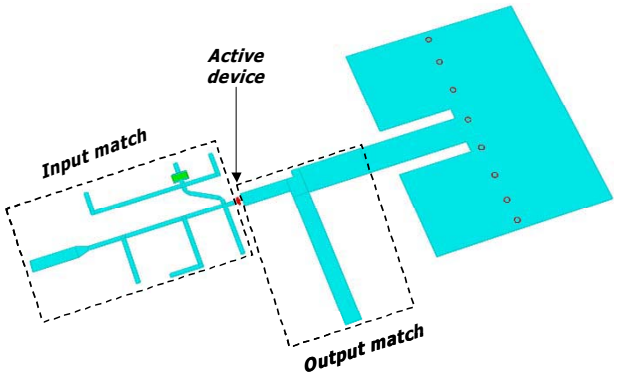


Fig. 5. Layout of the designed 2nd HT power stage.

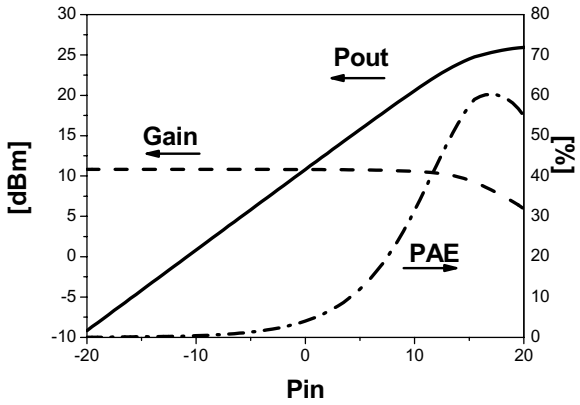


Fig. 6. Simulated active array performances

To discuss the spurious emissions from the antenna integrated with the amplifier, the Effective Isotropic Radiated Power $EIRP(\theta,\phi,f)=G(\theta,\phi,f)\cdot P_{out}(f)$ (P_{out} being the output power from the amplifier stage) has been evaluated at the fundamental frequency and at the first two harmonics. The input power P_{in} is set for maximum PAE (P_{in}=17dBm) where the corresponding output power are P_{out}(5GHz)=24.1 dBm, P_{out}(10GHz)=-6.6 dBm and P_{out}(15GHz)=-28.0 dBm. From diagrams in fig. 7 it can be observed that the second harmonic is 30dB and the third harmonic is 58.8 dB below the fundamental-frequency radiated power along the broadside direction. This is a remarkable result since with conventional harmonic tuning typical third harmonic radiation are only about 30dB below fundamental frequency radiation.

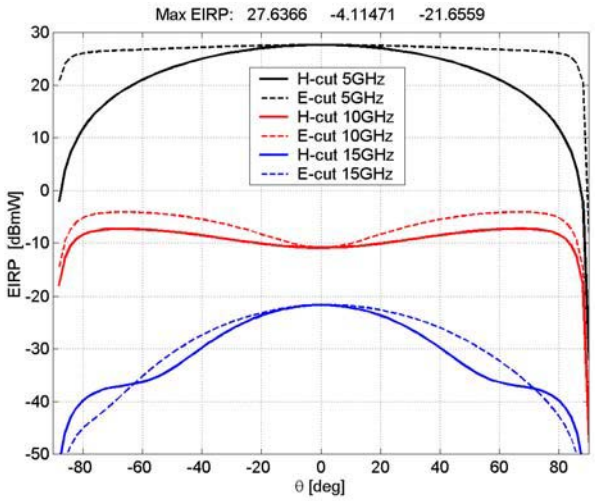


Fig. 7. Effective isotropic radiated power of fundamental, second and third harmonics for the patch antenna with high order mode suppression integrated with the amplifier.

III. Conclusion

An integrated design procedure for a high efficiency power amplifier - patch antenna combination has been described. The power amplifier has been designed making use of harmonic tuning strategies utilising proper second-harmonic loading. The patch antenna has been designed to meet optimal loading conditions for the power amplifier at fundamental, second and third harmonic frequencies, while minimising, at the same time overall system spurious emissions. Simulated results of a 5 GHz sample demonstrate a maximum power-added efficiency close to 60 % at -3 dB power compression, together with spurious emissions from the patch to -30 dBc and -48 dBc for second and third harmonic radiated power respectively.

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