MMIC implementation of a new active pre-distortion scheme for Highly Linear Power Amplifier

Andrea Meazza[1], Maurizio Pagani[1], Roberto Iommi[2], Giuseppe Macchiarella[2]

[1]CoRiTeL, Via Cadorna 73, I-20090, Vimodrone (MI), ITALY, Phone: +39-02-26598639
[2] Politecnico di Milano, Dipartimento di Elettronica e Informazione (PoliEri Lab), Piazza Leonardo da Vinci, 32 – 20133 Milano, ITALY

***Abstract* — This paper describes the complete design methodology used to implement a MMIC lineariser in 0.25um pHemt GaAs technology. Theoretical concepts and numerical simulations of a new pre-distorter prototype designed for a wide band and high linearity power amplifier are presented. Modeling and process variations sensitivity has been accurately taken into account during the implementation of the lineariser architecture allowing a time effective and safe design approach. Several parts of the main amplifier have been reused in the pre-distorter design reducing the total development lead-time and the risk of model inaccuracies.**

The implemented predistortion topology has been verified using Agilent ADS simulator showing an improvement up to 10 dBc in third order intermodulation distortion (IM3) over a relative bandwidth of 28%. These results are also confirmed by experimental characterizations that demonstrate the effectiveness of the new pre-distortion scheme and implementation methodology.

I. INTRODUCTION

MMIC technology is well recognized for its capability of reducing cost, size, weight and number of parts of modern digital radios. Monolithic circuits can be easily integrated inside multi chip modules (MCM) and they are tuneless, therefore they are suitable for volume production and automatic testing. When dealing with high spectral efficiency modulation schemes for radio equipments, i.e. 128 or 256 QAM, improving linearity and power-added efficiency in power amplifiers becomes very important. The lineariser prototype presented in this paper is mainly aimed to verify the validity of a novel pre-distortion architecture [1][2] based on a two loops scheme.

The predistorter implementation is based on a very wide band (relative bandwidth ≈ 28%), high linearity power amplifier for the frequency range 12÷16 GHz, previously developed. The adopted design choices in the prototype development have carefully considered all the issues related to process tolerances and model inaccuracies [3], which represent a relevant topic in all well designed circuits. These issues result to be even more important in MMIC technology because the tuneless nature of monolithic circuit.

II. BASIC CONCEPTS

The basic idea behind any predistorter is to create a signal that is opposite to the unwanted distortion generated by the main amplifier (MA, the amplifier to be linearised). On this principle is also based the feed-forward scheme but the cancellation of the undesired components is applied after their appearance. Instead, the predistorter here presented and implemented is based on preventing those effects. According to this, the input signal to main amplifier is distorted in such a way to avoid the creation of unwanted spurious signal at its output.

The new proposed predistortion architecture [2] is composed of two loops, the first aimed to produce the same distortion created by the main amplifier by means of a non-linear driver (NLD) and the second able to opportunely combine in amplitude and phase this distortion signal with the linear contribution coming from a linear driver (LD). The result of this processing is level adjusted by means of an output linear buffer and then injected into the main amplifier.

The creation of the same distortion produced by the main amplifier is achieved by means of the non-linear driver, a scaled down version of the main amplifier, and a linear output buffer, which allows main amplifier and non linear driver operating with the same back-off. It is assumed that the distortion components injected into the main amplifier do not affect the generation of non-linear products. This assumption is typically well verified in high linearity amplifiers operating with an adequate back off. The delay compensation of non-linear driver in the first loop is obtained using an identical driver (LD) but working in linear condition using a suited attenuation at its input. Actually, the LD is only less non-linear than the other driver (NLD). Consequently, it also generates intermodulation distortion, even much smaller than those generated by NLD. This effect is taken into consideration choosing a suitable value of the buffer gain.

The advantage of the approach based on identical drivers located on linear and non-linear path is the intrinsic ability of the circuit to automatically compensate process variations and temperature drift of drivers and main amplifier characteristics, resulting in a very robust product, a key factor for the success of any well designed MMIC device.

III. BLOCK SCHEMATIC

The simplified block diagram of lineariser is shown in Fig.1. The new predistortion approach is well suited for re-using parts of the main amplifier already simulated and tested, saving development time and reducing risks

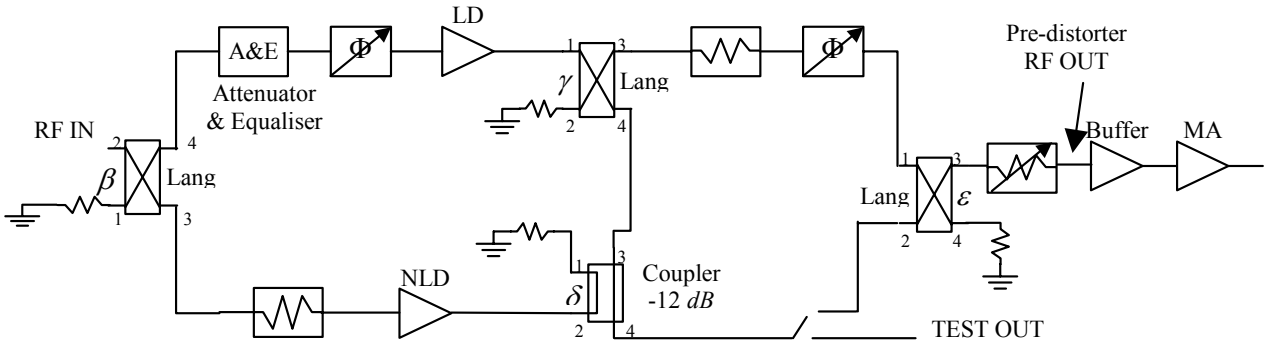

Fig. 1. Block diagram of predistortion architecture

of model inaccuracies. In particular, the balanced structure used in the main amplifier permits to re-use one half of the complete circuit as both linear and non-linear driver. This implies that the scaling factor k, as defined in [2], is equal to 3dB. This implementation approach leads to achieve drivers that are an exactly scaled down version of the main amplifier without any extra design effort. Also the Lange coupler of the main amplifier has been re-used as 3dB power splitters (block β and γ in the first loop) and as signal combiner (block ε in the second loop). An equalizer device has been added to the first loop in order to compensate for frequency dispersion of amplitude characteristics of phase shifter and coupler (block δ) over the operating band of the chip. Using this element avoids an extra attenuation control to keep the first loop balanced over the complete frequency range. It also works as attenuator in order to have the driver LD operating in linear condition.

Appling the design equations presented in [2], a first order dimensioning of lineariser blocks has been performed. The effect of mismatch among different blocks has not been taken into consideration in this early phase of the project. However, the design effort was to prevent such effect, adopting well 50Ω matched blocks and using extra attenuators at the input of both LD and NLD drivers.

From this preliminary analysis, it has been seen that it is possible to use fixed attenuators in both loops 1 and 2 without altering significantly the performances over the operating frequency range. However, it's instead useful to adopt tunable phase shifters to compensate for the considerable phase response variation over frequency of passive circuit elements in both loops. T-shunted topology LC all-pass networks have been chosen to implement the variable phase shifters. Phase control is achieved varying the bias of varactor diodes. In principle, an all-pass network requires a simultaneous control of inductance and capacitance to satisfy both phase and matching condition; as variable inductors are not available in MMIC technology, the network has been optimized around an average phase value in order to guarantee an acceptable matching level over the tune range only varying the capacitance values. It can be noted (fig.1) that the location of second loop phase shifter is along the linear path, after the linear driver. This implementation choice due to layout constrains, could affect the performances of the lineariser because the non-linear distortion created by the varactor diodes at operating power level. A more accurate design should consider the phase shifter located along the non-linear path, just after the δ coupler. In this point of the circuit the power level is much lower since the linear part of the signal is totally suppressed.

The gain control of output linear buffer, needed in order to have main amplifier and non-linear driver operating with exactly the same back off, has been implemented by means of a Π resistive attenuator, located at the output port of lineariser (RF OUT). The resistors are made with FETs operating in linear region and externally controlled by the gate voltage. As the series FET gate voltage is set for a certain attenuation level, the parallel FET gate voltages are automatically set by a suited external circuitry to keep a good 50Ω matching in all operating conditions.

The block schematic presented in figure 1, shows an auxiliary and excludible test port (TEST OUT) located just at the output of non-linear path after the δ node combiner. This test port allows optimum tuning of first loop variable phase shifter in order to achieve maximum linear component suppression along non-linear path. Moreover, when the test out port is excluded, the circuitry that implements the switch can be also effectively used as an extra variable attenuator in loop 2. This control can improve the tuning precision during the prototype measurements.

IV. CIRCUIT OPTIMISATION

The exact determination and optimization of parameter values and circuit performances has been carried out in Agilent ADS simulation environment. All the passive structures (Lange coupler, equalizer, δ coupler, inductors and connection microstrip lines) have been verified with EM simulator over a very wide band. In order to further increase the accuracy of performance prediction the varactor diodes, the drivers and the main amplifier have been characterized through small signal S-parameter measurements. The non-linear performances of drivers and main amplifier have been represented using ADS 's2d' polynomial model, accurately fitted on C/I3 and P1dB measurements.

The circuit has been optimized over the entire operating frequency range of main amplifier (12÷16 GHz) for a relative bandwidth of around 28%. The first

step of optimization has considered the determination of value of the first loop phase shifter for maximum linear components suppression at test port output, in small signal condition. The optimizer has then been forced to reach the maximum improvement of C/I3 at a certain output power level, keeping fixed the first phase shifter previously determined and varying the second loop phase shifter and the output buffer gain. Also the fifth order products have been monitored in order to keep them as low as possible.

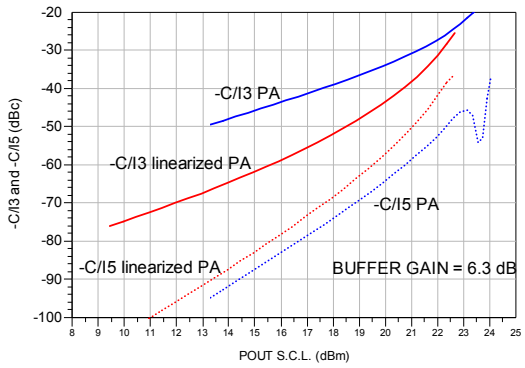

Fig. 2 C/I3 and C/I5 @ 13.9GHz

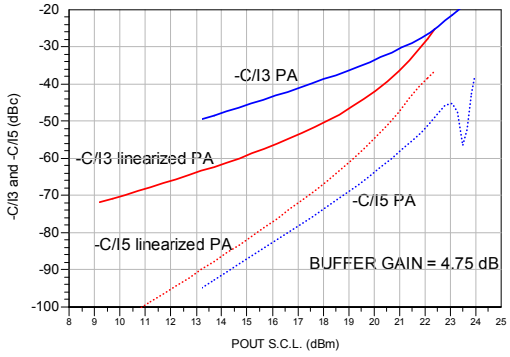

Fig. 3 C/I3 and C/I5 @ 16GHz

Fig.2 and fig.3 show, at 13.9GHz and 16GHz respectively, the third and fifth order C/I with a 2-tone input signal (the tones separation is 10MHz) as function of the single carrier output power level. Although the circuit has been optimized at the fixed power level of 17dBm S.C.L. with a C/I3 improvement greater than 10dBc, the effect of linearisation can be well appreciate over a very wide output power range.

A statistical analysis accomplished introducing the process dispersion data provided by the foundry is presented in fig.4. The Montecarlo simulation performed over 500 iterations shows a noticeable reduction of distortion even in extreme process parameters deviation from nominal case, which demonstrates that this active predistortion solution is well suited for monolithic applications.

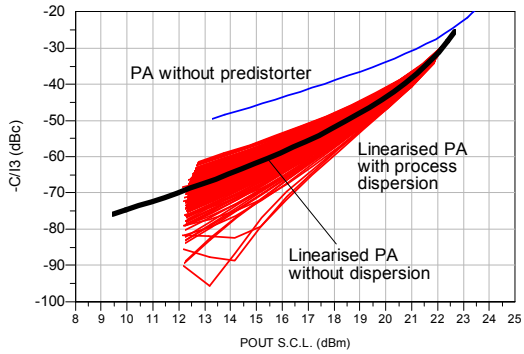

Fig. 4. Statistical dispersion of C/I3 @ 13.9GHz

Finally, the complete layout of predistorter is shown in fig.5. The output buffer has been implemented out of the chip.

V. Experimental results

The predistorter, the output buffer and the main amplifier chips manufactured in 0.25um pHemt on 100um GaAs technology, have been assembled and glued on a brass carrier and connected at RF through bonding wires. The main amplifier chip has been also used as output linear buffer. On the same carrier, the DC bias and control signal pads have been wired to an external connector. All the measurements have been performed into a 50Ω system. A photograph of the test bench is shown in fig.6.

The first phase of measurements was the tuning of loop 1 phase shifter in order to achieve maximum linear components suppression along non-linear path. This was achieved by means of S21 parameter characterization between "RF IN" (1) and "TEST OUT" (2) ports, as depicted in fig.1 and fig.5. The result of this measurement compared to the simulation data for 16GHz operating frequency is shown in fig.7.

Finally, fig. 8 reports the two tones response (C/I3) improvement at 16GHz respect to the performances of main amplifier without predistortion effect. The lineariser controls have been tuned for optimum performances in an output power range around 9dBm S.C.L. obtaining a third order intermodulation maximum improvement of 13dB. The effect of distortion reduction is much more appreciable if the tuning procedure is aimed to a specific single output power level. In this case third order products can be reduced up to 30dB for power level as high as 15dBm S.C.L.

These results show a general and fairly good agreement with the expected performances. However, the effectiveness of the predistorter is degraded as the power level is changed from the tuning value. This is probably due to the non-linear distortion effect introduced by the second loop phase shifter, which affects the performances of predistorter linear path. Therefore, this degradation effect can be drastically reduced moving the loop 2 phase shifter at the output of δ combiner where the power levels are much lower.

In conclusion, the experimental results confirm the validity of the predistortion approach and the effectiveness of the adopted implementation methodology.

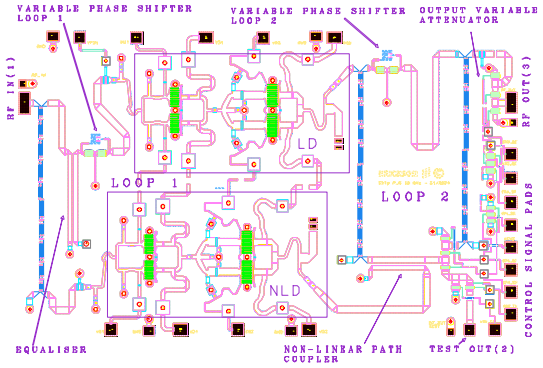

Fig. 5. ADS layout of the predistorter

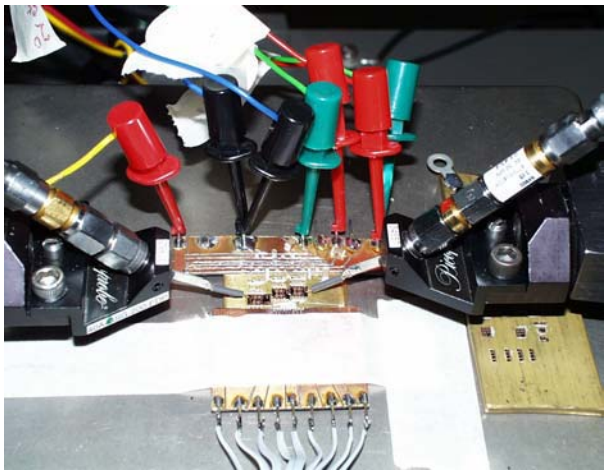

Fig. 6. Chip prototypes assembly into probe station

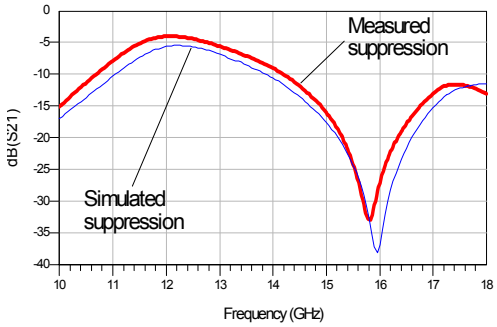

Fig. 7. Linear component suppression at TEST OUT port

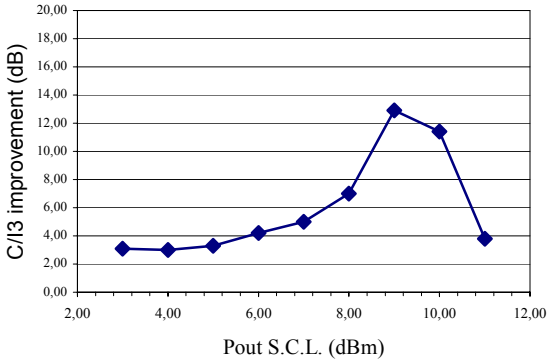

Fig. 8 C/I3 improvement due to predistorter as function of output power

VI. Conclusions

A complete MMIC implementation of a lineariser based on a new predistortion architecture has been presented. A very effective approach that takes into consideration a short time consuming design and issues related to model inaccuracies has been addressed. Simulation results based on real foundry components show a significant improvement in intermodulation performances of a power amplifier for the band 12÷16GHz (up to 10dBc of C/I3 over 28% of relative bandwidth), a true challenge for RF and microwave transmitter devoted to deal with very complex multilevel modulation schemes. These results are also confirmed by measurements on a prototype fabricated in GaAs technology, demonstrating the validity of the novel predistortion approach and implementation procedure.

Acknowledgements

The authors wish to acknowledge Gregorio Procopio and Giuseppe Sivverini for the assistance and support provided.

References

[1] P.Bianco, S. Donati Guerrieri, G. Ghione, M. Pirola, C.U.Naldi, C.Florian, G.Vannini, F.Filicori, L.Manfredi, “Optimum design of a new predistortion scheme for high linearity k-band MMIC power amplifier”, GAAS2001, London, September 2001.

[2] R.Iommi, G.Macchiarella, A.Meazza, M.Pagani, “A new active predistortion lineariser suitable for MMIC power amplifier”;GAAS2003, Munchen, October 2003.

[3] F.Palomba, M.Pagani, I.De Francesco, A.Meazza, A.Mornata, G.Procopio, G.Sivverini, “Process-Tolerant High Linearity MMIC Power Amplifiers”, GAAS2003, Munchen, October 2003.