F lip Chip Assembly of a 40-60 GHz GaAs Microstrip Amplifier

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ABSTRACT — **This paper describes the successful flip chip assembly of a broadband GaAs amplifier in microstrip design. The flip chip technology used was thermo compression (TC) flip chip bonding of the MMICs to gold ball bumps bonded on the thin film patterned alumina carrier.**
Also, we report on the occurrence of parasitic parallel plate (PPL) modes in the assemblies and we propose and investigate a scheme to eliminate the modes which, to the best our knowledge, have not been reported on before.
Finally we introduce our own flip chip transition equivalent circuit and we use this model in ADS to compare the simulated results with measurements. It is fair to say that the equivalent circuit models the flip chip transition well. This work was performed in the European MEDEA+ packaging project HIMICRO.

I. INTRODUCTION

Most reports on mm-wave GaAs flip chip refer to coplanar chip design. The coplanar MMIC design have many advantages over microstrip design such as cheaper processing due to no need of back side metallization, no need of via holes and thereby no call for wafer thinning. However, there are also drawbacks, e.g. the smaller number of foundries which have a coplanar MMIC process available. Other drawbacks are that the models for coplanar design are less developed and, in addition, there is a reluctance from microwave engineers to switch from microstrip to coplanar design.

One advantage of flip chip technology, when the frequencies reaches mm-wave, is the lower attenuation of the bump transition compared to a corresponding bond wire, [1]. In addition, it is normally not needed to compensate for the inductance as is usually the case for bond wire applications, [2]. The flip chip transition is also inherently wide band due to the small parasitics related to the bumps.

In this paper we present our work to find an appropriate way to flip chip assemble microstrip GaAs broadband amplifiers. Parasitic parallel plate modes are prone to occur in such assemblies as was previously reported in [3]. One approach to eliminate these modes is to add a resistive layer on the carrier under the chip surface. From our tests we have actually managed to sucessfully eliminate unwanted modes.

II. EM SIMULATIONS

To decide on different design parameters such as bump dimensions, pad design etc, EM simulations were performed with the 3D FDTD simulator Quickwave, [4]. The FDTD simulations in Quickwave were rather time consuming and in order to speed the design process we have developed an equivalent circuit based on the FDTD simulations. Fig. 1 shows the physical location of the elements of the equivalent circuit.

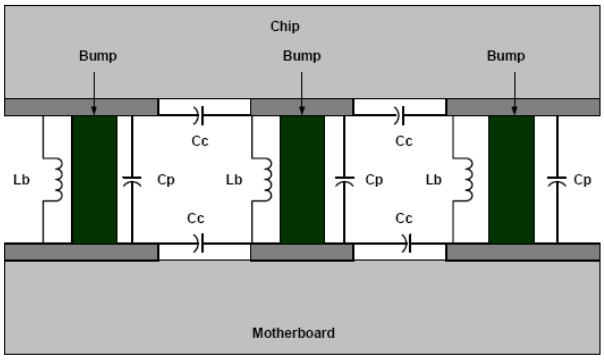

Fig.1. Location of inductances and capacitances in the bump section for a CPW-CPW transition.

Fig. 2 shows the equivalent circuit for the vertical transitions that was implemented in ADS.

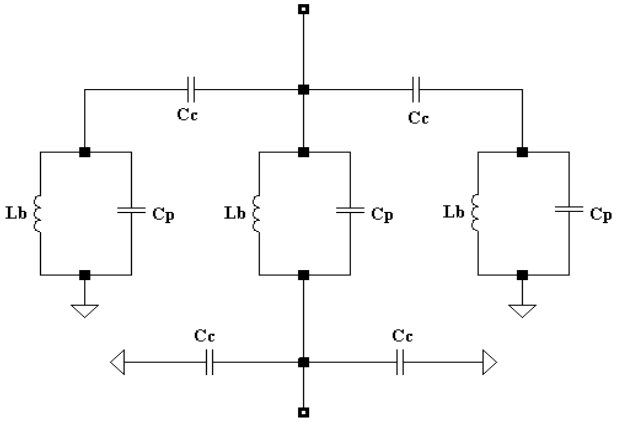

Fig. 2. Equivalent circuit for a bump section.

Each bump is represented by a parallel link of the capacitance C_p (capacitance between upper and lower bump pad) and inductance L_b (bump inductance). Capacitance C_p depends on the bump pad size (area of the bump pad outside the bump) and on the bump height. Inductance L_b depends on the bump height and bump diameter. The capacitance C_c represents capacitance between bump pads (i.e. between strip bump pad and ground bump pad), and depends on the bump pitch, bump pad size and bump pad shape. The ground on the

motherboard is the 'real' ground. The ground on the chip is not the same ground as on the motherboard – it is connected to the 'real' ground through the ground bumps (capacitance C_p and inductance L_b in parallel).

This model was later used in the simulations of the entire flip chip assembly.

III. Amplifier Design

The amplifier used in this test was designed in a commercial foundry process from OMMIC[1]. The gain of the amplifier is more than 6 dB from 40 to 60 GHz. The design was originally made as a subcircuit of a three-stage amplifier intended to be used in a 60 GHz wireless local area network (WLAN). The MMIC outline is shown in Fig. 3.

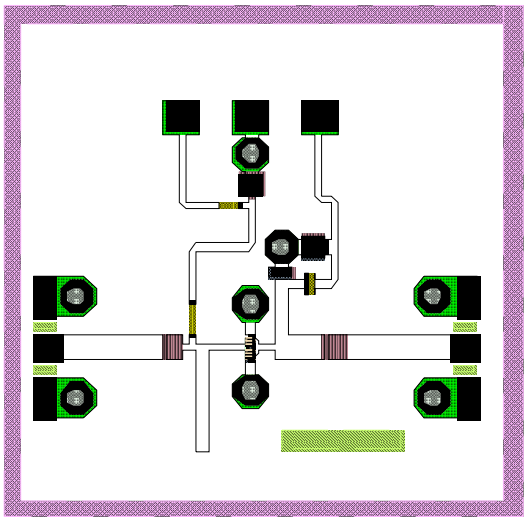

Fig. 3. One stage amplifier intended for 60 GHz WLAN

IV. Carrier Design

Three different carriers were designed in 254 µm thick alumina with etched gold pattern, Fig. 4. The carriers have coplanar transmission lines of 50 Ω impedance with a line width of 70 µm and 40 µm gaps. The total length of the carriers is 4.8 mm. The designs are referred to as AMP_bias, which is the coplanar carrier design with thin film alumina facing the chip and AMP_G, which is essentially the same design but with the ground plane extending over the whole free surface. The third design referred to as AMP_G_R has an extended ground plane and a 50 Ω/□ resistive layer underneath all metallization. After etching, the resistive layer remains in the area matching the chip. This resistive layer is facing the chip surface when the chip is flip chip assembled on this carrier. The three carriers have no back side metallization.

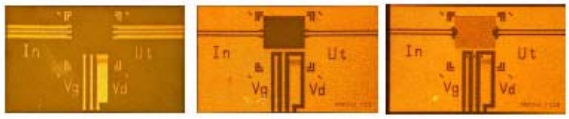

Fig. 4. Carrier design from left to right:
AMP_bias AMP_G AMP_G_R.

[1] Process D01PH from OMMIC, Limeil-Brevannes, France.

V. Test Assemblies

To enable flip chip assembly, balls were bumped on the thin film carrier in a regular ball bonder using a 25µm of AuPd1% wire. The bumps have a diameter (d) of 80µm, a height (h) of 40µm and a total height (H) of 80µm, Fig. 5.

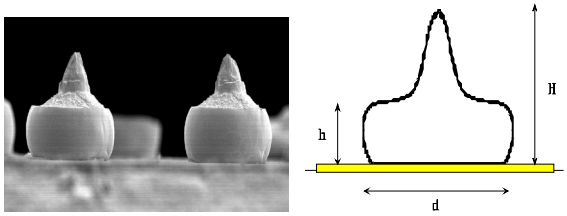

Fig. 5. Bump geometry made using 25µm gold/palladium wire.

The thermo compression flip chip bonding was made using flip chip bonder Fineplacer PICO. No coining of the bumps was done before FC bonding. The chip was heated to 210°C, the carrier was heated to 310°C, the applied force was 25 grams per bump and the bond time was 15 seconds.

VI. Measurements After Assembly

Two sets of each design was mounted and measured in the same setup. The chip was also measured in a standard probe set-up. The bias condition was equal in all cases, i.e.: V_d=3.0V, V_g=0V. The 1.5 mm long transmission lines, before and after the chip, adds approximately 0.5 dB extra loss. This has not been taken into account when comparing the results from the assemblies with the on-chip measurement in Fig. 6.

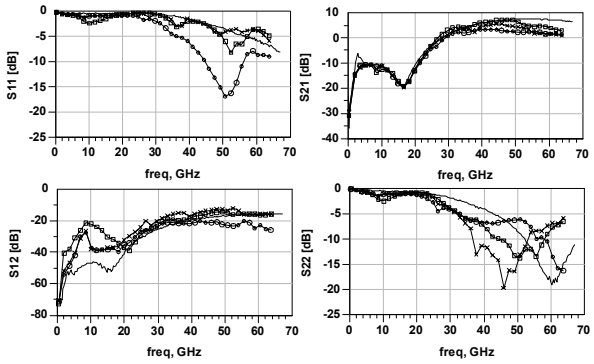

Fig. 6. Measured response of amplifier flip chip assemblies: squares correspond to AMP_bias, crosses to AMP_G and circles to AMP_G_R. The solid line represents the on-chip measurement.

Comparing these results with the on-chip measurements (solid line) we see that the assembly with the AMP_bias carrier (squares) gives an S_{21} as good as the on-chip measurement up to 50 GHz where the gain drops off.

The assembly with the extended ground plane (crosses) show evenly separated glitches in all four directions (S_{11}, S_{21}, S_{12} and S_{22}), probably giving evidence of some parasitic mode influence. The role of the ground plane width has been investigated and explained by [5] and [6]. In addition, the gain is lower in this assembly, which may be due to loss of power into parasitic modes.

The third design (circles) with the resistive layer added to the carrier shows that the parasitic modes are now eliminated. Unfortunately, the price for adding the resistive layer is a 2 to 3 dB extra loss.

An increased feedback, S12, can be noticed up to 20 GHz for all assemblies, especially is the AMP_bias case.

VII. Simulation With ADS Model

We have also simulated the performance of the flip-chipped amplifier in ADS. In this case study we compare the measured result of the chip assembled on the AMP_bias carrier to simluated data. The simulations were performed by measuring the amplifier separately and inserting the results into ADS as a module. The transmission lines on the carrier are momentum simulated since the standard coplanar lines used in ADS does not allow for a narrow width of the ground traces as is the case in our design. The bumps are modeled by the equivalent circuit as it is described in part II. The ADS schematic is shown in Fig. 7.

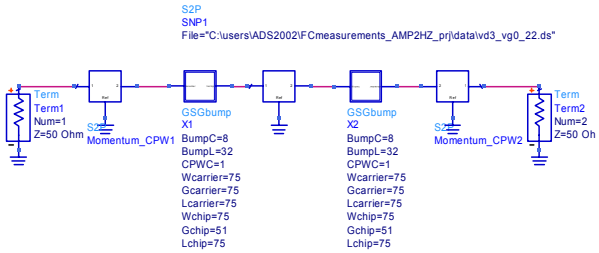

Fig. 7. The full amplifier flip chip assembly simulated with on chip measured data, ADS model for bumps and momentum simulated coplanar transmission lines.

In this simulation the width and length of the signal pads on the chip is 75 µm and the distance from the signal pads to the ground pads is 51 µm, Fig 8. These numbers gives us the input data referred to as Wchip, Lchip and Gchip in the bump equivalent circuit.

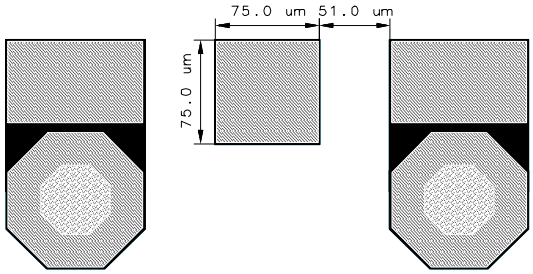

Fig. 8. Pad dimensions on the amplifier chip.

On the carrier the ground and signal pads are the same size, i.e. width, length and gap are 75µm and thus all three parameters Wcarrier, Lcarrier and Ccarrier are set to 75µm. The value to enter for the variables bump capacitance (BumpC) and Bump inductance (BumpL) comes from the size of the bump and has previously been decided on when working with this model.

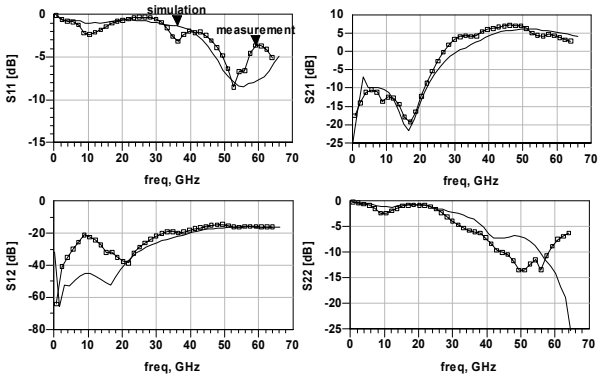

Fig. 9. Comparison between simulation of assembly (solid line) and measured data of the amplifier assembled on the AMP_bias carrier (squares).

In Fig. 9 we can see that the simulated and measured data resemble each other quite well. In the forward transmission case, S_{21}, the curves matches almost exactly in the whole frequency range. The match of the return loss S_{11} is also very good, only some ripple from measurement is not accounted for. In backward transmission the feedback at lower frequencies does not show in simulation and this is natural since the model does not take this into consideration.

It is also worth to notice that since the amplifier chip is a microstrip design the proximity effect should be taken into account since a part of the electromagnetic field extends from the chip surface into the carrier. Thus the characteristic impedance of the microstrip is slightly altered. This was not included in the simulation.

VIII. Conclusion

We have succeeded to flip chip mount GaAs microstrip amplifiers on alumina carriers with thermo compression bonding technology. Measurements show that gain was not deteriorated up to 50 GHz.

The parasitic parallel plate modes came with the extended ground plane and were eliminated with the resistive layer on the carrier. However, this extra resistive layer resulted in a 2 to 3 dB penalty on the gain curve.

The developed equivalent model for the CPW-CPW vertical transition shows good agreement with the measurements.

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