A Low Voltage 12-GHz Silicon-Germanium Static Frequency Divider with a Selectable Division Ratio

L.Masini, A.Golfarelli*, M.Pozzoni**

Laboratori Fondazione Guglielmo Marconi, Via Porrettana 123 - I 40044- Pontecchio Marconi - Bologna, leonardo.masini@labs.it

* Laboratori Fondazione Guglielmo Marconi, Via Porrettana 123 - I 40044- Pontecchio Marconi - Bologna, alessandro.golfarelli@labs.it

** STmicroelectronics, Via Tolomeo 1 – I 20010- Cornaredo –Milano, massimo.pozzoni@st.com

An integrated 12-GHz static frequency divider with a selectable division ratio (16/1, 64/1) realised in a Silicon Germanium technology dedicated for high volume production, is presented. It operates at low bias voltage (2.7-3.6V) providing balanced output signals on 50-ohm loads. The chosen architecture, the adopted design approach and used technology led to a good trade-off among maximum input frequency, input sensitivity, noise floor, power consumption, division ratioes and die size compared with the current high frequency dividers. The circuit features make itself a versatile block for high frequency PLL systems, while the circuit core can be used as a macrocell for the design of totally integrated fast PLL's.

1. Introduction

The fast-growing needs of high-speed high-complex communication systems requested by multimedia services lead to the design and fabrication of ever-increasing complexity and performing electronics. Keeping a high reliability, a great interest is in the integration of many digital and RF functions on the same chip for 10Gb/s fiber optics, satellite receivers, new Microwave Pt-Pt connections and measurement equipment.

High Speed frequency dividers, as well as VCO's, are two of the most important building blocks in the high frequency wide-band wireless and wireline electronic systems. Recently, several static divider prototypes have been proposed both in Si and GaAs technology with different architectures [1], [2], [3]. In the following we present the low voltage static divider operating at low voltage bias supply with two selectable division ratios (16/1 or 64/1).

2. Technology

The 12-GHz divider is designed with the BiCMOS7G Silicon Germanium technology. The BiCMOS7G is a 0.25um SiGe HBT/CMOS from STmicroelectronics, suitable for system-on-chip applications. Together with SiGe HBT transistor (h_{FE}=100; BV_{CE0}=2.6V; V_{EA}>50V; f_T>65GHz) the process provides designers NPN BJT's with five metal layers, MIM capacitors and high resistive poly.

3. Circuit Design

The 16/1-64/1 Divider consists of I/O amplifiers, Asynchronous, Synchronous and Mux stages (Fig.1).

A full Synchronous divider reduces the noise floor and increases the current consumption. On the other hand, a complete Asyncronous solution degrades the noise lowering the power consumption. Thus the divider architecture includes an Async 8/1 division followed by the Sync. The Async stage allows a high frequency division with low power consumption. The Sync section follows the Async to improve the noise floor (Fig.2). The I/O Amplifiers provides on chip 50-ohm matching while the Mux section includes the output selection circuitry.

The Async stage comprises a series of three MS-FF (Master-Slave Flip-Flop) (Fig.3). In order to achieve high speeds at low bias voltage, the MS-FF is designed with two Latch series connected without the common adoption of feedback emitter followers (Figg.4 and 5). This choice also reduces the risk of on-chip ringing oscillations caused by Emitter Followers which can affect the eye diagram. With the fulfilment of the maximum current constraint for MTTF, the size and current of each

transistor are optimised to reduce the propagation delay time. Moreover, in the upper level current switches, the transistors are reduced to minimise the parasitic capacitance without degrading the cut off frequency (f_T). A 400mVpp differential internal voltage swing has been guaranteed.

Fig.6 shows the Sync section with its basic blocks (MS-FF, T-FF, AND). The T-FF's include EXOR and MS-FF circuits (fig.7). The EXOR circuit is shown in Fig.8.

To enhance the sensitivity of the Divider a wide-band amplifier has been designed and inserted at the input. Emitter feedback resistors are used to enlarge the bandwidth and to control the gain (Fig.9).

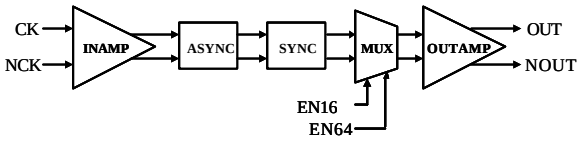

Figure 1- Block Scheme of the Divider

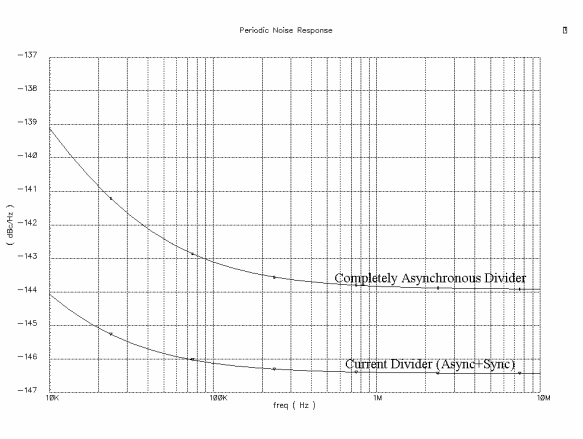

Figure 2- Simulated Noise of the complete Async Divider and the current solution both designed with same SiGe technology

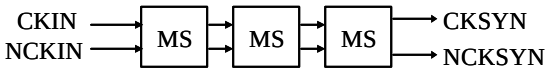

Figure 3- Block Scheme of the Async. Section

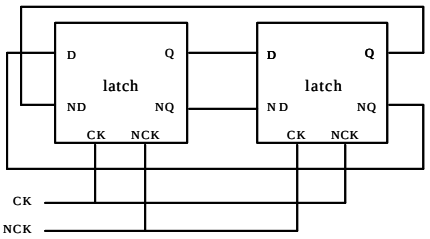

Figure 4- MS-FF

In order to reduce signal distorsion resulting from multiple reflections, on chip 50-ohm matching is adopted. In particular 50-ohm resitors are connected between the base and VCC of the input emitter follower.

The output stage comprises buffers and MUX to enable the divided by 16 or by 64 output signal (fig.10). The OutAmp provides good output return loss (VSWR<1.8:1) to reduce the time jitter induced by the impedance mismatching. The Output amplitude divided signal is 200mV peak to peak on 50-ohm load.

The on-chip RF signal and bias lines were modelled through the connection of RLC basic cells. While the capacitance value was extracted with the DIVA tool, the conductor line inductance was calculated by means of analytical formula [4]. On the other hand frequency dependent conductor series resistance was computed taking into account the skin effect.

Let t the conductor thickness, the skin effect appears at frequencies where the skin depth $d < t/3$.

$$d=1/(\pi \mu \sigma f)^{1/2}$$

where μ, σ and f are respectively the metal permeability, the metal conductivity and the operating frequency. Thus the conductor resistance per unit length r can be approximated as follow

$$r=\{(1/\sigma W t)^2+[k/(2\sigma d(W+t))]^2\}^{1/2}$$

Even if k depends on the shape of the structure and then on the field distribution, in this work it was set to 1.

Particular care has been devoted to the design of the layout drawn with the aim of reducing crosstalk and parasitics. As a direct consequence an optimal partitioning was achieved among Async, Sync and I/O blocks to reduce the influence of on-chip connection lines and unwanted resonances. Critical lines were shortened as much as possible to lower their related inductance thus preventing ringing and undumped oscillations (5).

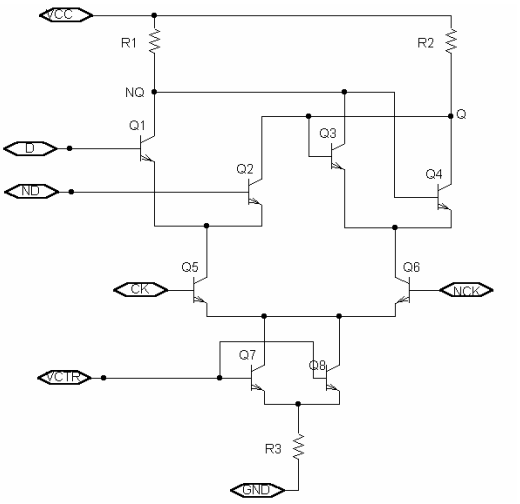

Figure 5- Latch Electrical Scheme

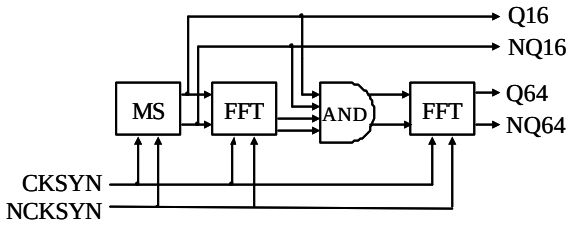

Figure 6- Block Scheme of the Sync. Section

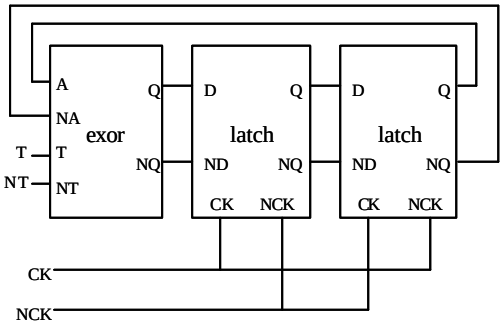

Figure 7- T-FF

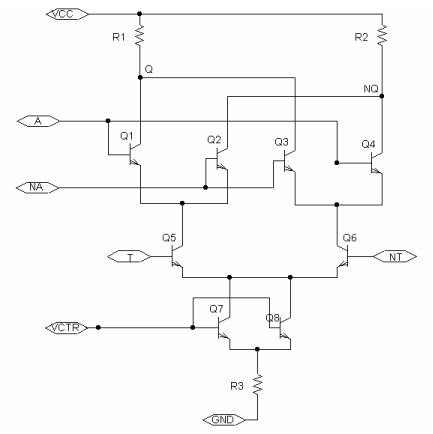

Figure 8-EXOR Electrical Scheme

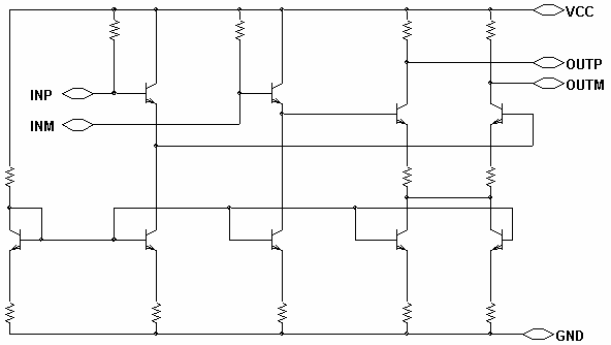

Figure 9-INAMP Electrical Scheme

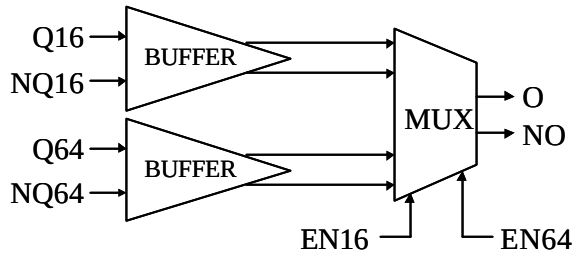

Figure 10- Block diagram of the Mux Section

4. Experimental results.

Naked chips of the Divider were mounted on the AR1000 substrate (Fig.11). External components such as resistor capacitors and Dip Switches were placed on the boards both to clean DC lines from the noise of bias power suppliers and to feed EN16 and EN64 pins.

The Divider operates in the 2.7-3.6V voltage range with the input signal from DC to 12.3GHz and a total current consumption of 60mA (37mA from Async + Sync and 23mA from I/O Buffers). The 16/1 or 64/1 ratio is selectable and available at the output. The die size is 1.3 mm x1.3 mm (Fig.12)

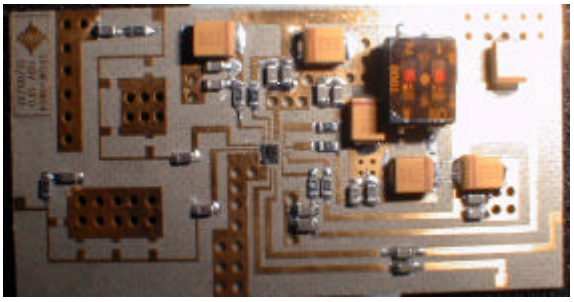

Figure 11- Divider chip mounted on the Evaluation Board

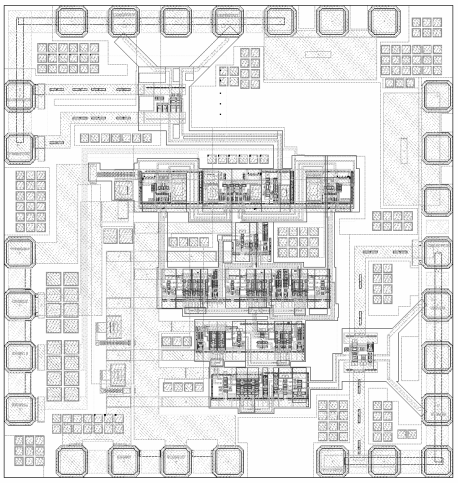

Figure 12- Layout

Figures 13 and 14 show respectively the input sensitivity and the complementary outputs of 64/1 port. In particular Fig.14 plots the oscilloscope results when the input frequency signal of divider is 10.3 GHz. The Divider works properly in the temperature range -20°C to 110°C and can also operate in single ended mode.

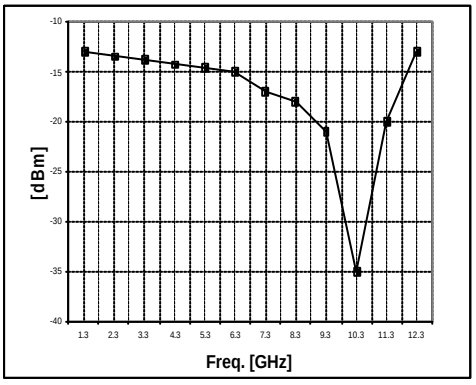

Figure 13-Measured Input Sensitivity

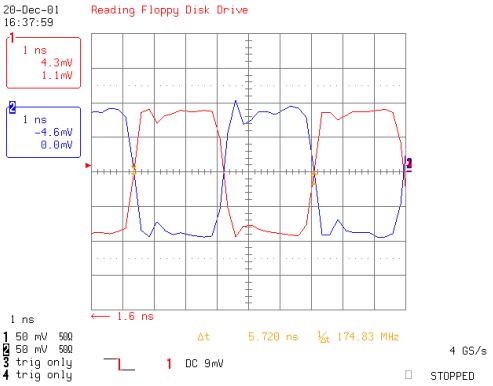

Figure 14-Output Waveforms of the 10.3GHz input signal divided by 64

5. Conclusion

A low power 12-GHz Static frequency divider with selectable division ratio (16/1 64/1) was designed and fabricated in a SiGe technology intended for high volume production. The chosen architecture, the adopted design approach and the technology capabilities led to a good trade-off among maximum input frequency, input sensitivity, noise floor, power consumption, division ratioes and die size compared with the current available high frequency dividers.

6. References

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(2) Z.Lao, W.Bronner, A.Thiede, M.Schlechtweg, Ahusulmann, M.R.Motzer, G.Kaufel, B.Raynor and M.Sedler, “35-GHz Static and 48-GHz Dynamic Frequency Divider IC’s Using 0.2-um AlGaAs/GaAs-HEMT’s ”, IEEE JSSC, Vol.32 No.10, Oct..1997, pp. 1556-1562.

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(5) E.M.Cherry and D.E. Hooper, “The Design of Wide Band transistor feedback amplifiers ”, Inst. Elect. Eng Proc, Vol.110 N.2, Feb.1963.