High f_T 30nm $In_{0.7}GaAs$ HEMT's Beyond Lithography Limitations

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Abstract

Two types of 30nm $In_{0.7}GaAs$ HEMT has been successfully fabricated, using SiO_2/SiN_x sidewall process and BCB planarization, and ZEP flowing and sloped etching technique. The sidewall gate process was used to obtain more fine line in one type of device, which enabled to lessen the initial line length to half by this process, and to fill the schottky gate effectively in a narrow gate line, the sputtered tungsten (W) metal was utilized instead of evaporation method. To reduce the parasitic capacitance through dielectric layers and gate metal resistance, the etch-backed BCB was used for the assisting layer of gate top head. The other 30nm device could be fabricated with inverted double-exposure & double-develop method when initial defined 100nm could be reduced to 30nm by using ZEP flowing and sloped etching. The fabricated two 30nm $In_{0.7}GaAs$ HEMT's showed similar characteristics such as f_T above 400GHz. We believe that the developed technology will be directly applicable to an InGaAs nano-HEMT with finer gate length if the initial line length will be reduced below 60nm range.

I. INTRODUCTION

InGaAs/InAlAs HEMT on InP substrate has shown the excellent frequency characteristics due to the enhanced electron mobility and the increased conduction band discontinuity (ΔE_c) [1-2]. Recently, the device microwave characteristics have been improved by reducing the gate length (L_g) to nano-meter scale and adopting the highly strained In_xGaAs channel (x>0.53) [3]. According to the Fujitzu group's work, f_T of 562GHz for the strained $In_{0.7}GaAs$ channel HEMT with L_g of 25nm was reported [3].

In this work, nano-patterning technique was developed in order to overcome the lithography limitation. Through the sidewall process, ZEP flowing and sloped etching technique, initially defined line length could be lessened to 30nm [4]. To fill the schottky gate metal effectively in narrow line opening with high aspect ratio above 3 for sidewall gate device, the sputtered tungsten (W) was used instead of conventional E-beam evaporated metal. With the developed processes, two 30nm $In_{0.7}GaAs$ HEMTs was successfully characterized.

II. 30nm Gate Process Beyond Lithography Limitation

The conventional e-beam lithography equipment with an acceleration voltage of 30 kV and a Tungsten (W) or LaB_6 filament would offer a minimum feature scale of about 100nm. To reduce the device gate length (L_g) to the sub-100nm scale, the state-of-the-art e-beam lithography equipment with high resolution will be needed. The side-wall process has been widely used to overcome these lithography limitations, particularly in CMOS device fabrications [4].

Previously we proposed a damage-free and highly reproducible sidewall gate process [5]. Through dielectric re-deposition and dielectric etch-back, the final gate length (L_g) could be lessened by the dimension of the two side-wall spacers [5]. The obtained final gate length after the dielectric etch-back was 30nm. The procedure for the

fabrication of triple shaped gate structure is shown in **fig. 1** and **2**. After the tungsten sputtering in the sidewall gate, 2nd gate metal (Ti/Au) with 100nm thickness was evaporated and lifted off, and then unnecessary tungsten was removed by RIE. Finally, planarization using BCB dielectric with low dielectric constant (ε_r) of 2.8 was carried out and 3rd gate metal (Ti/Au) with 600nm thickness was evaporated and lifted off. **Figure 3** shows the SEM photographs of the fabricated 30nm triple shaped gate structures.

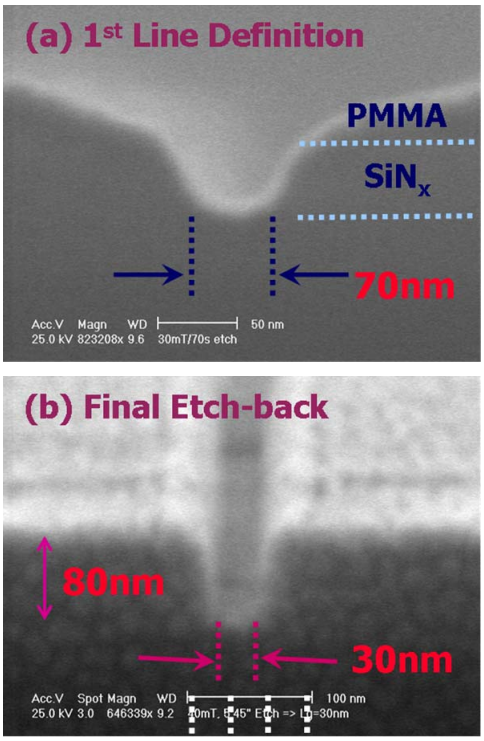

Fig. 1 SEM Images for 30nm Sidewall Process

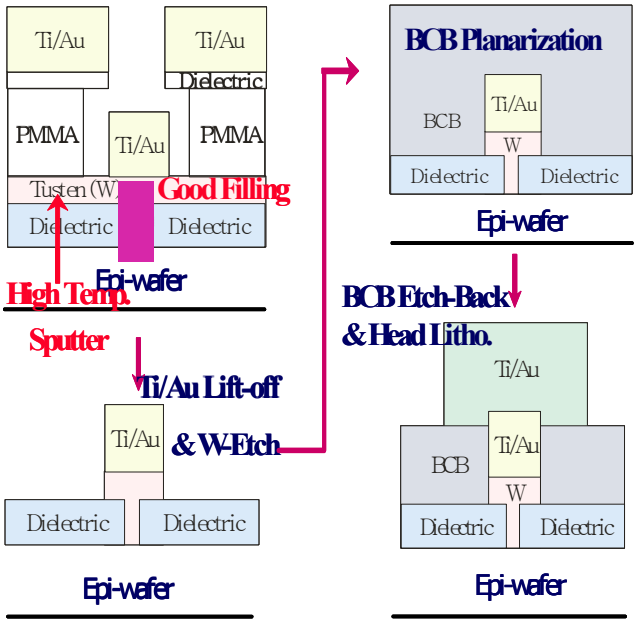

Fig. 2 Procedures for BCB assisted Triple-Gate Tech.

Figure 4 and **5** shows the SEM images of pattern transfer profile after ZEP flowing and sloped etching using RIE lag effect. The initial line of 100nm could be reduced to 30nm by using the above two techniques such as ZEP flowing and sloped-RIE etching. On top of the obtained line, bi-layers of PMMA and Copolymer were used to define 0.3μm wide gate head, which could be called as inverted double-exposure & double-develop method. The procedures for obtaining 30nm T-shaped gate were also described in **fig. 5**.

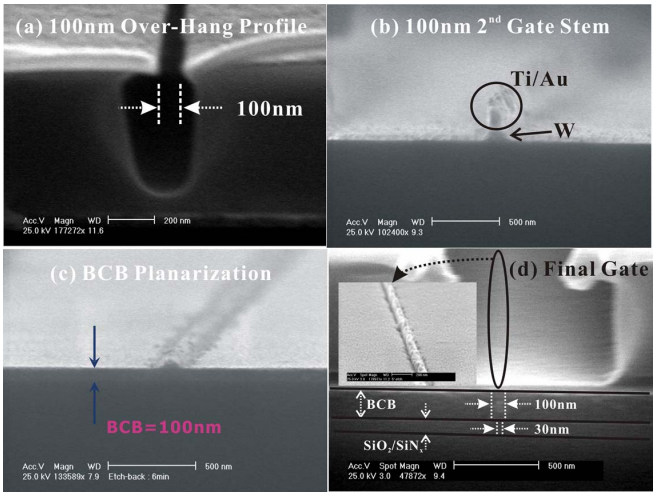

Fig. 3 SEM Images for Triple-Gate Process

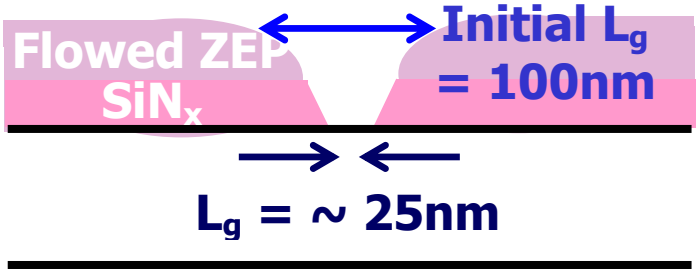

Fig. 4 L_g Reduction by Flowing & Slope-Etch Tech.

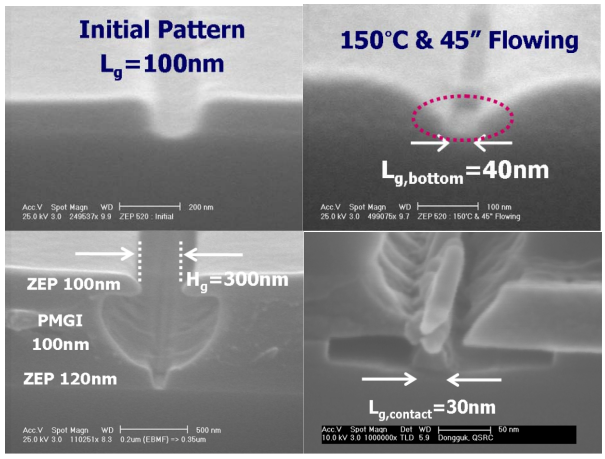

Fig. 5 SEM Images for 30nm T-Gate Process

III. Characterization of 30nm $In_{0.7}GaAs$ HEMTs

Pseudomorphic InGaAs/InAlAs HEMT epitaxial layer was grown by a solid-source molecular beam epitaxy (MBE) on a 3 inch semi-insulating InP substrate. Strained 8nm $In_{0.7}GaAs$ channel was adopted to enhance the carrier transport properties, as shown in **fig. 6**. The hall measurement results indicated a 2-DEG density of $3\times10^{12}/cm^2$ with a low field Hall mobility of $10{,}300cm^2$/V-sec at 300K. Device fabrication begins with mesa isolation down to the InAlAs buffer layer by wet chemical etching. For Source/Drain (S/D) ohmic contact, Ni/Ge/Au(10/45/120nm) was evaporated, lifted off and alloyed at 320°C in H_2 ambient. The measured ohmic contact resistance was as small as 0.035Ω-mm, which is acceptable for sub-50nm gate device. The developed nano-patterning methods were applied to form 30nm gate opening, in which selective gate recess with S-A was done.

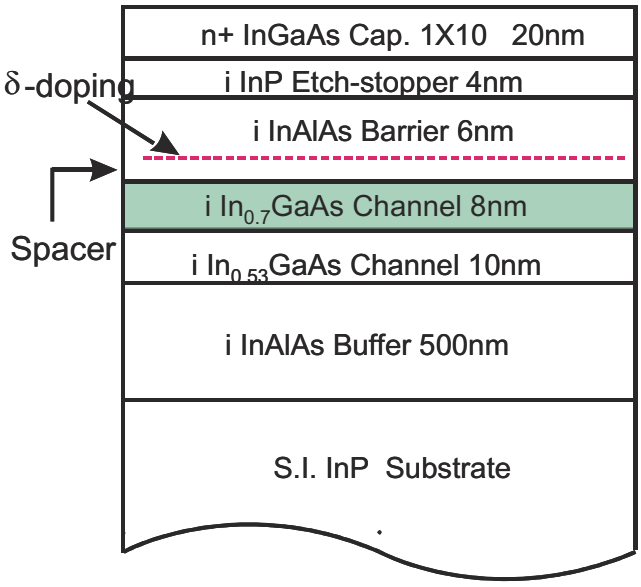

Fig. 6 Epi-Structure for InGaAs/InAlAs HEMT

The fabricated devices were characterized through on-wafer measurements for DC and microwave performance analysis. The output I-V transfer curves were plotted in **fig. 7**. The device was found to have V_{th} of -0.3V, I_{dss} of 180mA/mm, $G_{m,max}$ of 1.3S/mm and BV_{gd} of -4V. Up to the drain bias (V_{ds}) of 1.3V, the device has showed little short channel effects such as the abnormal increase of G_o and the shift of V_{th} with drain bias. The small-signal S-parameters for 2x50μm device were measured using on-wafer probing and network analyzer (1~40GHz). Shown in **fig. 8** and **9** were the plots of H_{21} versus the frequency for the device biased near peak $G_{m,max}$ region. Extrapolating H_{21} to zero gain with -6dB/octave slope, the estimation above 400GHz was made for f_T. We believe that these results demonstrated the excellent sub-50nm InGaAs HEMT with a little short channel effect.

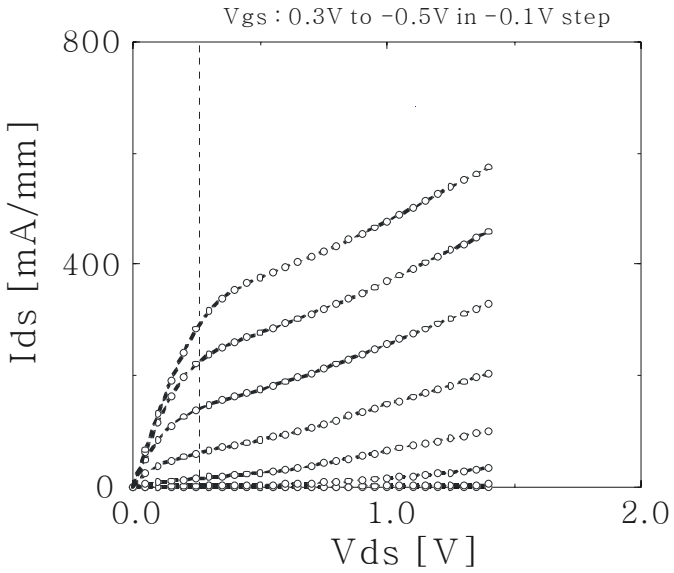

Fig. 7 DC characteristics of 30nm HEMT's

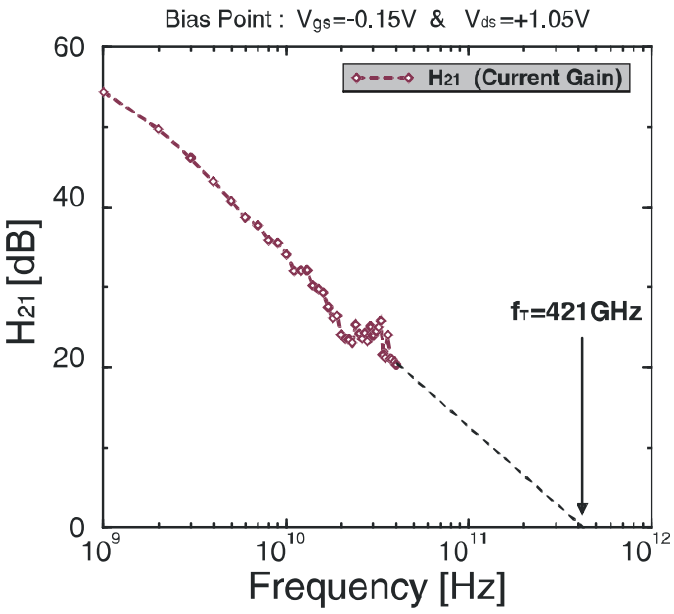

Fig. 8 RF Performance for 30nm Triple-gate HEMT

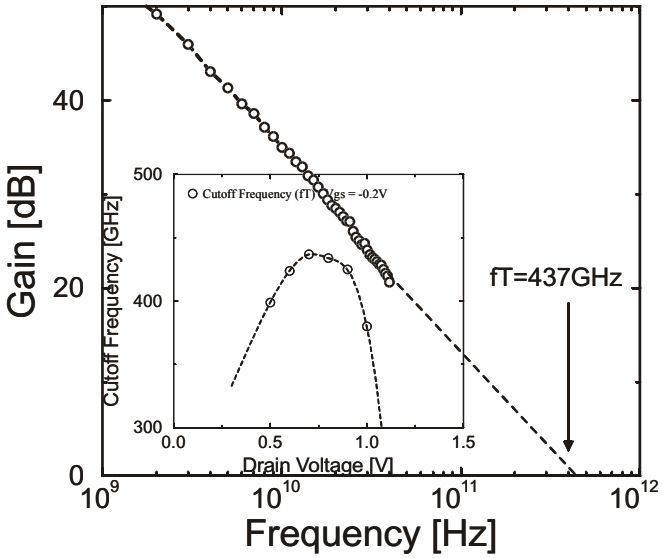

Fig. 9 RF Performance for 30nm T-gate HEMT

IV. CONCLUSION

We have fabricated two types of 30nm $In_{0.7}GaAs$ HEMTs with triple shaped gate metal using sidewall process and BCB planarization, and with T-shaped gate using ZEP flowing and sloped etching technique. Fine lines such as 30nm could be obtained by dual SiO_2/SiN_x sidewall process and the triple shaped gate metal process assisted by BCB layer did provide the metal structure stability and small parasitics. The developed process was applied to fabricate 30nn InGaAs HEMT's, which led to $G_{m,max}$ of 1.3S/mm and f_T above 400GHz.

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