Indium Phosphide MMIC Low Noise Amplifier and related cryogenically applications in a Radioastronomical Focal Plane Array Receiver

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***Abstract* — We will present realisations of MMIC Low Noise amplifiers designed to operate in a cryogenic environment, working from 18 to 26 GHz. These devices have been produced with the intent to be installed in a five beams feed array receiver, realised to improve the single dish survey and VLBI performances of the 32m diameter parabolic dish antenna of the Medicina Radioastronomical Station, near Bologna, in Italy. The entire project named FARADAY has been developed in the FP-5 context supported by EU. Many efforts has been concentrated to produce devices with the best compromise between lowest noise, flat gain, and good input matching. For this device, MMIC 0,1 um gate length InP HEMT process has been used. We will start the work description from the design specification to the on wafer devices measurements. We will also introduce our packaging material investigations in order to have a reliable working device at cryogenic temperature. Packaging device efforts has been devoted also to realise a modular carrier that let the choice between coaxial and waveguide interface.**

I. INTRODUCTION

Obtained successes by Weinreb [2], Gough [3], and Galliego [4] have validated InP technology for Ultra low noise Radioastronomical cryogenical applications. This peculiarity is more obvious to growing of the frequency. Best Low Noise performance are obtained with MIC approach where it is possible to join the low characteristic noise of the InP with selected low loss passive components and dielectric. Limit of this approach for large scale production is in the high number of manual operations on RF path that can be traduced in high cost and long production time. MMIC approach gives high performance devices, reducing the manual operation number on the RF path, allowing performance uniformity, lower cost on mass production and short production time. FARADAY consortium [1], leaded by Jodrell Bank Observatory (JBO) and composed by ASTRON (NL) INAF-IRA (I), TcfA (PL) had the opportunity, thanks to CSIRO-ATNF (AU) to approach TRW- Velocium InP MMIC HEMT 0,1 um Foundry Process

II. AMPLIFIERS SPECIFICATIONS

Designer driver idea for the Low Noise Amplifiers (LNA) was focused to obtain the lowest noise performances available with the selected technological process, taking into account a reasonable input and output return loss. This because this amplifiers has been designed to be placed in a receiver for radioastronomical applications with the aim to operate polarimetric science. This means that we need an Orthomode transducer (OMT) at the foci of the receiver feed system in order to obtain two polarizations. Performances of this device strongly depend on the return loss of what will be connected to and receiver configuration channel don't consider to use isolator between feed system and LNA to increase the match . Table I report a schematic view of the LNA's specifications. Because the receiver channels specifications are 40 dB of total gain before the first conversion section, another class of amplifier has been designed in order to obtain the desiderated performances (Table II)

Gain	26±1.5 dB
Input Return Loss	< -15 dB
Noise Temp.	Best effort
Working Temp.	20 °K

Table I

Gain	15±1.5 dB
Input Return Loss	Primary constraint
Noise Temp.	Moderately Low
Working Temp.	20 °K

Table II

III. AMPLIFIER DESIGN DESCRIPTION

MMIC InP HEMT 0.1µm gate length process has been provided by TRW-Velocium. Active device used are 4-fingers HEMT, gate width is 120 µm (4x30). Cryogenic devices and passive component models weren't available then we assumed to design at room temperature and subsequently tune the device for cryogenic operations. For this reason each gate is separately biased. Power supply designed for this application tune the gate voltage automatically in order to keep fixed the desiderated drain current. The chip size dimensions are 3.2 x 2.25 mm. Due to the gain growing at low temperature, stability and RF isolation bias paths are also carefully investigated. Stability approach has been conservative: every single stage has been designed to be unconditionally stable, following the indications given by K and B1 parameters [5]. The S-probe stability check method has been tested for future applications: this method let the designer to probe the stability in every internal section of the amplifier [6]. In order to reduce coupling effect of microstrip elements, we have considered as general design rule, where applicable, twice the substrate thickness as minimum distance between two microstrip element. Every critical part of microstrip circuit has also been electromagnetically simulated with EMSight®, the Microwave Office® EM-simulator, powered by AWR™, and the results have been compared with circuital simulation: only minor effect has been noted. Moreover an off-chip matching network has been designed to prevent possible low frequency oscillation that could be primed through unwanted positive feedback path along the bias line.

A. Low Noise Amplifier

A 3-stage cascaded low noise amplifier layout is shown in Fig.1: All matching circuits, except the first one, have been designed using distribute element like microstrip line (line-step-line matching method). A one-turn spiral inductor has been used in the first matching circuit as tradeoff between dimension constraints and the optimum noise matching point. This amplifier has been designed as a front-end element, the first active device encountered by the received signal. Two different version of this amplifier has been designed in order to test a different grade of on-chip DC isolation.

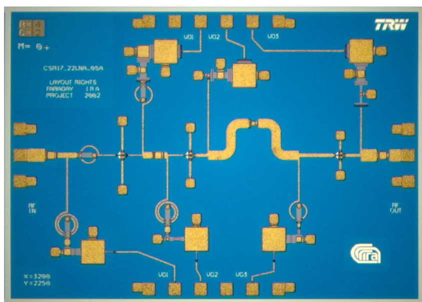

Figure 1

B. Back off Amplifier

The layout of 2-stage cascade back off amplifier is shown in Fig.2: Matching circuit has been designed to achieve high return loss performances over the entire 18 to 26 GHz bandwidth. DC bias line has been designed to stabilize the device over the working bandwidth with a low DC power consumption.

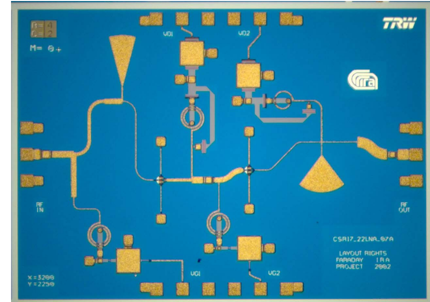

Figure 2

IV. SIMULATED RESULTS AND ON WAFER MEASUREMENTS

An intensive on-wafer measurement session has been performed in order to characterize these amplifiers. Five wafers have been measured for a total of 400 devices tested. In this paper we are describing just two of four different design that has been placed from IRA on this wafer run. From TRW PCB validation measurements results a higher transconductance $\mathbf{g_m}$ value than expected.

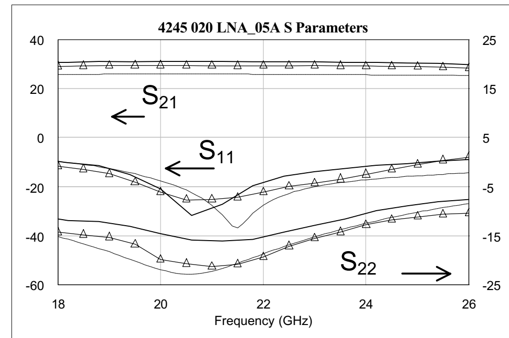

Figure 3

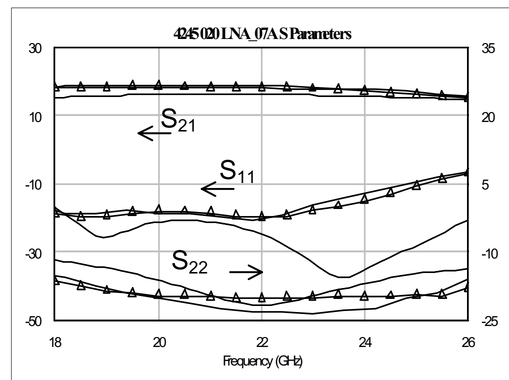

Figure 4

It means much more gain of what we expect. Figures 3 and 4 shows S-parameter measurement results of two different amplifiers named respectively 22LNA_05A and 22LNA_07A. These are related to 1 of 5 wafers tested. Discontinued line represents simulated results and marked line are related to packaged devices. Continue line represent a typical device response. Efforts devoted on MMICs design could be useless if the MMIC interfaces increase the losses, degrade noise performance and mismatch the device. Shaped microstrip have been used in order to compensate wire bonds drawbacks (Fig. 7). It is remarkable the narrow device performances spread that is less than 1dB@±2σ (σ is the standard deviation in the Gaussian distribution analytical expression).

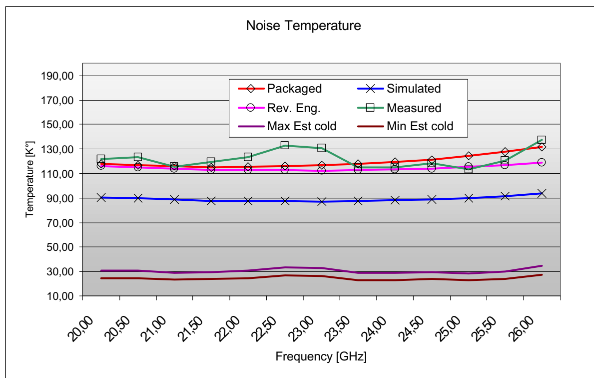

Figure 5

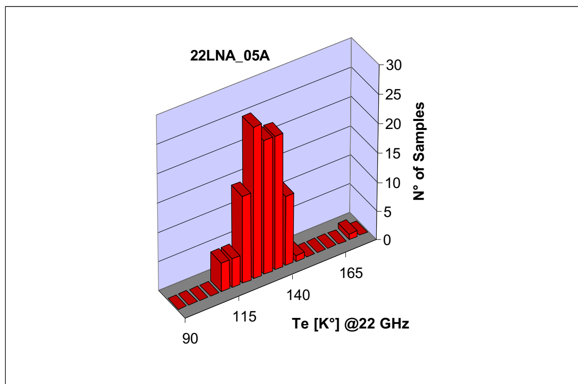

Figure 6

Fig.5 show noise results related to a 22LNA_05A. Cross Marked line represent simulated result. Square marked like represent a typical device. Quick reverse engineering process that helps to estimate the real device performances is represented with circle marked line. Diamond marked line take care also of packaging effect. Preliminary cold measurement reduce the noise contribution between the two unmarked line (20-30K°). Also in this case the devices performance spread result narrow **(14°K @ ±2 σ)** with only 11 over 100 samples exceed T_e^{AVG} + 2σ. In Fig.6 is represented the wafer statistical distribution of T_e @ 22 Ghz normalized at 290°K. Another important result obtained is the relevant number of working chip outcoming from this wafer run. Less than 8% resulted broken or not compliant with the specifications. The gap from measured and simulated result could be attributed to a non modeled substrate and passive components losses and on non sufficient accuracy of the noise measurement workbench. Actually industry standard accuracy allows noise measurement with uncertainty of **± 0.2 dB.** We are working to apply a very rigorous testing method with uncertainty of **±0.06 dB** to verify if differences could be related to measurement precision [7]. Ripple in measurements are related to a non-optimum noise source matching. Also in this case we are planning to use some strategy to reduce this effect.

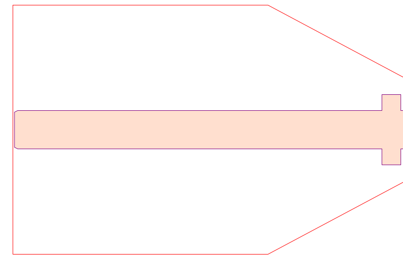

Figure 7

V. Amplifier Packaging

Packaging is a critical point that could result in a irreversibly chip damaging if not carefully considered. Moreover, working conditions are different if compared with the on-wafer testing ones and a on-carrier measurements are necessary to discover possible instability source coming from the carrier design. Designed devices will operate in a 20°K cryogenical environment: cooling down the device also result in a undesirable mechanical deformation, depending on material physical propriety [8]. Semiconductors inside the carrier are usually attached by a conductive epoxy or welded. The different deformation between carrier and semiconductor may cause destructive mechanical stress. With InP semiconductor using common brass carrier results in chip destruction during cooling down process. It has been investigated which kind of alloy could be the best trade off for us and several materials have been compared. Selected material must offer high thermal and electrical conductivity, because carrier is a ground reference and also a heat-dissipating element. Its thermal Expansion Coefficient must be equal or a little bit higher than InP, because semiconductor chip offer better compression than stretching performance. Many efforts have been devoted in order to an alloy that met our specifications. W_{90} / Cu_{10} alloy is produced using an High temperature sintering and infiltrate process. Ni/Au Metallization is possible by Electroplating or Physical Vapor Deposition (Ni metalizzation is necessary to avoid Gold contamination by Cu during heating process necessary for packaging). As reported in the table III this material has excellent physical and mechanical properties. Drawback of this material isn't machinable. Osprey™ CE7 is a Si_{30}/Al_{70} alloy and it has an excellent thermal expansion coefficient and conductivity but this alloy has poor electrical conductivity. This is an important

specification because carrier is our ground reference, and high losses in the carrier could produce mismatch from the expected results. We want investigate if after the gold plating process the poor conductivity of this alloy don't affect the amplifiers performances. The preferred candidate seems to be Silvar-K™ Alloy: It is easy machinable and it has been already cryogenically tested with InP devices from CSIRO-ATNF staff. The major drawback of this alloy is the relevant cost if compared with the other candidates. For these reason two different packaging solutions has been designed. Fig.8 show a conservative solution where the entire carrier is realized with the same material. In order to reduce the quantity of controlled expansion material another solution has been proposed (Fig.9). In this case a small island of alloy is permanently screwed to a brass carrier before the gold plating process and the die will be fixed on this mechanical-stress-absorber with conductive epoxy. Another way to solve the problem could be use indium to weld the die to a common brass carrier. This material is ductile and can absorb mechanical stress inducted by the brass carrier. This solution that seem to be a "Columbus egg" introduce many practical trouble during the amplifier assembling process. At the moment our efforts are devoted to find the best compromise between cost, performances and packaging complexity.

	CTE [μm/m/°C]	Thermal Conductivity [W/m K @ 25°C]	γ [%IACS]
Cu	17.08	398	100
InP	4.05	68	
Brass	>12	>120	4
Kovar	5.03	17	2.02
Silvar-K™	7	110	18
W90 / Cu10	6.05	202	42

Table III

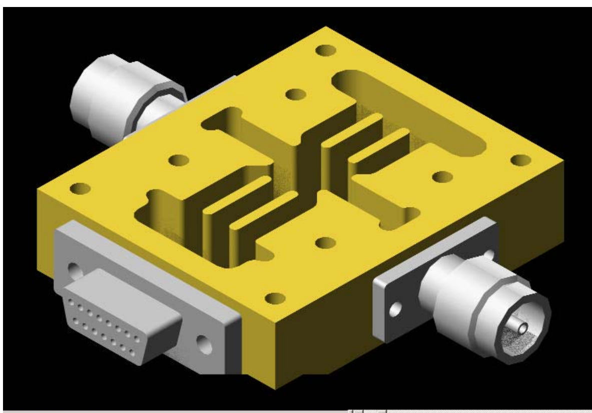

Figure 8

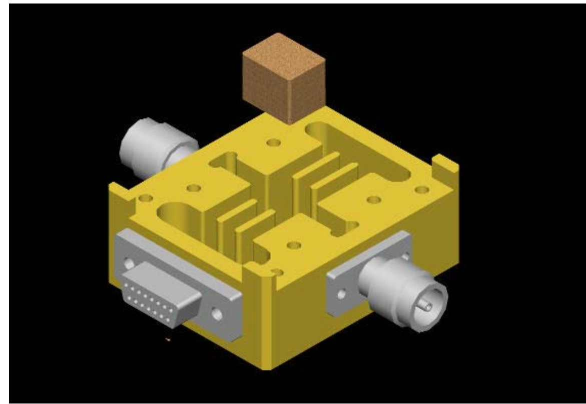

Figure 9

VI. Conclusion

22 Ghz MMIC LNA have been designed, realized and measured. High performances usable devices have been produced. Various package solutions have been adopted to guarantee properly LNA operation . We are moving to use this technology for higher frequency applications, where InP MMIC process will probably lead the games.

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