Performance Analysis of Transimpedance Amplifiers in Various Technologies

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***Abstract* — The paper deals with transimpedance amplifiers (TIA) for optical telecommunication systems in the 10 to 43 Gb/s speed range. The limits of performance in HBT, pHEMT and CMOS technologies are investigated. Detailed noise analysis of the photodiode-TIA cluster is carried out and the factors limiting TIA sensitivity are determined. It is shown that with existent technologies the GaAs pHEMT provides lowest TIA noise.**

I. Introduction

Transimpedance amplifier (TIA), as a first element following the photodiode (Fig. 1a), is the most critical element on the receiving side of an optical link. Both noise performance and time domain response have to be considered when the sensitivity of an optical receiver is optimized.

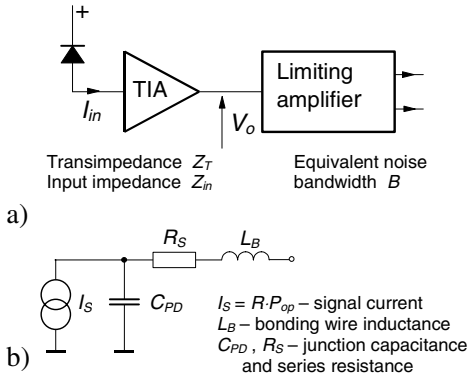


Fig. 1. a) structure of a typical optical receiver, b) small signal model of the photodiode used in this paper.

All available technologies are used currently in the TIA design [1-4] and the performance achieved qualifies these circuits for both 10 Gb/s and 40 – 43 Gb/s systems. Two major TIA configurations predominantly used are shown in Fig. 2.

This paper attempts to analyze the characteristics of the two configurations in a more general way and to provide

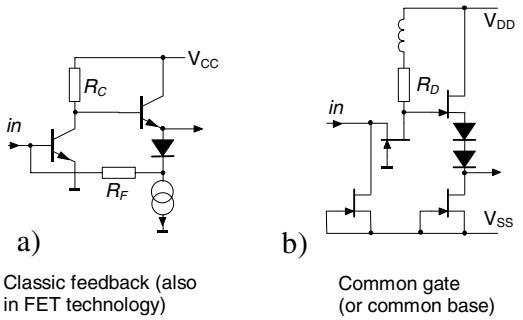


Fig. 2. Typical transimpedance amplifier configurations: a) based on resistive feedback, b) using inherently low impedance input stage (called *straight TIA* in the text)

measures to determine achievable gain and noise performance. Many simplifications were conscientiously used to keep the resulting equations manageable.

Following major assumptions were made: a) voltage follower stage has unity voltage gain and low output impedance (which may not be true in the 40 GHz frequency range); b) noise contribution comes from the first stage and it's load only.

In the first part of the paper the gain and frequency response are considered and the limits on gain for a given bandwidth are derived.

In the second part, general (although simplified) equations for the equivalent input noise current are presented and used to compare both the two configurations and the available technologies.

II. Gain Analysis

Gain analysis of the TIA is based on an equivalent small signal model shown in Fig. 2. The amplifier itself is considered unilateral and its output impedance is neglected. Input impedance Z_{in} is generally high in case of feedback TIA and low in the straight TIA. The model applies to both configurations – for a straight TIA the resistance of R_F is infinite.

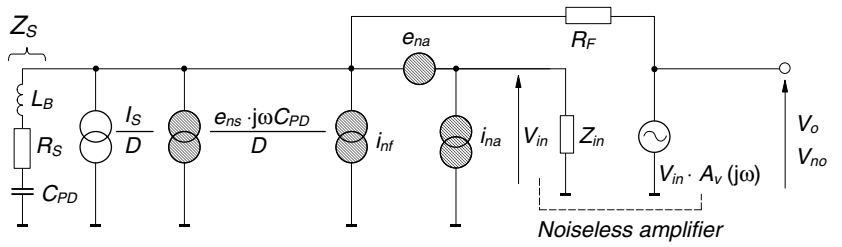


Fig. 2. Equivalent small signal and noise model of a transimpedance amplifier

$$D = 1 + j\omega R_S C_{PD} - \omega^2 L_S C_{PD}$$

$$\overline{e_{ns}^2} = 4kT \cdot R_S \cdot df \quad \overline{i_{nf}^2} = 4kT \cdot G_F \cdot df$$

e_{na} , i_{na} and the correlation admittance $Y_{cor} = \dfrac{\overline{i_{na} \cdot e_{na}^*}}{\overline{e_{na}^2}}$ are the noise parameters of an amplifier (see Appendix).

General expression for circuit transimpedance (Fig. 2) is

$$Z_T = \frac{V_o}{I_S} = \frac{A_v \cdot R_F}{D \cdot (1 - A_v + R_F Y_{in}) + j\omega C_{PD} R_F} \qquad (1)$$

Noise current density referenced to input (I_S source terminals) $i_{nin} = V_{no} / Z_T$ is computed as

$$i_{nin} = D \cdot \left[i_{nf} + i_{na} + \frac{e_{na}}{R_F} \cdot (1 + R_F Y_S) \right] + \mathrm{j}\omega C_{PD} \cdot e_{nS} \qquad (2)$$

In case of no-feedback configuration – like common base input stage – general expressions for Z_T and i_{nin} are

$$Z_T = \frac{A_v}{D \cdot Y_{in} + j\omega C_{PD}} \qquad (3)$$

$$i_{nin} = D \cdot i_{na} + (e_{na} + e_{nS}) \cdot \mathrm{j}\omega C_{PD} \qquad (4)$$

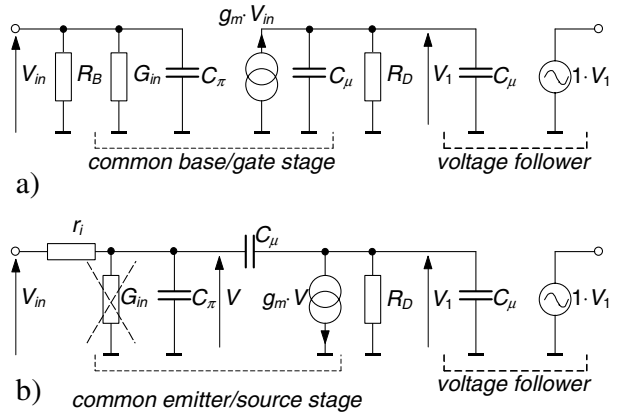


Fig. 3. Simplified small signal equivalent circuit of an amplifier for a straight (a) and feedback (b) configuration. R_B is a bias resistor for the input transistor. Relatively small G_{in} in b) may be neglected at higher frequencies.

The two cases will be dealt with separately. For the straight (no-feedback) circuit the voltage gain may be approximated to the first order as

$$A_v(j\omega) = \frac{A_o}{1 + j\omega\tau_a} = \frac{g_m R_D}{1 + j\omega \cdot 2R_D C_\mu} \qquad (5)$$

where $C_\mu = C_{bc}$ or C_{gd}.
Substituting (5) into (3) the expression for Z_T may be derived in case of $L_B = 0$. This will allow evaluating inherent limitations for this configuration. Z_T is given by

$$Z_T(j\omega) = \frac{R_D}{1 + \mathrm{j}\omega\tau_a} \cdot \frac{1}{1 - \frac{\omega^2 \tau_D}{\omega_T} + \mathrm{j}\omega\left(\frac{C_{PD}}{G_{in}} + \frac{1}{\omega_T} + \tau_D\right)} \qquad (6)$$

where the time constants are: $\tau_a = 2R_D C_\mu$ and $\tau_D = R_S C_{PD}$, and $G_{in} = g_m$, $\omega_T \approx g_m / (C_\pi + C_\mu)$. This equation sets the limit on the transimpedance $Z_T(0) = R_D$ given the photodiode and transistor parameters. For a given bandwidth B an upper limit for the allowable time constant τ_a may be found and hence the R_D value for a certain transistor size and technology.

Next, the gain limits will be derived for three illustrative sets of transistor and photodiode parameters for 10 Gb/s and 40 Gb/s transmission:

A) $f_T = 50$ GHz, $B = 10$ GHz, $C_{PD} = 0.2$ pF, $R_S = 30\ \Omega$.
B) $f_T = 100$ GHz, $B = 10$ GHz, $C_{PD} = 0.2$ pF, $R_S = 30\ \Omega$.
C) $f_T = 160$ GHz, $B = 40$ GHz, $C_{PD} = 50$ fF, $R_S = 20\ \Omega$.

Transistor f_T may easily be achieved with existing bipolar, HEMT or CMOS technologies and case A may be representative for a 0.25 µm CMOS, case B for a 0.13 µm CMOS and case C for a 90 nm CMOS [9].

When L_B is included into the circuit, the transimpedance is given by the fourth order equation:

$$Z_T(j\omega) = \frac{R_D}{(1 + \mathrm{j}\omega a) \cdot (1 + \mathrm{j}\omega b - \omega^2 c - \mathrm{j}\omega^3 d)}$$

where

$$a = \tau_a = 2R_D C_\mu \qquad b = \frac{C_{PD}}{G_{in}} + \frac{1}{\omega_T} + \tau_a \qquad (7)$$

$$c = \frac{\tau_a}{\omega_T} + L_B C_{PD} \qquad d = \frac{L_B C_{PD}}{\omega_T}$$

Equation (6) has been solved for the three cases considered for a range of transistor g_m values. Assumption was made that transistor dimensions are kept constant and g_m is changed by appropriate adjustment of transistor current. C_μ was taken as 15 fF for cases A and B, and 10 fF for case C. Resulting R_D values are plotted in Fig. 4 with solid lines. Eq. (7) was used next to find numerically maximum R_D and suitable inductance L_B to achieve required bandwidth B. Additional constraint was imposed on the frequency response to be monotonic, without any significant peaks. This requirement is needed to assure adequate response in time domain and sufficiently clean eye diagram plot. The results are shown in Fig. 4 with dashed lines.

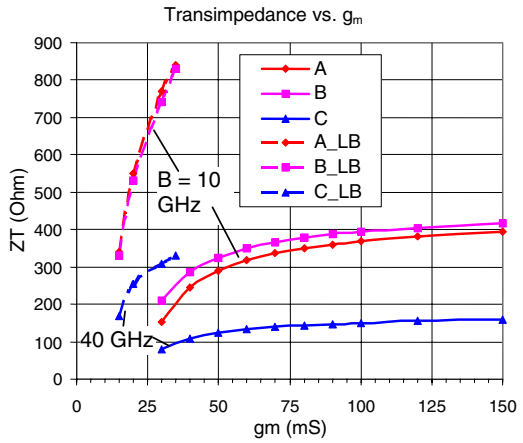


Fig. 4. Transimpedance vs. first transistor g_m for the three cases considered. Solid lines – circuit without L_B, dashed lines – for inductive compensation.

Similar considerations were carried out for a feedback TIA. Relevant equations are given below.

For $L_B = 0$

$$Z_T \approx \frac{-R_F}{1 + \mathrm{j}\omega\left(\tau_D + R_F C_\mu + \frac{C_{PD} R_F}{g_m R_D}\right) - \omega^2 R_F C_\mu \left(\tau_D + \frac{2C_{PD}}{g_m}\right)}$$

For $L_B \neq 0$

$$Z_T = \frac{-R_F}{1 + j\omega a - \omega^2 b - j\omega^3 c} \qquad (8)$$

where

$$a = \tau_D + R_F C_\mu + \frac{C_{PD} R_F}{g_m R_F}$$

$$b = L_B C_{PD} + R_F C_\mu \left(\tau_D + \frac{2C_{PD}}{g_m} \right) \qquad c = L_B C_{PD} R_F C_\mu$$

It is interesting to note that to the first order the response does not depend on transistor f_T assuming that C_μ is consistent with required bandwidth. The major pole is formed by the feedback resistor R_F and the photodiode capacitance.

Analysis similar to the presented above has been performed and the results are presented in Fig. 5 for B = 10 GHz and in Fig. 6 for the bandwidth B = 40 GHz. It was assumed that the load resistance R_D needed might be achieved with appropriate circuitry (passive or active).

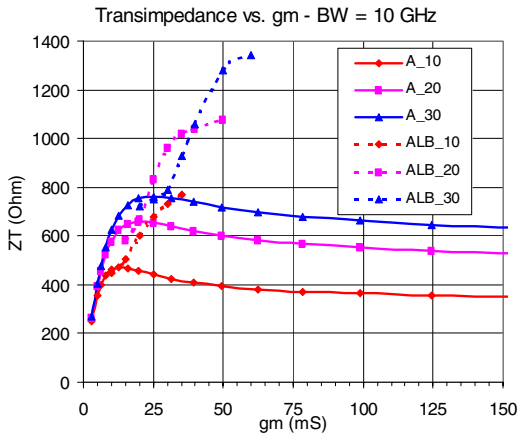


Fig. 5. Transimpedance vs. transistor g_m for the three cases and B = 10 GHz. Solid lines – circuit without L_B , dotted lines – for inductive compensation. Results for the voltage gain $g_m R_D$ = 10 , 20 and 30 are shown.

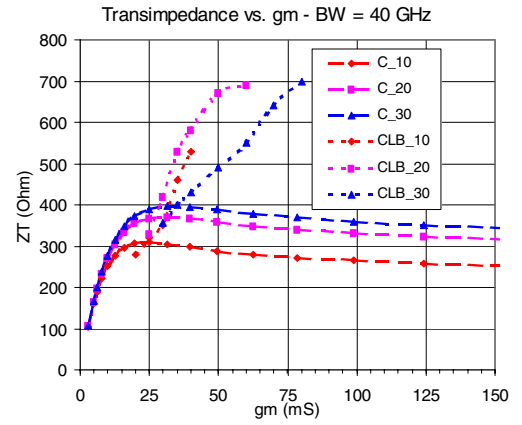
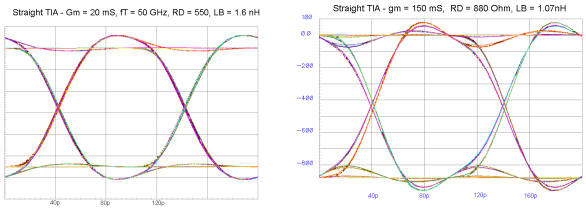


Fig. 6. Transimpedance vs. first transistor g_m for the three cases and B = 40 GHz. Solid lines – circuit without L_B , dashed lines – for inductive compensation.

It may be noticed that the feedback circuit provides approximately 2 times more gain than the straight TIA under comparable conditions. L_B inductor in general allows increasing the gain at a given bandwidth, although the compensation is feasible over a relatively narrow range of g_m values. Particularly in a straight configuration, the low input impedance (at high g_m) causes peaking in the frequency response and corresponding distortion of the eye diagram (see Fig. 7).



a) $g_m = 20$ mS, $R_D = 550\ \Omega$ b) $g_m = 150$ mS, $R_D = 880\ \Omega$

Fig. 7. Eye diagram plots: a) for B = 10 GHz and monotonic response, b) for circuit with too low input impedance and B = 13.8 GHz. 10 Gb/s NZR signal.

III. Noise Analysis

General expressions for the input current noise density are given by (2) and (4). Noise sources e_{na} and i_{na} include contributions from the first transistor, its load and possibly from the bias resistor R_B (Fig. 8).

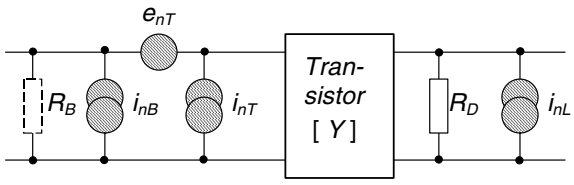


Fig. 8. Noise sources in the amplifier stage. e_{nT} and I_{nT} characterize first transistor

The noise sources e_{na} and i_{na} are given by

$$e_{na} = e_{nT} + \frac{4kTdf}{R_D} \frac{1}{y_{21}} \qquad i_{na} = i_{nB} + i_{nT} + \frac{4kTdf}{R_D} \frac{y_{11}}{y_{21}} \tag{9}$$

Simple expressions were adopted for transistor noise description [2, 3, 5]:

For a bipolar transistor:

$$e_{nT} = 4kT \cdot r_b \cdot df \qquad i_{nT} = 2q \left(\frac{I_C}{|\beta(j\omega)|} + I_B \right) df \tag{10a}$$

For a CMOS transistor:

$$e_{nT} = 4kT \cdot \left(r_G + \frac{\Gamma}{g_m} \right) df \qquad i_{nT} = \frac{4kT\Gamma \cdot (\omega C_G)^2 df}{g_m} \tag{10b}$$

For a HEMT transistor:

$$e_{nT} = \cdot \left(\frac{2qI_D \cdot C_n}{g_m} + 4kT(R_G + R_C) \right) df$$
$$i_{nT} = \frac{2q\, I_D \cdot C_n \cdot (\omega C_G)^2 df}{g_m} \tag{10c}$$

where: C_G is the total gate to channel capacitance, R_G is gate resistance, R_C is a part of a channel resistance under the gate and C_n is the fitting coefficient [5].

Appropriate correlations were taken into account. Input noise current density is given below.

For a non-feedback amplifier:

$$\overline{i_{nin}^2} = |D|^2 \overline{i_{na}^2} + \omega^2 C_{PD}^2 \left(\overline{e_{na}^2} + \overline{e_{nS}^2} \right) + 2\,\mathrm{Re}\left(-D \cdot \overline{i_{na} e_{na}^*} \cdot j\omega C_{PD} \right) \tag{11}$$

For amplifier with feedback:

$$\overline{i_{nin}^2} = |D|^2\left(\overline{i_{nf}^2} + \overline{i_{na}^2}\right) + \omega^2 C_{PD}^2\left(\overline{e_{na}^2} + \overline{e_{nS}^2}\right) + 2\,\mathrm{Re}\left(-D\cdot\overline{i_{na}e_{na}^*}\cdot \mathrm{j}\omega C_{PD}\right) \quad (12)$$

Equations (11) and (12) show the significance of the photodiode capacitance – it is important to use the diode with the lowest possible C_{PD} in high sensitivity systems.

Selected results of analysis are shown in Fig. 9 and 10. Only feedback TIA is presented here as the straight configuration has higher noise, because: transistor input voltage noise is somewhat higher, gain (and hence R_D is lower and additional contribution from input R_B.

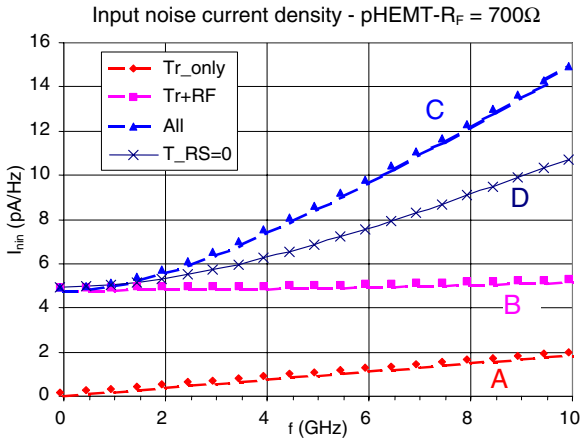


Fig. 9. Components of the total input referred noise current: A – contribution from transistor only, B – transistor and feedback resistor, C – all components, D – noise from photodiode R_S excluded

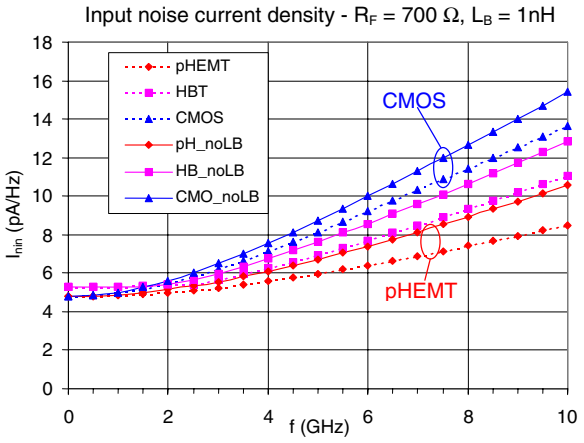


Fig. 10. Input noise current density for a pHEMT, SiGe HBT and CMOS feedback amplifiers. Solid lines: no L_B correction, dotted lines: with L_B = 1 nH. In each case: f_T = 100 GHz, g_m = 25 mS, R_F = 700 Ω

In Fig. 10, three technologies were compared for a particular case of a 10 GHz feedback circuit. Representative transistor parameters were taken from publications [4, 6, 8] and all other factors were kept equal. As may be expected the lowest noise is achieved with the pHEMT devices. Results for 40 GHz TIAs are similar in nature.

When the noise properties are considered under supply power restrictions, the lowest noise at a given bias current is achieved with SiGe and InP bipolar devices, because of their high g_m.

IV. Conclusions

Of the two major configurations of transimpedance amplifiers the feedback TIA (Fig. 2a) provides higher gain at given bandwidth and with the same transistors used. In terms of transimpedance gain, the existing technologies (CMOS, HEMT and bipolar) have comparable capabilities. In terms of sensitivity, (equivalent input noise current) HEMT transistors give best results.

Appendix

Two-port noise figure F vs. source impedance Y_S may be expressed as

$$F(Y_S) = 1 + \frac{\overline{(i_n - e_n\cdot Y_S)^2}}{4\,\mathrm{k}T_0\cdot G_S\cdot df} \quad (A.1)$$

introducing correlation admittance and equivalent noise resistance R_N and conductance G_N

$$Y_{cor} = G_{cor} + \mathrm{j}B_{cor} = \frac{\overline{i_n e_n^*}}{\overline{e_n^2}}$$
$$\overline{i_n^2} = 4\mathrm{k}T_0 G_N df \qquad \overline{e_n^2} = 4kT_0 R_N df \quad (A.2)$$

the two-port noise parameters are given by (A.3)

$$B_{sopt} = B_{cor}$$
$$G_{sopt}^2 = \frac{G_N}{R_N} - B_{cor}^2 \quad (A.3)$$
$$F_{opt} = 1 + 2R_N(G_{sopt} - G_{cor})$$

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