SiGe:C HBT technology for advanced BiCMOS processes.

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***Abstract*— In this paper we discuss the present status of SiGe:C heterojunction bipolar transistors (HBTs), together with some Figures-of-Merit (FOMs) and their relation to technology. We also discuss new innovative solutions to the relatively low breakdown voltage and high-frequency substrate losses of Si technologies, when compared to III-V based technologies.**

I. High-speed SiGe:C HBTs

Silicon Germanium Carbon (SiGe:C) heterojunction bipolar transistors (HBTs) have rapidly found their place in modern BiCMOS technology. Today, SiGe:C HBTs are considered main-stream for radio-frequency (RF) applications. Their success lies in the combination of advanced performance due to band-gap engineering and state-of-the-art lithography, and CMOS compatible device architectures suitable for high-level integration. Fig. 1 shows a typical example (SEM cross-section) of CMOS compatible SiGe:C HBT. Hence, *standard* BiCMOS technologies become a good alternative for new microwave applications [1]–[4].

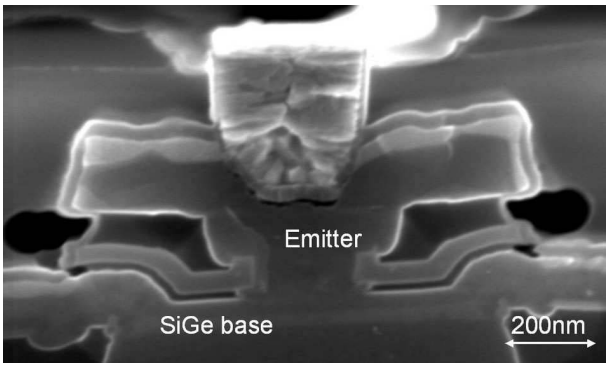

Fig. 1. SEM cross-section of a typical SiGe:C HBT, with a non-selectively grown epitaxial SiGe:C base layer and an in-situ doped emitter.

In speed SiGe:C HBTs have come close to III-V technologies, and the limits have not yet been reached. Cut-off frequencies as high as $f_{\mathrm{T}} = 350\mathrm{GHz}$ [5] and ring-oscillator delays as small as $\tau = 3.6\mathrm{ps}$ per stage [6] have been reported. In this paper we discuss the usefulness of these advanced SiGe:C technologies for microwave applications and make a comparison with III-V technologies, also taking into account parameters like substrate losses and breakdown voltage.

By further vertical- and lateral-scaling with respect to previously reported results [7], and carefully optimising the parasitics [8] we report here on experimental state-of-the-art SiGe:C HBT devices.

Fig. 2 shows a typical Gummel-plot, from which it can be seen that both I_{C} and I_{B} are ideal over a wide range of V_{BE}, with a slope close to 60mV/dec.

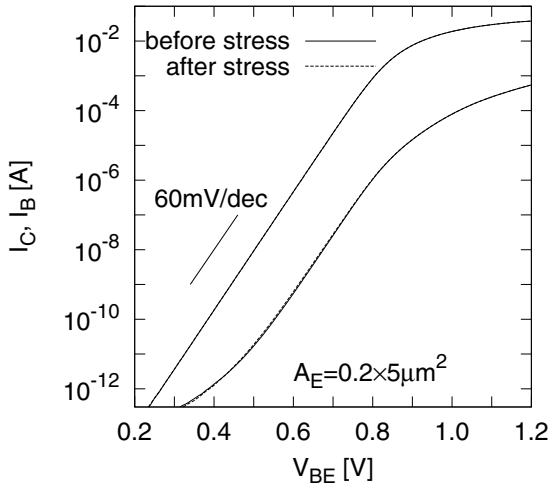

Fig. 2. Typical Gummel-plot, I_{C} and I_{B} versus V_{BE}, of a device with an emitter area of $0.2 \times 5\mu\mathrm{m}^2$, before and after high-current stress. Device are stressed for 11h. at $I_{\mathrm{E}} = 20\mathrm{mA}$ with $V_{\mathrm{CB}} = 1\mathrm{V}$, and measured with $V_{\mathrm{CB}} = 0\mathrm{V}$.

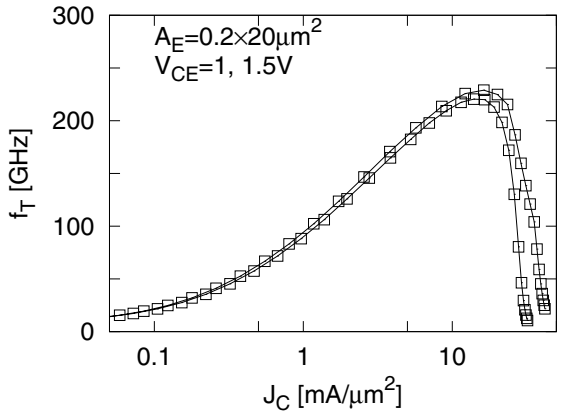

Fig. 3. Cut-off frequency f_{T} versus collector current density J_{C}, for similar devices as shown in Fig. 2.

In Fig. 3 the f_{T} is plotted versus collector current density J_{C}, showing a peak of $f_{\mathrm{T}} = 230\mathrm{GHz}$ at $J_{\mathrm{C}}^{\mathrm{top}} = 16\mathrm{mA}/\mu\mathrm{m}^2$. To demonstrate the superior robustness of these devices, compared to *e.g.* GaAs or InP based HBTs, we have also stressed them for up to 11 hours at $J_{\mathrm{C}} = 1.25 \times J_{\mathrm{C}}^{\mathrm{top}}$ ($V_{\mathrm{CB}} = 1\mathrm{V}$). As seen in Fig. 2, this has no impact on I_{C} or I_{B}.

Based on the results obtained from our experimental SiGe:C HBTs and by further realistic scaling of the vertical transistor profile, we have performed (2D) device simulations. These simulations show that devices with a cut-off frequency $f_{\mathrm{T}} \approx$

500GHz are certainly a possibility (see Fig. 4), provided also the lateral dimensions and parasitics are scaled proportionally, see also Sec. II

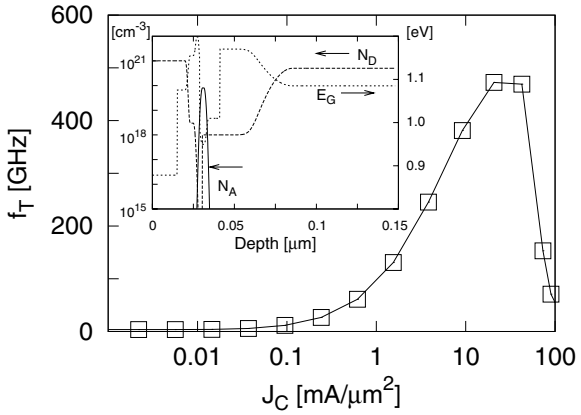

Fig. 4. Simulated (2D) $f_{\rm T}$ versus $J_{\rm C}$ of a scaled Si/SiGe HBT. The inset shows the vertical transistor profile: donor-, N_D (dashed), and acceptor-, N_A (solid), concentration, and effective bandgap E_G (dotted).

II. Figures-of-Merit and Technology

To characterise the high-frequency performance of RF devices, the cut-off frequncy $f_{\rm T}$ and maximum oscillation frequency $f_{\rm max}$ are the most commonly quoted figures-of-merit (FOM). $f_{\rm max}$ is often said to be a more reliably FOM, because it takes external parasitics into account. However, Agarwal *et al.* [8] already showed that, with advanced devices, also $f_{\rm T}$ strongly depends on series resistances in the emitter- and collector-lead ($R_{\rm E}$ and $R_{\rm C}$), and parasitic collector-base capacitance ($C_{\rm CB}$),

$$\frac{1}{2\pi f_{\rm T}} = \frac{C_{\rm T}}{g_m} + \tau_N + (R_{\rm E} + R_{\rm C}) \times C_{\rm CB}, \qquad (1)$$

with $g_m = dI_{\rm C}/dV_{\rm BE}$ is the transconductance, $C_{\rm T} = C_{\rm EB}^{\rm diff} + C_{\rm EB}^{\rm depl} + C_{\rm CB}$ is the total capacitance, and τ_N is the minority delay in the neutral base- and collector-region [9]. Hence, the only parasitic not included in $f_{\rm T}$ that is included in $f_{\rm max}$ is the base resistance ($R_{\rm B}$), as is expressed in the (over-simplified) relation

$$f_{\rm max} = \sqrt{\frac{f_{\rm T}}{8\pi R_{\rm B} C_{\rm CB}}}. \qquad (2)$$

From Eq.(1) one can see that in order to increase the $f_{\rm T}$, one should increase the ratio of the transconductance g_m over the total capacitance $C_{\rm T}$. For this, two technology parameters are involved: with band-gap engineering in the base (*i.e.* by applying SiGe) one can increase g_m, *without* lowering the base doping N_A^b, which would result in early high-injection effects in the base. Reducing the emitter access resistance $R_{\rm E}$ helps to minimise the voltage drop, and hence, result in a higher junction voltage and thus collector current. The reduction in $R_{\rm E}$ also helps to reduce the RC-delay, the second term in Eq.(1). The other two parameters in the RC-delay, $R_{\rm C}$ and $C_{\rm CB}$ are both linked to the collector doping N_D^c. Agarwal *et al.* [8] showed that N_D^c has an optimum value for peak-$f_{\rm T}$, depending on other parameters, like $R_{\rm E}$. This optimum doping level then only leaves the base access resistance and the lateral transistor dimensions (both for $R_{\rm B}$ and $C_{\rm CB}$) as the parameters to improve on $f_{\rm max}$.

As was already discussed for instance by Hurkx [9], $f_{\rm T}$ and $f_{\rm max}$ are defined for conditions normally not met in actual circuits. As an alternative FOM, which does include real circuit conditions, the available bandwidth (-3dB compression) is proposed [10]. By choosing a proper load admittance, $y_{\rm L}$, the voltage gain of a common emitter stage can be expressed in the transistor Y-parameters,

$$G_V = \frac{v_o}{v_i} = \frac{-y_{21}}{y_{22} + y_{\rm L}}. \qquad (3)$$

From the frequency dependence of the transistor Y-parameters it is then possible to define the available bandwidth, $f_{\rm A}$, as a sum of the input- and output-bandwidth, $f_{\rm v}$ and $f_{\rm out}$ [10]:

$$\begin{aligned} \frac{1}{2\pi f_{\rm A}} &= \frac{1}{2\pi f_{\rm v}} + \frac{1}{2\pi f_{\rm out}} \\ &= R_{\rm B} C_{\rm T} + R_{\rm L} C_{\rm out}, \end{aligned} \qquad (4)$$

where $R_{\rm L} = 1/{\rm Re}(y_{\rm L})$ is the load resistance, and $C_{\rm out} \approx C_{\rm CS} + (1 + g_m R_{\rm B}) C_{\rm CB}$ is the total capacitance seen at the output, including the Miller-effect on $C_{\rm CB}$.

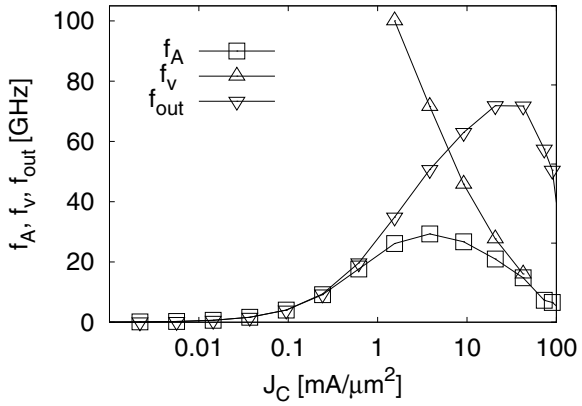

Fig. 5. Voltage gain bandwidth, $f_{\rm A}$, as a function of collector current bias, together with the separate components $f_{\rm v}$ and $f_{\rm out}$, see Eq.(4).

Fig. 5 shows the bias dependence of the different components in Eq.(4), together with the resulting bandwidth, for the same simulated device as used for Fig. 4. This plots shows that although this device has an extremely high $f_{\rm T}$, it may still be limited in its usefulness for high-frequency microwave applications. In this case the available bandwidth $f_{\rm A}$ is limited by the high $C_{\rm CB}$. This high $C_{\rm CB}$ is a direct result of the high collector doping needed to reach the very high $f_{\rm T}$, showing that optimisation towards high $f_{\rm T}$ does not necessarily leed to the most optimal device for circuit application.

III. Substrate losses

When compared to III-V based technologies, *e.g.* GaAs and InP, Si-based technologies, *e.g.* SiGe BiCMOS, have a clear advantage with respect to large-scale integration (System-on-Chip, SoC) and in general also a cost advantage for high volume production. The intrinsic transport properties in silicon, however, have some significant draw-backs when compared to common III-V materials like GaAs and InP. It has both a lower band-gap and a lower (electron) mobility.

The relatively small bandgap of Si, as compared to GaAs and InP, is responsible for a higher substrate conductivity. Even for ultra-lowly doped Si-substrates only a small amount of residual oxide charge is needed to create a conductive channel

at the Si-SiO_2 interface, thereby significantly increasing the effective substrate conductivity [11]. This relatively high substrate conductivity results in higher substrate losses, especially at RF frequencies, than for the semi-insulating GaAs and/or InP substrates.

Since most of the substrate is only used as a carrier, the actual devices are only made in the top 1—2μm, the most straight-forward way to limit the influence of the lossy substrate is to simply remove it and replace it by a different carrier. The substrate transfer technology (STT), described by Dekker *et al.* [12], could in principle be applied to any process. This was shown successfully by Aksen *et al.* [13], who processed an early development version of QUBiC4G [14] on SOI substrates. The transfer to glass and subsequent removal of the silicon substrate and thick copper backside metalisation is then quite straight-forward, see Fig. 6.

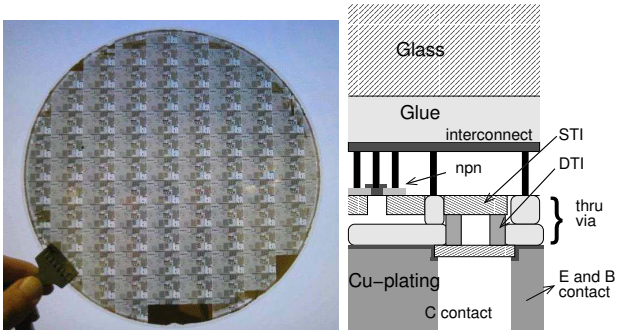

Fig. 6. Fully processed BiCMOS wafer, transfered to a glass substrate (left), and the schematic cross section of the process, with the thick copper connection at the backside (right).

This approach yields excellent substrate isolation *without* any degradation of the intrinsic device performance. In fact, the available bandwidth f_{A}, which strongly depends on the output capacitance, is significantly improved by removing the substrate and hence effectively eliminating the collector-substrate capacitance C_{CS}, see Fig. 7.

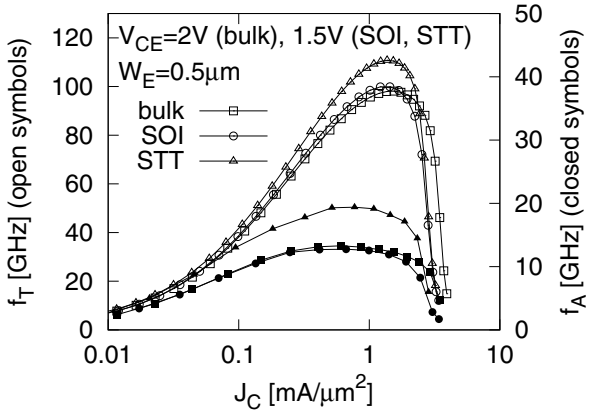

Fig. 7. Measured f_{T} (open symbols, left axis) and f_{A} (closed symbols, right axis) as a function of collector current density, for identical devices on bulk silicon, on an SOI substrate, and after transfer to glass (STT).

IV. Breakdown Voltage

The lower bandgap of Si is also the main cause of the lower critical electric field before breakdown, when compared to GaAs or InP. To reach the very high speed in today's SiGe:C devices, the collector is relatively highly doped, causing high electric field peaks at the collector-base junction. This results both in earlier junction breakdown $\mathrm{BV_{CB0}}$, and earlier feedback breakdown $\mathrm{BV_{CE0}}$. Recently Hueting *et al.* [15] proposed a new device concept, that applies the so-called Resurf or field shaping effect [16], well known for high-voltage power devices, to a lower voltage RF device. Using trenches filled with a field-plate along the collector drift region, together with an optimised doping profile, the electric field is flattened, resulting both in a higher breakdown voltage and a delayed on-set of the Kirk-effect [17]. The delayed Kirk-effect, in turn, results in a higher peak f_{T}. Hence, the $f_{\mathrm{T}} \times \mathrm{BV_{CB0}}$ product, which serves as a FOM for the trade-off between speed and breakdown, can be improved by as much as a factor of 2 to 3.

First experimental evidence of this improved speed to breakdown trade-off by using the Resurf-effect was shown by Melai *et al.* [18], using a slightly different device, with a *pin*-diode between the base- and collector-contact along-side the collector drift region in stead of the field-plate proposed in [15]. Fig. 8 shows a cross section of this so-called Resurf HBT (RHBT), while Fig. 9 shows the f_{T}, $\mathrm{BV_{CB0}}$ and the $f_{\mathrm{T}} \times \mathrm{BV_{CB0}}$ product as a function of device-width (emitter-width). Since the field-shaping effect depends on a limited amount of charge, it only occurs over a limited distance, decreasing for increasing back-ground doping. Hence, for reasonably fast devices with a collector drift-region doping in the order of $10^{17}\mathrm{cm}^{-3}$ the Resurf-effect only works for devices with a width well below 1μm. For sufficiently narrow devices a strong improvement in the trade-off is found. For devices with an emitter-width $W_E = 0.7\mu$m we obtain an optimum of $\mathrm{BV_{CB0}} = 24\mathrm{V}$ and $f_{\mathrm{T}} = 27\mathrm{GHz}$, yielding a product of $f_{\mathrm{T}} \times \mathrm{BV_{CB0}} = 650\mathrm{GHzV}$.

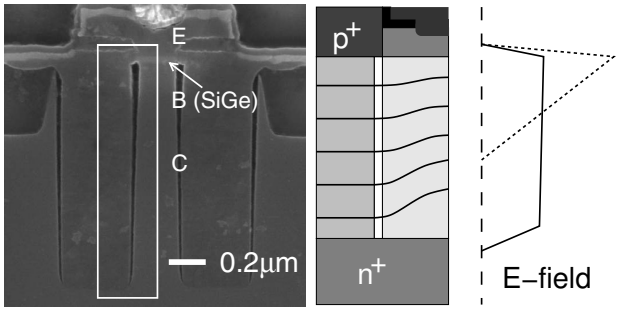

Fig. 8. SEM cross section of a Resurf HBT (left), and a schematic view of half the device (rectangular area in SEM), showing the Resurf effect of the pin-diode in the trench on the electric field in the collector drift-region (right).

The trade-off between f_{T} and $\mathrm{BV_{CB0}}$ is very important, especially for RF-power applications, for which it is more efficient to generate high RF power using a high voltage rather than a high current, see for instance [19]. This trade-off is benchmarked between different technologies in Fig. 10. From this benchmark study we see that reasonably high $f_{\mathrm{T}} \times \mathrm{BV_{CB0}}$ products are obtained at low $\mathrm{BV_{CB0}}$ (mainly SiGe), but at higher values, $\mathrm{BV_{CB0}} \gtrsim 20\mathrm{V}$, almost exclusively GaAs or InP devices are found. With the RHBT we obtain an $f_{\mathrm{T}} \times \mathrm{BV_{CB0}}$ product comparable to that of GaAs devices. Simulations predict that, by further device optimisation, it is possible to obtain values of $f_{\mathrm{T}} \times \mathrm{BV_{CB0}} > 2000\mathrm{GHzV}$ at $\mathrm{BV_{CB0}} = 25\mathrm{V}$, comparable to the best III-V results published [20].

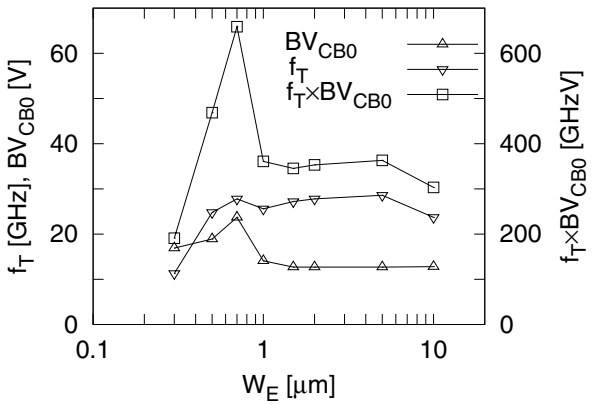

Fig. 9. Measured $\mathrm{BV_{CB0}}$, f_T and their trade-off versus emitter-width W_E in a Resurf HBT.

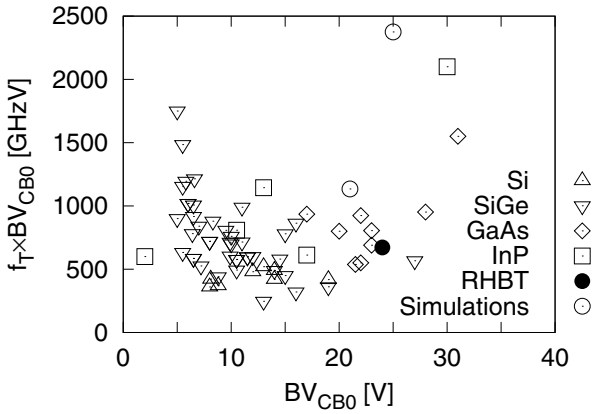

Fig. 10. Benchmark of the $f_\mathrm{T} \times \mathrm{BV_{CB0}}$ product as a function of $\mathrm{BV_{CB0}}$, for various technlogies, as found in literature. The filled circle shows the optimum device shown in Fig. 9. The open circles are the result of simulation on optimised devices [15].

V. Conclusions

SiGe:C Heterojunction Bipolar Transistors have entered the speed range previously only accessable with III-V technologies. To fully benefit from this improved speed, however, it is essential to take into account all parasitics.

The high level of integration in Si-based technologies clearly have an advantage for analogue/mixed-signal applications, for a full System-on-a-Chip (SoC). However, for high frequency devices, there are two main draw-backs: the lossy silicon substrate, and the low critical electric field at breakdown, both related to the relatively small band-gap of Si. For both issues a possible solution has been shown. By applying Substrate Transfer Technolgy (STT), we have complete freedom of choice for the final substrate, thereby reducing the substrate parasitics significantly, or even eliminating them completely. The small lithographic dimension possible in modern Si-based technologies, allows to use the Resurf effect down to 20—25V, which improves the $f_\mathrm{T} \times \mathrm{BV_{CB0}}$ product for a SiGe HBT with a factor of 2 to 3.

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