SiGe Building Blocks for Microwave Frequency Synthesizers

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***Abstract*— Implementations of Ku- and Ka-band PLL building blocks in the Philips QUBiC4G SiGe technology are presented: a 10 GHz fully-integrated low-phase-noise differential Colpttis oscillator, a 25 GHz low-power adaptive prescaler, and a 18 GHz truly-modular fully-programmable frequency divider.**

I. Introduction

Traditionally, phase-locked loop (PLL) microwave frequency synthesizers rely on dielectric resonator oscillators and sampling phase detectors [1], [2]. These signal sources profit from the high quality factor of the dielectric resonator and the absence of frequency dividers within the PLL to provide very low levels of phase noise. However, dielectric resonators can not be integrated on a chip, and are quite bulky in respect to usual MMIC dimensions. In addition, application flexibility and variable output frequency for e.g., channel or band selection, demand the use of programmable frequency dividers within the feedback loop.

The relative complexity of frequency dividers and fully-integrated oscillators makes them an expensive building block when realised in III-V technologies. In this paper, we will highlight microwave PLL building blocks implemented in a main-stream production SiGe technology [3]. After a brief review of the technology, we will discuss a low-phase-noise fully-integrated VCO, a low-power fixed frequency divider with programmable input sensitivity, and a truly-modular programmable frequency divider. These building blocks can be placed on a generic PLL configuration as presented in Fig. 1.

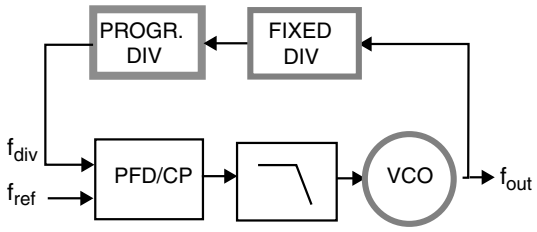

Fig. 1. Phase-locked loop frequency synthesizer. Blocks in gray are discussed in this paper.

II. Technology

We used the QUBiC4G BiCMOS process from Philips Semiconductors [3]. It features a range of devices for high-frequency mixed-signal designs, including $f_T/f_{max} = 70/100$ GHz NPNs, 0.25 μm CMOS, poly-silicon resistors with 90, 220, 365 and 2000 ohm/sq., a 5.7 fF/μm^2 oxide capacitor and a 5 fF/μm^2 MIM capacitor. Minimum drawn NPN emitter size is 0.5x1.0 μm. The double poly SiGe NPN heterojunction bipolar transistors feature an Inside L-Shaped spacer between the base and emitter which creates sub-lithographic emitter openings. Collector to substrate parasitic capacitance C_{cs} has been reduced by the use of deep trench isolation (DTI), and base to collector parasitic capacitance C_{cb} has been reduced by the use of shallow trench isolation (STI). The process features five metalization layers, with two thick top layers for high-quality on-chip inductors and transmission lines.

III. Fully-integrated VCO

In this section, we report on the feasibility study of a 10 GHz fully-integrated microwave voltage-controlled oscillator (VCO) in QUBiC4G technology. We opted for a differential common-base Colpttis topology. In addition, band switching was applied to reduce phase noise degradation due to external noise sources coupled to the tuning input of the VCO.

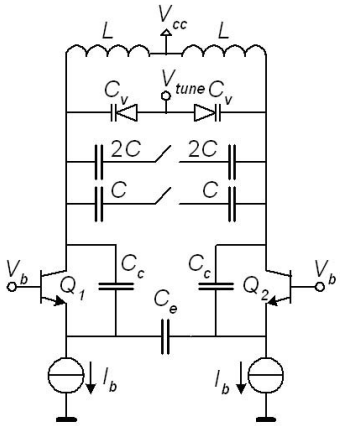

Fig. 2. Switched differential common-base Colpitts VCO topology.

A. Circuit design

Colpitts-type oscillators have better phase noise performance than cross-coupled oscillators. This is mostly due to a higher output voltage swing and better energy transfer efficiency between the active circuit and the tank [4]. The differential common-base Colpitts VCO implemented in this work is shown in Fig. 2. It consists of a tank circuit with discrete (capacitor array) and continuous (diode varactors) tuning and an active negative conductance formed by $Q1$, $Q2$, C_c and C_e. The capacitive divider formed by C_c and C_e has three main functions: together with the inductor, varicaps and the capacitor array, it determines the oscillation frequency of the oscillator; it forms a positive feedback loop between the active devices and the tank [5]; and it acts as an interface

circuit between the LC tank and the active circuit components. The quality factor Q of the tank is maintained through the transformation of the resistive load seen at the active device emitters α/gm (with α the common-base current gain), into a higher differential impedance $R_{eq|tank}$ seen at the tank terminals,

$$R_{eq|tank} \approx 2\left(1+\frac{2C_e}{C_c}\right)^2 \frac{\alpha}{gm} \quad (1)$$

There is a trade-off between loop-gain and tank Q in choosing the capacitance ratio C_c/C_e. The value used in this design is $C_c/C_e = 1$, including active device parasitic capacitors. Simulations showed that this was the optimum ratio with respect to phase noise. The tuning elements (diode varactors and capacitor array) are placed in parallel to the inductor, so that C_c/C_e remains relatively constant over frequency. Compared to other integrated common-base Colpitts oscillators [5], where the varactors are placed in parallel to C_e, this set up reduces variation in tank Q-factor and thus VCO phase noise with tuning.

In this design, a circular single-turn inductor is used. To reduce substrate losses and parasitic capacitances, a waffle-patterned DTI shield is placed beneath the inductor. The 3 μm thick top-metal-layer inductor has an inner diameter of 270 μm with a width of 10 μm. Measurements showed an equivalent differential inductance of around 0.66 nH in the 10 GHz frequency range. The measured Q factor is about 26 at 10 GHz and peaks at around 20 GHz with a value of 30. Inductor and VCO simulations were performed using the compact model described in [6]. Simulations showed that the tank voltage swing reaches up to 3.4 V peak in the highest frequency band.

B. Measurements

A photomicrograph of the switched VCO with integrated buffer is shown in Fig. 3. The layout was made as symmetrical as possible to ensure true differential operation. It includes on-chip supply and tuning voltage decoupling, and occupies 0.8 x 0.91 mm^2 of die area including bond-pads. Active area is 0.4 x 0.53 mm^2.

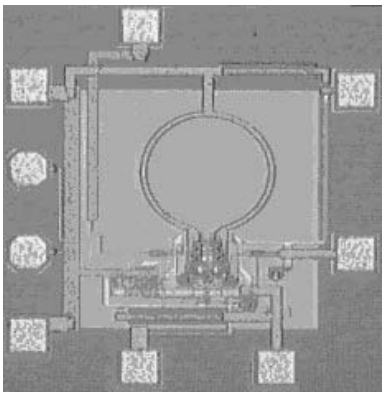

Fig. 3. Photomicrograph of the switched VCO.

The measured tuning characteristic is shown in Fig. 4. The switched oscillator covers a tuning range of 9.4 GHz to 10.7 GHz in four bands of approximately 500 MHz each. The phase noise of the VCO was measured on-wafer using the HP3048A setup. It achieves a phase noise performance of up to -94.4 dBc/Hz at 100 kHz offset from a 10.5 GHz carrier, as seen in

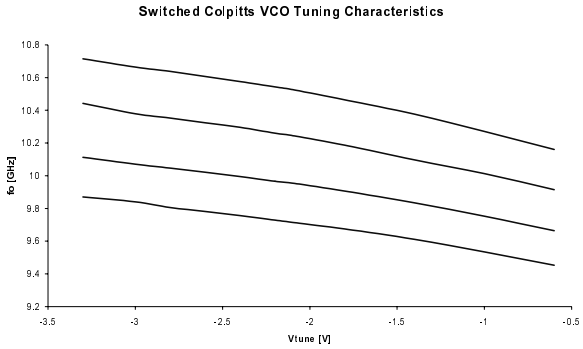

Fig. 4. VCO frequency as a function of reverse tuning voltages, for the different bands.

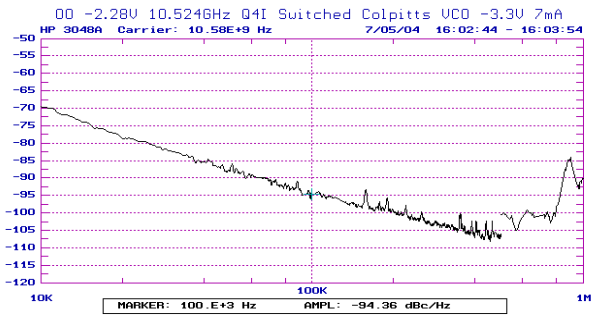

Fig. 5. Switched Colpitts VCO phase noise measurement. The increased noise level close to 1 MHz offset frequencies is due to imperfect decoupling of the on-wafer measurement system.

Fig. 5. The VCO consumes 7 mA in each of the core devices and operates on a supply voltage of 3.3 V.

IV. Fixed-ratio frequency divider

In this section we describe a low-power frequency divider, namely a prescaler divide-by-8 circuit. The prescaler consists of an input amplifier, of a cascade of three divide-by-two stages, and of an output buffer with 50 Ω output impedance for simple interfacing to PCB microstrip lines.

A. Circuit design

The divider cells are based on the toggle flip-flop principle. The toggle flip-flop consists of two D-latches in series, with the inverted output of the second latch being fed-back to the input of the first latch, see Fig. 6. A current-mode-logic (CML) D-latch consists of a "gate" differential pair (the "gate pair") and of a cross-coupled differential pair (the "latch pair").

The maximum operation frequency of the toggle flip-flop is determined by the load on the output of the gate differential

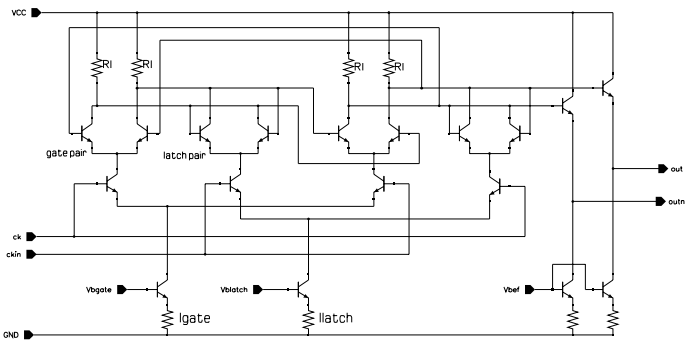

Fig. 6. Circuit implementation of an adaptive divide-by-2 cell (adaptive toggle flip-flop).

pairs [7]. Fig. 6 shows that the output of a gate pair is loaded by the latch pair and by the input circuitry of the other gate pair. An analysis of the load at the output of the gate pair shows that the latch pair accounts for a significant fraction of the load.

At the relatively high current density levels used to achieve peak f_T in the transistors, the dominant parasitic elements of the latch pair are the base-emitter diffusion capacitances, followed by the base-emitter and the collector-substrate junction capacitances. The junction capacitances can be decreased by sizing of the latch pair transistors, and a decrease of the base-emitter diffusion capacitances can be achieved with a decrease of the current flowing in the latch pair. This is not possible with a standard D-latch implementation [7], [8], because the gate and latch differential pairs share the same biasing current source.

In our circuit we splitted the bias currents of the gate and latch pairs as depicted in Fig. 6 [9]. This enables the bias current of the latch pairs I_{latch} to be set independently of the gate pair biasing current I_{gate}, decreasing the parasitic diffusion capacitances. A decrease of the parasitic junction capacitances was achieved by choice of a smaller transistor size. At low frequencies the current I_{latch} can be increased to improve the low-frequency sensitivity level, when necessary. In this way the divider described here features a programmable input sensitivity capability.

B. Measurements

Measurements of the processed frequency divider have been performed on-wafer. The biasing currents I_{gate} and I_{latch} can be set externally through input pads. The results of on-wafer sensitivity measurements are presented in Fig. 7, for three different situations of I_{latch}, with $I_{gate} = 1.5$ mA. Decreasing I_{latch} increases the maximum operation frequencies as discussed in the previous section. Note the shift in the free-running oscillation frequencies as well. High sensitivity at both ends of the sensitivity curve can be obtained by making I_{latch} adaptive as a function of the operation frequency, extending the operation range with respect to standard techniques.

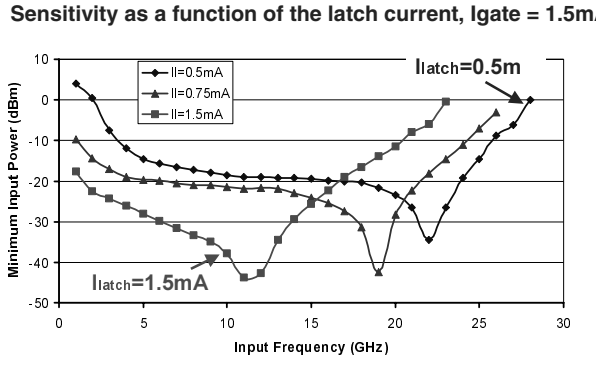

Fig. 7. Input sensitivity as a function of the latch current level. On-wafer measurements. I_{gate} = 1.5 mA, I_{total} = 23 mA, Vcc = 2.7 V.

V. Programmable Divider

High-frequency fully-programmable dividers are conventionally implemented as a combination of a dual-modulus prescaler (of division ratios P, P+1) and two-additional frequency counters [10]. This approach lacks modularity and complicates design and layout work. In this section, we highlight a 18 GHz fully-programmable divider which can divide by any integer number in the range 16-255. The divider is based on the extended programmable prescaler architecture [11], [12], eliminating the need for additional frequency counters. The circuit can be used as a generic building block for integer and fractional-N PLLs, or in wide-band PLLs operating with large reference frequencies for VCO phase noise suppression.

A. Programmable divider architecture

The architecture of our modular programmable divider is presented in Fig. 8. It is based on a cascade of 2/3 divider cells. A chain of n 2/3 cells provides division ratios in the range 2^n to $2^{n+1} - 1$. Extended division range is obtained if the effective length of the divider chain n'_{min} is changed as a function of the programmed division ratio, with the use of extra OR gates as seen in Fig. 8. Without the OR gates a chain of 7 programmable-by-2/3 divider cells provides division ratio from 128 to 255. To have a building block with higher application flexibility, we added OR gates to extend the division range from 16 up to 255. In our case, $n'_{min} = 4$ and $n = 7$. The modularity of the circuitry enables modification of the division range and of the maximum input frequency by addition or removal of basic 2/3 divider cells to the existing structure.

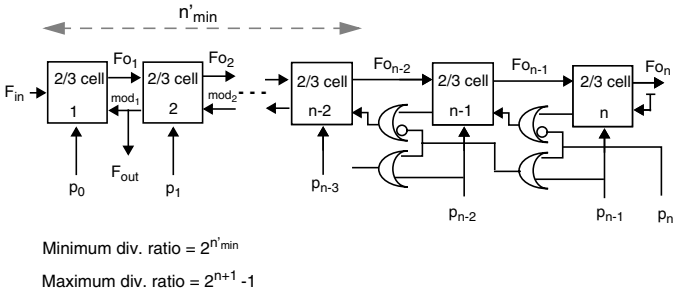

Fig. 8. Block diagram of a modular programmable divider with extended division range. In our design $n'_{min} = 4$ and $n = 7$, providing division from 16 up to 255.

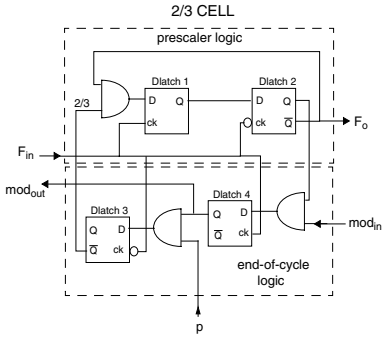

Fig. 9. Functional blocks and logical implementation of a 2/3 divider cell.

B. Circuit implementation

The logical implementation of the 2/3 divider cells is depicted in Fig. 9. The *prescaler logic* block divides, upon control by the *end-of-cycle logic*, the frequency of the F_{in} input signal either by 2 or by 3, and outputs the divided

clock signal to the next cell in the chain. The divider was implemented entirely with current-mode logic (CML) circuitry. Fig. 10 depicts an AND-Dlatch circuit as used within the 2/3 divider cells. The nominal logic swing is ± 200 mV. Level shifters were inserted between cells to adjust the DC levels and avoid saturation of the bipolar transistors. The current levels of different cells were adjusted as a function of its input frequency. A transient simulation result is presented in Fig. 11, with an input frequency of 15 GHz. The divider is programmed to divide by 31, i.e. the 4 high frequency cells are programmed to divide-by-3 once in a division cycle. As the divider output signal, one can take any of the *mod* signals.

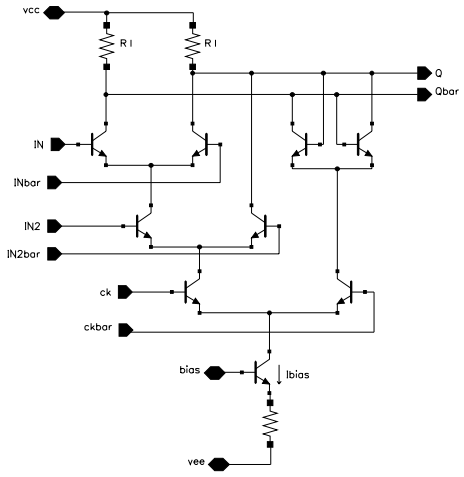

Fig. 10. Circuit implementation of an AND-latch logic cell.

C. Measurements

The programmable divider was evaluated on-wafer. When testing on-wafer, open programming inputs (floating pads) translate into a logic 1 level at each 2/3 cell, e.g. the divider will divide by 255 if all inputs are open. The measured

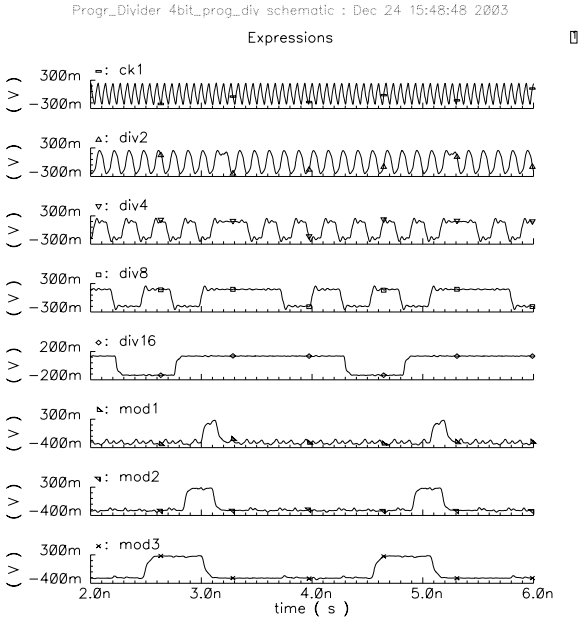

Fig. 11. Transient simulation of the optimized frequency divider. Division ratio = 31, f_{in} = 15 GHz.

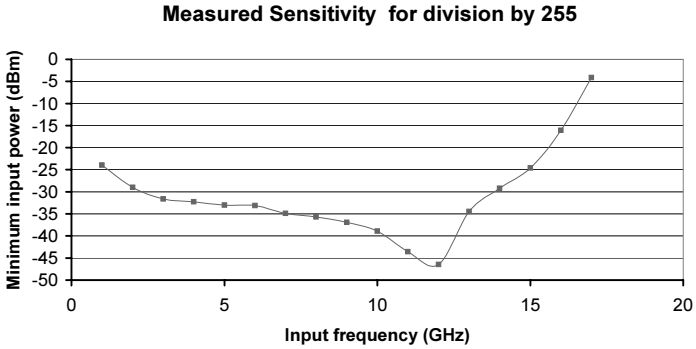

Fig. 12. Measured input sensitivity of the fully-programmable divider.

sensitivity of the divider in this condition is presented in Fig. 12. The maximum operation is 18 GHz, with all divider cells programmed to divide-by-3 (worst-case situation). The core divider cells consume 35 mA at a supply voltage of 3 V.

VI. Conclusion

We presented building blocks for PLL microwave frequency synthesizers in the SiGe QUBiC4G BiCMOS process of Philips Semiconductors: a low phase noise fully-integrated common-base Colpitts VCO with a switched tank circuit; a low-power frequency divider (divide-by-8) with programmable input sensitivity and extended operation range with respect to standard techniques; and a fully-programmable 16-to-255 frequency divider featuring a modular architecture.

Acknowledgement

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