Application of UTSi® CMOS On Sapphire to RF and Mixed Signal Requirements in Advanced Space Systems

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Modern satellite systems require integrated circuits capable of meeting demanding radiation, performance, power consumption, price and integration requirements. As satellite systems evolve to large digital payloads and phased array antennae, highly integrated mixed signal and RF ICs are becoming critical to overall system performance. Ultra-Thin-Silicon, or UTSi, CMOS is a modern, high yield version of silicon on sapphire which provides natural radiation hardness with the advantages of high volume commercial CMOS manufacturing. This paper will discuss the variety of products and their performance available for satellite applications from Peregrine Semiconductor, including phase locked loops, mixers, switches, A/D converters, EEPROM, digital logic and integrated passive devices.

Introduction

In this paper we describe one of the newest variations on the CMOS theme: commercial quality CMOS built in silicon on sapphire called UTSi CMOS. We present basics of the technology, including materials, devices, processing, models, and circuit functions and how these factors relate to multi-Gigahertz and mixed signal IC's.

Utsi Technology description

Silicon on sapphire, SOS, was invented in the early 1960's at Rockwell and proved its high speed and low power potential. In its original embodiment poor crystalline quality resulted in very low yields and therefore in high cost. The defects are eliminated by a simple two-step process consisting of an ion implantation followed by an anneal/oxidation [US patent 5,600,169]. With the defects removed, ultrathin (1,000 A, or less) layers of high quality silicon are achieved. CMOS circuitry is then fabricated by a standard, but simplified, process flow (certain steps are eliminated thanks to the insulating sapphire substrate). Figure 1 shows a cross-sectional view comparing bulk Si CMOS to UTSi CMOS. Advantages of forming UTSi CMOS transistors on a pure sapphire substrate are manifold including the following:

- Lower capacitance and therefore higher speed at lower power
- Fully depleted operation, improving linearity, speed, and low voltage performance
- Excellent RF performance:
  - f_{max} typically 3X f_t (60 GHz at L = 0.5 µm; and 100 GHz at 0.25 µm)
  - very high linearity (+38 dBm IP3 mixers)
  - high Q integrated passives (Q_L > 40 at 2 GHz for 5 nH inductor)
  - high isolation (>50 dB between adjacent devices)
- Integrated EEPROM available without additional masks or process steps
- Multiple threshold options without additional cost
- An extremely low-loss substrate at RF frequencies
- Excellent ESD protection with low parasitics
- New design options over GaAs due to availability of good PMOS transistors
- Optically transparent substrate for use in optical applications
- Processed in standard CMOS facilities on large wafers
- Lower cost than other RF processes

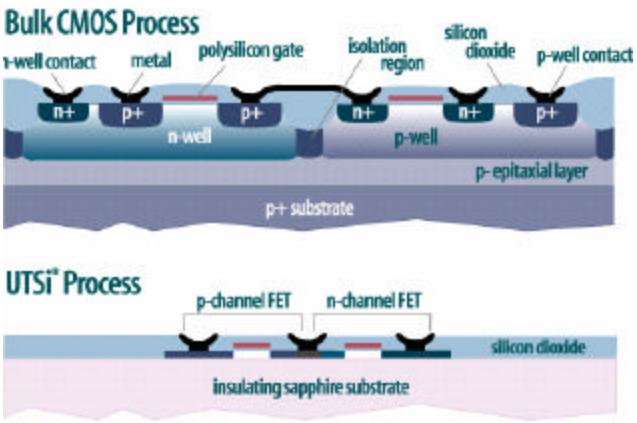

Figure 1. Cross-sectional view of bulk Si CMOS (top) and UTSi CMOS (bottom) showing reduced complexity and parasitics thanks to UTSi CMOS' sapphire substrate.

Radiation Performance

Radiation effects include total ionising dose, TID, and single event effects, SEE. Single event latchup is impossible in UTSi CMOS due to its dielectric isolation structure. UTSi CMOS is also very immune to single event upset, SEU, due to the 100 nm thick Si layer.

Figure 2, shows the radiation pre-radiation and post-radiation response of N channel transistors after 100 krad of Co^{60} radiation. As can be seen, the fully depleted transistor shows no evidence of radiation-induced back-channel leakage, since there is no floating back channel.

For the bias condition to enhance threshold voltage shift, less than 50 mV shifts occur.

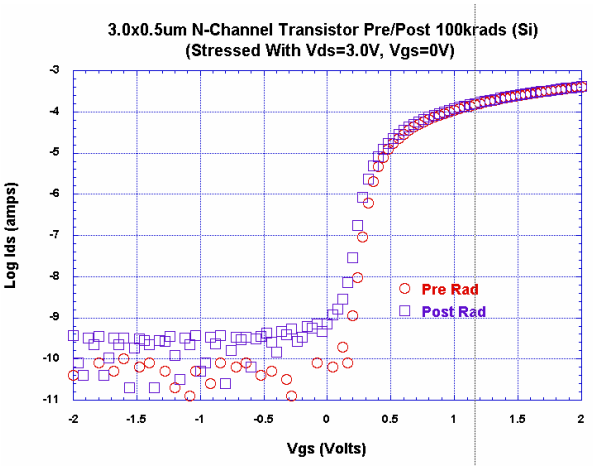

Figure 2. Pre and post radiation response of NMOS transistor after 100 krad Co^{60} radiation.

RF Performance

RF performance of UTSi CMOS devices is discussed. Since all devices made are in UTSi silicon on sapphire, their radiation performance is as discussed above. The following sections will discuss performance of UTSi CMOS based devices, many of which have been delivered to satellite customers.

Mixers

Linearity of RF mixers has become a critical parameter to accommodate modern digital modulation schemes such as CDMA. Due to the inherent linearity of the fully depleted UTSi transistors, extremely high linearity can be achieved. Figure 3 shows the IP3 of passive mixers made with UTSi FETQUAD devices.IIP3 values in excess of +30 dBm are achieved in the configuration of Figure3.

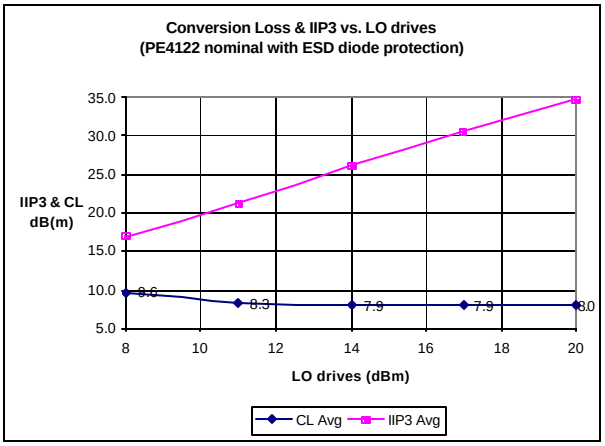

Figure 3. IIP3 vs. input LO power for UTSi FETQUAD based mixer, showing linearity > +30 dBm.

RF Switches

RF switches are increasing in importance due to new architectures and duplexing techniques. The two key parameters, isolation and insertion loss, can be traded for each other to some degree. A full line of RF switches operating from 1 to 6 GHz with compression points from 10 to 35 dBm. Typical insertion loss is 0.5 dB at 2 GHz with isolation of 35 dB. Since these basic switches can be integrated with high Q passives and digital control logic, they can be integrated into highly complex microwave switching matrices, as shown in Figure 4.

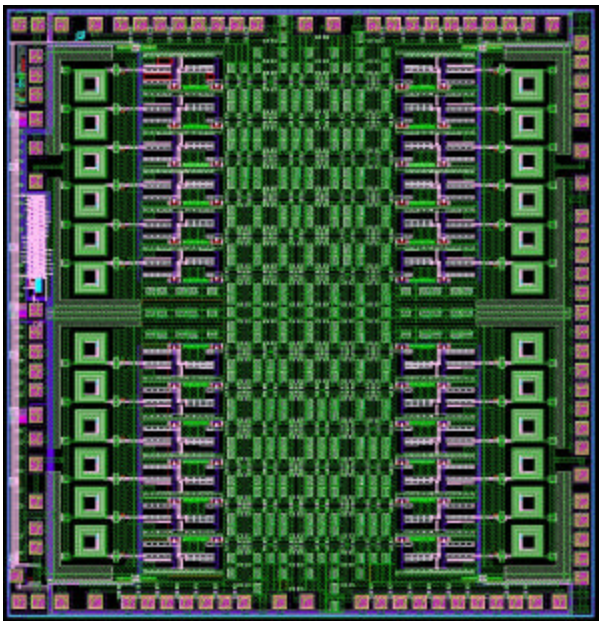

Figure 4. Photomicrograph of 4x6 microwave matrix switch, MSM, containing 24 SPDT non-reflective switches, four 6:1 Wilkinson power dividers and a serial-parallel digital interface. The chip is 3.5x3.5 mm.

Phase Locked Loops

PLLs require combination of RF, analog and digital circuitry. Overall performance is usually measured by observing the phase noise plot. Peregrine has delivered high performance PLL chips to virtually all satellite manufacturers at 2.2 GHz and 3.0 GHz, called the PE9601 and PE9601, respectively. Their detailed characteristics are available on the web.[see www.peregrine-semi.com] Figure 5 shows a typical output for these parts, with excellent phase noise of better than -85 dBc/Hz at 1 kHz offset. Figure 5 also shows the pin-compatible Qualcomm QC 3236 which has more than 10 dB higher phase noise over most of the frequency band.

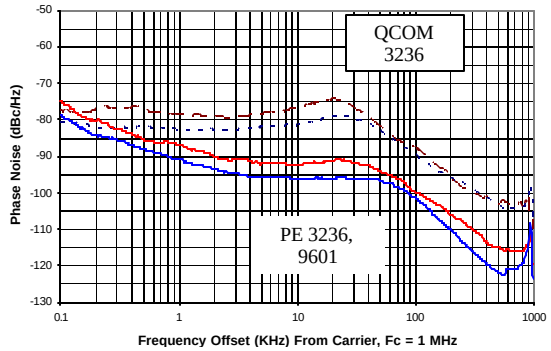

Figure 5. Phase noise plot of PE 9601 2.2 GHz PLL.

These PLLs offer direct access to the accumulators, enabling delta-sigma modulation. This advanced form of fractional-N architecture permits even lower phase noise at very small step sizes. In Figure 6 we show a PE9701 with a DSM modulation, enabling -93 dBc/Hz at 10 kHz offset while having a frequency variation of 57 Hz.

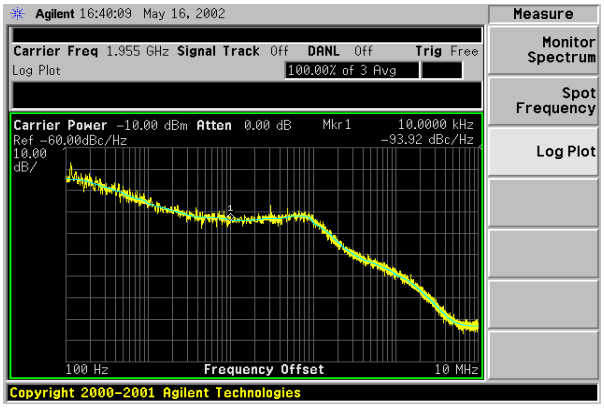

Figure 6. Delta-sigma modulated (DSM) PE 9601 showing -93 dBc/Hz at 10 kHz offset. Modulation scheme allows 57 Hz step resolution.

A key advantage of these PLLs over the bipolar Si type (such as Qualcomm or Plessey) is that the CMOS on sapphire is virtually SEU immune. Proprietary testing has shown that the PLLs have unmeasurable upset rates of the control logic.

Passive devices

The most important passive device for RF integration with CMOS devices is a high Q-factor inductor. In order to match a 50 ohm system to the input of a MOSFET, the inductor is required to match the capacitive input of the MOSFET. Q-factor is limited by the substrate resistivity of bulk CMOS, which in turn has limited the usefulness of CMOS in true RF analog applications. In Figure 7, we show a direct comparison of inductors made on bulk Si and on sapphire (the substrate for UTSi CMOS). The bulk Si inductor is from the design library of Taiwan Semiconductor and is made on top of several microns of silicon dioxide (the core process is a 5 level metal process).

The UTSi inductor is made in 3 um thick Al on top of 2 microns of silicon dioxide on the sapphire substrate. As can be seen, the Q factor at 2 GHz on sapphire is about 20 on sapphire while it is less than 5 on bulk Si. Also, the self-resonant-frequency, SRF, is only about 3 GHz on bulk Si due to capacitance to the substrate. The SRF on sapphire is about 8 GHz and can be made higher with layout changes.

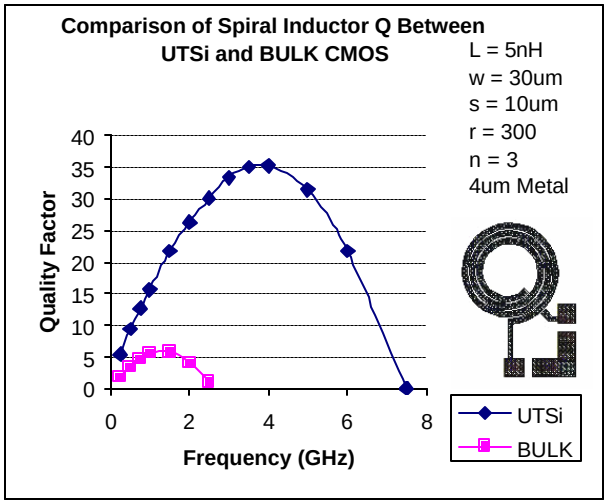

Figure 7. Comparison of 5 nH inductors fabricated on bulk Si and on sapphire (simulated result) showing higher Q-factor and self resonant frequency.

A unique concept is being developed by Peregrine called Control Logic and Integrated Passives, or CLIP. In this concept, a base sapphire device is built which contains control logic such as current sources, digital logic and EEPROM along with passive networks for matching and filtering. This offers substantial weight and cost savings and can be applied to receivers, power amplifiers and T/R modules for phased array antennae.

EEPROM

A key element in integrated circuits is non volatile memory, of which EEPROM is the most common. It is especially useful for enabling modification of programming or analog trimming after the system or chip has been partially designed. It is also useful for minimizing inventory since a single IC design can be modified by storing adjustment coefficients, as is commonly done in temperature compensated crystal oscillators, TCXO's.

Peregrine has invented a unique EEPROM cell that can be integrated with any UTSi CMOS device. The first such device is the PE 9722, which is a serial load PLL with programming stored in embedded EEPROM. This

product eliminates the need for a controller ASIC to set the frequency of the PLL.

Figure 8(a) shows the top view of the EEPROM cell and 8(b) shows a cross-sectional view. The unique writing and erasing mechanism is shown in Figure 8(b). Unlike traditional EEPROM cells, which write with electrons and are erased by removal of electrons, the Peregrine PlusCell™ writes with electrons and erases by injecting holes. Hence, there is no over-erase problem and any decay in stored charge cannot convert a "1" into a "0".

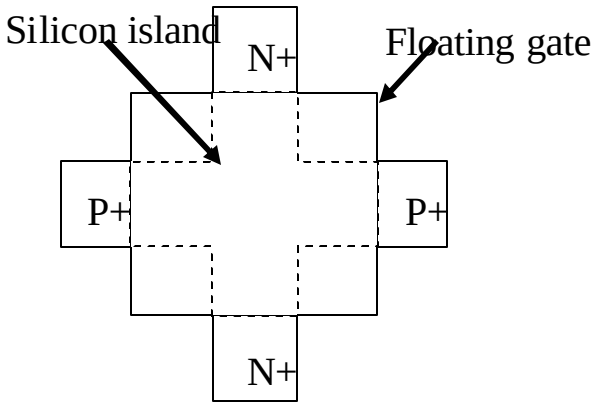

Figure 8(a). Top view of EEPROM cell on UTSi CMOS. Electrons are injected by the PMOS device and holes are injected by the NMOS device.

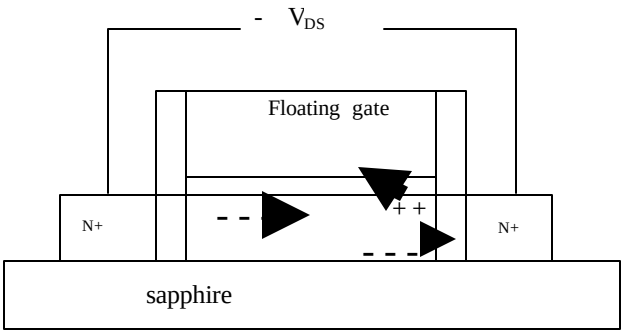

Figure 8(b). Cross-sectional view of EEPROM cell showing writing mechanism of the NMOS device injecting holes. Using the orthogonally-place PMOS device would inject electrons.

The EEPROM cell has been tested to 100,000 write cycles, has over 100 years retention time. It has also been irradiated to more than 100 krad Co^{60} and still exceeds storage read margin.
Since routing of high voltage for programming is done over sapphire, rather than over Si as in bulk Si, the EEPROM cell has no effect on any RF, analog or digital circuit functions.

Other applications

Since sapphire is transparent from near UV to far IR, UTSi CMOS has been applied to make high performance parallel optical interconnects. Figure 9 shows module which is a 10 Gbps bi-directional (transmit and receive) parallel optical module made on UTSi CMOS.

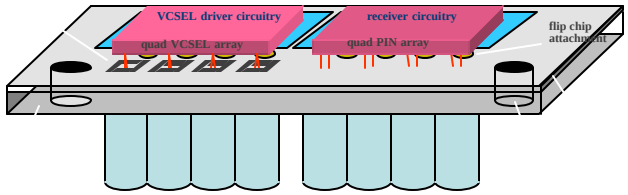

Figure 9. Flipped Optical Chips on UTSi, FOCUTS, consists of VCSEL arrays and photodetector arrays flip chip attached to their respective driver circuits. The light enters and exits through the transparent substrate, resulting in a monolithic parallel optical link

By flip-chipping VCSEL lasers and P-i-N photodetectors onto circuits designed to drive them (laser drivers and TIA/LA, respectively), virtually all bonding parasitics and alignment issues are resolved. Laser cutting of alignment holes in the sapphire substrate provide a mechanical self-alignment feature which ensures reliable optical coupling.

A fully-packaged assembly, called FOCUTSpak, has been completed. The assembly is environmentally sealed and can be completed in a mil/aero/space version. Operation to 3.125 Gbps has been demonstrated and 10 gbps is expected when 0.25 um technology is available.

Future capabilities & conclusion

Because UTSi CMOS is fundamentally a CMOS technology, it scales in speed and power with gate length. Peregrine has completed a 0.25 um fab plant expansion which enables frequency of operation to extend to Ku band.
In conclusion, Peregrine offers a radiation hard, SEU hard commercial CMOS on sapphire technology for use in RF, analog and mixed signal space applications where size, weight, performance and power consumption are critical.