A New Non-Quasi-Static Non-linear MOSFET Model Based on Physical Analysis

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***Abstract* — This paper presents a novel approach to the physical modelling of Si based sub-micron MOSFETs. The model is based on a set of simplified transport equations for the conducting channel in a MOSFET. These equations incorporate non-quasi-static (NQS) effects due to the inclusion of time derivatives, and describe the semiconductor dynamics in terms of coupled particle and displacement currents leading to a description in terms of a relatively small number of nonlinear differential equations. Thus, internal device behaviour can be accurately modelled. A new method of modelling the charge density in the channel has also been developed in the form of a single expression that describes the charge under the Gate for any biasing conditions. The new model has a low empirical content, and is fully continuous over all operating regions.**

I. INTRODUCTION

Many present day simulation tools, such as SPICE, rely on equivalent circuit models. These models originate from the fundamental physical equations but end up having a high empirical content. Models of this kind are fast and simple to use but have many limitations and potential inconsistencies. For instance, very high frequency operation requires consideration of the temporal relaxation of the inversion and depletion charges. The majority of the MOSFET models used in SPICE are based on the quasi-static assumption, in which an instantaneous charging of the inversion layer is assumed [1]. As clock speeds increase into the GHz region, however, non-quasi-static (NQS) effects begin to have a major impact on device behaviour and the transistor cannot be accurately modelled by making such assumptions.

A common practice in device modelling is to use a 2-region model, that is, to use one set of equations to govern the operation of the device under one regime of biasing conditions, and to use another set of equations to model the operation in another regime [2]-[4]. While such models have the ability to describe device operation reasonably well, discontinuities can result at the boundary points leading to simulation errors. Another common modelling technique is to use a table look-up model [5]. These models store information such as the drain current in tables for a large range of biases. However, the information is only valid for one set of physical parameters. Thus, changing the channel length, for instance, makes the entire stored information base inapplicable. Surface potential based models, e.g. [6], require complex, implicit, iterative calculations to solve for the surface potentials in the channel and are too complex and time-consuming for typical circuit-level simulation.

This paper provides a new NQS, non-linear, explicit, physical MOSFET model. The created model is robust, accurate, has a low empirical content and is computationally efficient. A new expression is developed to describe the charge density in the MOSFET channel in terms of the actual channel voltage and not the surface potentials. This expression is fully continuous for all operating conditions eliminating any potential for discontinuities. The DC and AC characteristics of the model have been simulated in C-code and in Agilent's Advanced Design System (ADS), using symbolically defined devices, and the DC results are compared to experimental results for a MOSFET with a channel length of 0.18 μm and a width of 100 μm. The dynamic voltage variations at various points along the channel are shown for an AC simulation. The dynamic load line is also shown to prove the model's ability to switch between the subthreshold and strong inversion regimes. Finally, a one-tone power measurement test is simulated and compared to experimental measurements to show the predictive capabilities of the model in strongly nonlinear operation.

II. MODEL FORMULATION

The proposed model originates from the following set of simplified transport equations for the conducting channel of a MOSFET:

$$i_{DS}(y,t) = \underline{\mu}.w.Q_n(y,t).\frac{\partial v(y,t)}{\partial y} \tag{1}$$

$$w\frac{\partial Q_n(y,t)}{\partial t} = -\frac{\partial i_{DS}(y,t)}{\partial y} \tag{2}$$

where y is the position in the channel [0,L], $i_{DS}(y,t)$ is the channel current, v(y,t) is the channel voltage, $Q_n(y,t)$ is the channel charge and w is the device width. $\underline{\mu}$ is a field dependent mobility term that saturates for high electric fields, and is given by

$$\underline{\mu} = \frac{\mu}{1 + \frac{\mu}{v_{sat}}\left|\frac{\partial v(y,t)}{\partial y}\right|} \tag{3}$$

where v_{sat} is the velocity saturation speed for electrons ~ $0.8x10^5$ m/s, and μ is the surface mobility of the electrons in the channel ~ 0.06 $m^2/(V\text{-}s)$. These equations provide a charge conservative model, which incorporates the NQS effects due to the presence of the time derivative in equation (2). Therefore, the only requirement left is to provide a fully continuous charge expression that is dependent on both the Gate voltage and the channel voltage.

Standard analysis of the charge under the Gate in a MOSFET stipulates that when the Drain voltage exceeds the saturation voltage (= $(V_G\text{-}V_T)$, where V_G is the Gate voltage and V_T is the threshold voltage), the channel charge in the saturation region is zero. Using such an approximation with equation (1) above wrongly predicts that the current will go to zero when in fact it reaches its saturating value. To analyse in detail the charge in the channel we employed the physical simulator Athena, (used to create the physical device), and Atlas, (used to simulate applied biases on the device), both products of Silvaco Corp.. Numerous simulations with various biases applied to the terminals of typical MOSFETs were carried out. These simulations showed that the electron concentration along the surface of the semiconductor did not decrease below the acceptor concentration level, unless the device was biased deep into saturation. Such a finding was quite surprising as numerous references, [7]-[9], state that for channel voltages greater than the saturation voltage the inversion layer should not be strongly inverted. The results from Silvaco gave contrary results, and showed that the charge density (calculated by integrating the electron concentration from the substrate to the surface) actually saturates to a minimum value with an increasing Drain voltage. Fig. 1 shows typical results from a Silvaco simulation. The charge density versus channel position is shown for an increasing Drain voltage for a device with L=0.35 μm, t_{ox}=10 nm and V_{GS}=3.0 V. The Drain voltage is increased in steps of 0.25 V from 0.25 V up to 1.5 V.

To model this charge-dependence the authors formulated an expression based on the charge expression used in metal oxide semiconductor capacitors (MOS-Cs). The 2-terminal MOS-C expression was adapted, however, to allow for a reduction in charge due to a channel voltage, as would be the case in a 4-terminal MOSFET. The new charge expression is given by

$$Q_n(y,t) = C_{ox}\left(V_{Geff}(t) - \frac{v(y,t)V_{Geff}(t)}{\alpha v(y,t) + V_{Geff}(t)}\right) \quad (4)$$

where C_{ox} is the oxide capacitance per unit area, $V_{Geff}(t)$ is an effective Gate voltage that provides a continuous expression for the charge from weak inversion into strong inversion [10], and α is an empirical expression which was chosen to empirically fit (4) to the results in Fig. 1. The threshold voltage of the device, which is incorporated into the $V_{Geff}(t)$ expression, was also chosen empirically. For Gate voltages less than the threshold voltage $V_{Geff}(t)$ decreases exponentially, as does the second term in (4). Thus, (4) is fully continuous between

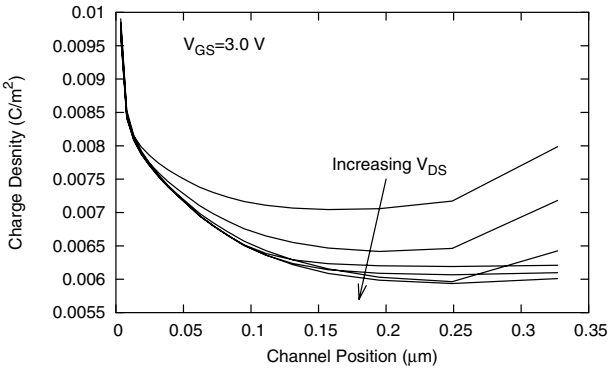

Fig. 1. Charge density versus channel position. As the Drain voltage is increased the charge density saturates to a minimum value.

the subthreshold and strong inversion regimes. For Drain voltages larger than $V_G\text{-}V_T$ the second term in (4) saturates to $V_{Geff}(t)/\alpha$. Equation (4) therefore saturates to a minimum value as the Drain voltage increases. Thus, (4) is also fully continuous for any Drain voltage. Equation (4) can now be substituted into equations (1) and (2) to complete the model equations.

III. DC AND AC SIMULATIONS

For DC simulations the time derivative in equation (2) is set to zero. This implies that the rate of change of the current along the channel is zero. This is as expected since there is no charge build up and the current entering must be equal to the current exiting. After the necessary spatial differentiation is performed we are left with the following nonlinear differential equation:

$$\begin{aligned} &\frac{\mu}{1+\frac{\mu}{v_{sat}}\left|\frac{dv(y)}{dy}\right|} wC_{ox}\left(V_{Geff} - \frac{v(y)V_{Geff}}{\alpha v(y)+V_{Geff}}\right)\frac{d^2v(y)}{dy^2} \\ &-\frac{\mu}{\left(1+\frac{\mu}{v_{sat}}\left|\frac{dv(y)}{dy}\right|\right)^2} wC_{ox}\left(V_{Geff} - \frac{v(y)V_{Geff}}{\alpha v(y)+V_{Geff}}\right)\frac{\mu}{v_{sat}}\frac{dv(y)}{dy}\frac{d^2v(y)}{dy^2} \\ &-\frac{\mu}{1+\frac{\mu}{v_{sat}}\left|\frac{dv(y)}{dy}\right|} wC_{ox}\left(\frac{V_{Geff}}{\alpha v(y)+V_{Geff}}\right)^2\left(\frac{dv(y)}{dy}\right)^2 = 0 \end{aligned} \quad (5)$$

This equation is also a boundary value problem, as we know the voltages at the positions y=0 and y=L i.e. the Source and Drain voltages respectively. The channel length, L, is divided up into N segments, each segment being of length h=L/N. To solve for the voltages at the N-1 nodes between each segment, the above derivatives were replaced with central differences equations and the resulting N-1 nonlinear algebraic equations were solved using Newton's method iteratively. A straight-line voltage distribution is used as an initial guess. Simulations require 3-8 iterations to converge depending on the choice of DC bias. The solution yields the voltage distribution along the channel of the MOSFET. Furthermore, the charge distribution and the current distribution along the channel are also obtainable from

these results.

For the AC solution equation (2) is solved. This equation relates the particle current to the displacement current in the channel. The change in current along the channel is attributed to the capacitive current across the oxide (ignoring bulk currents). This equation ensures current and charge continuity. A circuit diagram that is described by (2) is shown in Fig. 2.

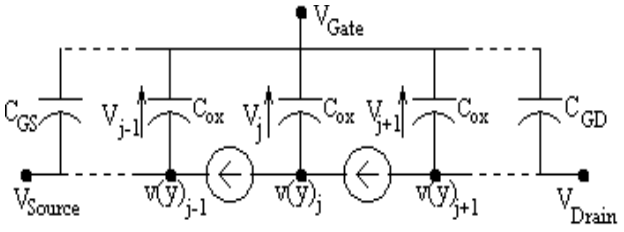

Fig. 2. Circuit diagram for the MOSFET channel. C_{GS} and C_{GD} are included to model the Gate-Source and Gate-Drain overlap capacitances respectively. The current sources have values as defined by equation (1).

The displacement current can also be expressed by the following expression:

$$w\frac{\partial Q_n(y,t)}{\partial t} = whC_{ox}\frac{dV_j(t)}{dt} \qquad (6)$$

where $V_j(t)$ is the voltage across the oxide between the Gate and the $v(y,t)_j$ node. Equation (6) is then substituted into (2). This yields a time-dependent differential equation for the voltage between the Gate and each particular channel node.

This model is then incorporated into a simple amplifier circuit with bias and matching networks. The voltages across the oxide are solved for in conjunction with the other state variable values using the Improved Euler Method, where the DC solution provides the initial conditions for the AC simulation. The channel node voltages are subsequently calculated using $v(y,t)_j=V_G(t)-V_j(t)$. To test the validity of the model, simulation results for the DC characteristic were compared to experimental results for a MOSFET. Also, a one-tone power-sweep simulation was performed and the results were compared to experimental measurements, as shown in the next section.

IV. Results

Fig. 3 shows the voltage and charge distributions along the channel of a MOSFET of length 0.18 µm with V_{GS}=3.0 V, V_{DS}=3.0 V and V_{SB}=0 V. The applied bias places the transistor deep into saturation. The figure shows simulations for N=50 and N=5. As can be seen, the use of just 4 internal node points can accurately describe the distributions in the channel just as accurately as 49 internal node points. Fig. 3 also shows that the charge along the channel is continuous and does not go to zero towards the drain end, as is the case in conventional models. A plot of the current distribution, which has been omitted to save space, confirms that the current along the channel is constant.

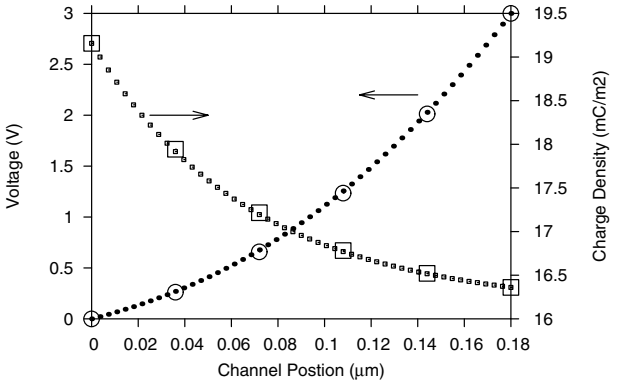

Fig. 3. Voltage and charge density distributions along the channel for V_{GS}=3 V and V_{DS}=3 V. Larger squares and circles are for N=5 and smaller squares and circles are for N=50. α=6 and V_T=0.45 V.

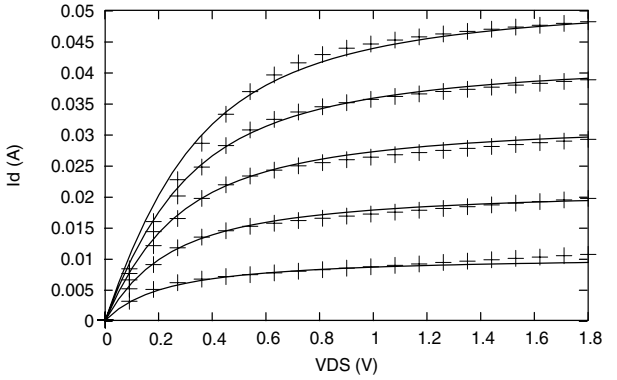

Fig. 4. Simulated (—) and measured (+) current characteristics for a MOSFET with a Gate length of 0.18 µm and a width of 100 µm. Gate voltages are from 0.8 V up to 1.6 V, increasing in steps of 0.2 V.

To confirm the accuracy of the model the DC characteristic was simulated (incorporating Source and Drain parasitic resistances) and the results were compared to experimental results for a device with L=0.18 µm and w=100 µm. Fig. 4 shows that the new model compares well with experimental results supporting the validity of the charge density expression developed earlier.

Fig. 5 shows the dynamic voltage variation in the MOSFET channel with N=5 for an input amplitude of 1.0 V at 2 GHz, and with a DC biasing of V_{GS}=2.0 V and V_{DS}=2.0 V. The plot shows the voltages at the points L/5, 2L/5, 3L/5, 4L/5 and at the Drain. Such voltage plots are unavailable with other circuit-level modelling approaches.

A common gauge used to assess the large-signal performance of an amplifier is to plot the dynamic load line. The dynamic load line for an input signal with an amplitude of 1.5 V and with a DC biasing of V_{GS}=1.0 V and V_{DS}=1.0 V, over 5 periods of operation, is shown in Fig. 6. From this graph the nonlinearities of the model are clearly evident. The 3 V peak-to-peak input signal only produces a 1.7 V peak-to-peak signal at the Drain. Also, for Gate voltages less than the threshold voltage the current is seen to exponentially decay towards zero.

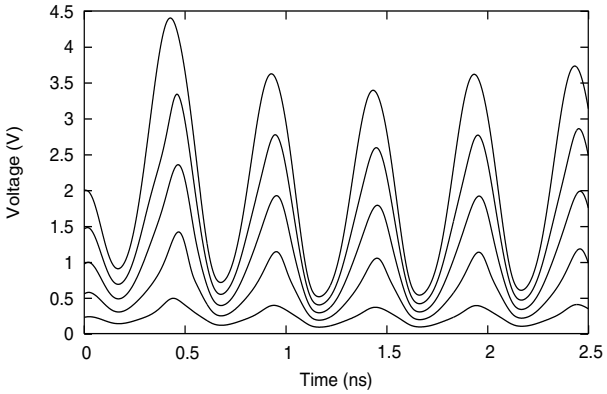

Fig. 5. Voltage variations along channel for an input amplitude of 1 V. The lowest plot is for the position L/5 and the highest plot is the Drain voltage variation.

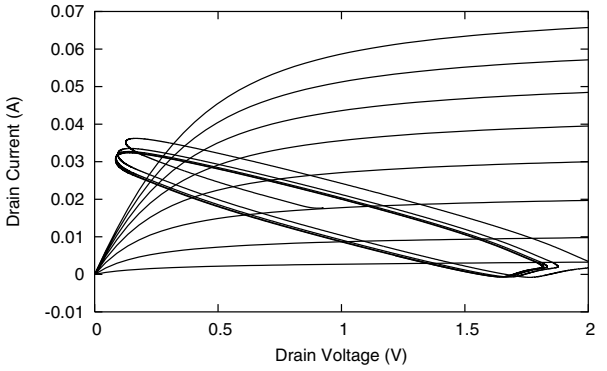

Fig. 6. Dynamic load line for an input amplitude of 1.5 V and with a DC biasing of V_{GS}=1.0 V and V_{DS}=1.0 V. DC characteristic shows currents for V_{GS}=0.6 V up to 2.0 V in steps of 0.2 V.

To further validate the model single-tone power sweep simulations were carried out and compared to experimental results. Fig. 7 shows the fundamental, second and third harmonics at the output of the amplifier for an input signal at a frequency of 2 GHz. As can be seen the agreement between the simulation results and the experimental measurements are quite good. The saturating output power for the fundamental tone is a classic characteristic for any amplifier and this is modeled quite accurately here.

V. Conclusion

A new nonlinear physics based MOSFET model has been developed and simulated in the C-code and ADS environments and compared to experimental measurements. The model incorporates a new fully continuous charge modelling technique that is dependent on the channel voltage and not the surface potentials. Good agreement is shown for the DC characteristic curve. The internal voltage and charge distributions, which cannot be shown by conventional simulators, are also shown. The single tone power measurement simulation also verifies the robustness of the model and its ability to predict the nonlinear Drain current accurately.

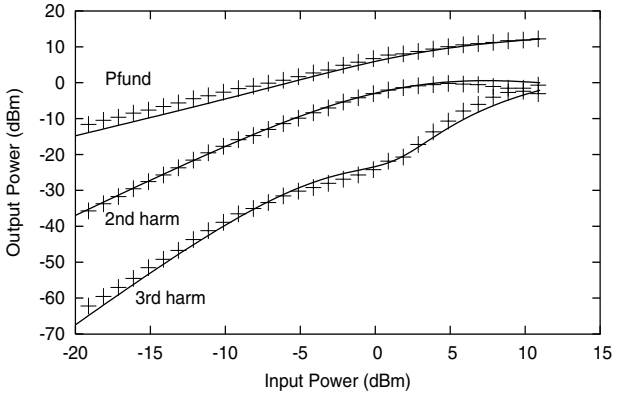

Fig. 7. Simulated (—) and measured (+) output harmonics against swept input power for one-tone power measurements at V_{GS}=0.6 V and V_{DS}=1.6 V.

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