

A Low Cost SMT Integrated Frequency Doubler and Power Amplifier for 30GHz DBS Uplink Applications

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Abstract – A SMT (Surface Mount Technology) MMIC (Monolithic Microwave Integrated Circuit) frequency multiplier (x2) and power amplifier has been designed for DBS (Direct Broadcast Satellite) and other commercial applications. Using PHEMT technology this MMIC takes a 15GHz input signal and passes it through a harmonic frequency doubler and then through three stages of power amplification at 30GHz. This MMIC provides an output power of 21dBm, fundamental suppression of 45dBc and is stable across all voltages and temperatures. This single MMIC SMT solution frequency multiplier and power amplifier is unique compared to any known or published data.

I. Introduction

One of the problems with DBS (Direct Broadcast Satellite) is returning data from the consumer to the provider. Return information requires only a low data rate and is usually conveyed by modem or voice over land line. Numerous return data items such as pay-per-view, billing, configuration changes, local programming orientation, gaming, etc. could make DBS more effective if transparently done. [6-10]

One solution being implemented in Europe and Asia is to use a 30 GHz uplink frequency for low data rate return. The system uses the same antenna and cable with only additional TV top box and LNB changes. Uplink is carried on the coax just above the receive band (2.5 GHz) then multiplied and amplified for transmit at 30 GHz. A simple representation is shown in Figure 1.

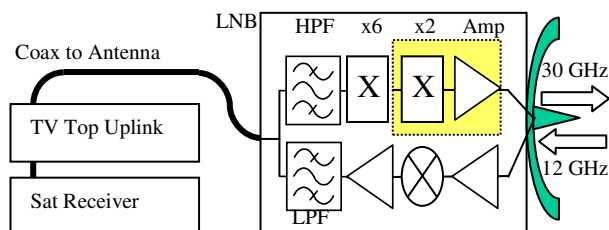


Figure 1. DBS 30 GHz uplink system

This paper focuses on the 15GHz to 30 GHz frequency multiplier and 100mW power amplifier that are integrated together to form the last stage in the uplink. The MMIC had to be SMT (Surface Mount Technology) compatible, low cost, and high performance. The paper being proposed poses the numerous challenges faced and innovative solutions used to develop this high volume mmW product.

II. MMIC Process and CAD Tools

The 6-inch wafer-based mm-wave PHEMT process uses a 0.15 μ m gate, and has an f_T of 85GHz. The wafer material is selected for high power and breakdown with some compromises for noise. A Ti/Pt/Au T-gate is used for low input resistance and high reliability. This PHEMT process is designed to operate with a peak drain voltage up to 5.5V, and is equipped with passive components which include a 150 Ω/\square bulk resistor, 50 Ω/\square Thin-film resistor, a 0.39 fF/ μ m² MIM capacitor, a backside via process, and two metal layers for transmission lines. [2, 4-5]

The process includes 100% on-wafer MMIC test and verification of performance. Passive structures were simulated using Agilent's ADS and Momentum EM software.

III. Frequency Doubler and Amplifier Design

A simplified schematic of the frequency doubler and amplifier (QMMP-6130) is shown in Figure 2. The one-stage frequency doubler relies on the non-linear behavior of the FET to produce the doubled signal at the output. A high-pass filter at the input shorts any reflected 2nd harmonic signal to ground. Theoretically, this filter does not affect the 15GHz excitation signal. The input also consists of matching components tuned for 15GHz. An additional LC-filter is included at the input for stability. The doubler is operated at pinchoff to create a half-wave conduction angle ideal for generation of the 2nd harmonic. When the MMIC is operated at cooler temperatures (-20C to -40C) the k-factor of the doubler degrades twice as fast as an amplifier operated in the linear region. In order to

ensure stability at all temperatures and biases, the LC-filter is designed to resonate at 30GHz. The filter looks like an open at 30GHz. Since a high reactance is presented to the input of the doubler, S21 drops at 30GHz. Below 30GHz the filter looks capacitive, and has little effect on the 15GHz signal. The shunt inductor at the output short circuits the drain at the fundamental, and passes the 2nd harmonic through. [3]

A medium power amplifier follows the frequency doubler, and includes three cascaded stages designed to deliver maximum power and stable gain at 30GHz. The interstage matches are optimized for narrowband gain and power at 30GHz.

Biased to $V_{ds} = 4V$ the frequency doubler and power amplifier are designed to provide 21dBm of output power at 30GHz and 16.5 to 17dB of large signal gain. The fundamental suppression of the high and low pass filter network is 45dBc.

The layout is efficient since this is a high volume application where cost is paramount. The prototype layout is shown in Figure 3 with the final production layout approximately 20% smaller. The layout of the MMIC is designed with yield and reliability in mind including bond pad size, and automated assembly handling.

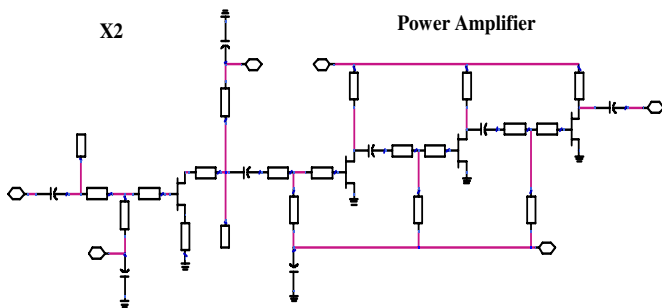


Figure 2. Simplified circuit

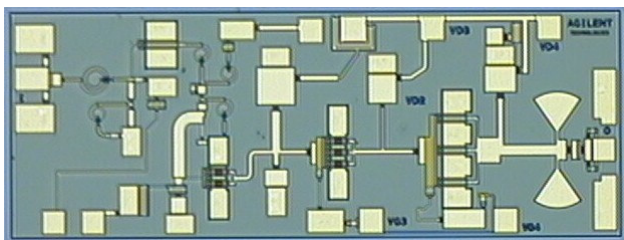


Figure 3. MMIC Photograph
Die size = 1920 x 760 micro-meters

IV. Packaging

The package is 5x5mm in dimension and has full surface mount capability. It takes into account the parasitics involved with routing a high-frequency signal up and through the substrate. Built with Rogers 4350 material, the package has a metal backside, making it fully compatible with modern low cost, high volume assembly and test in panel form. [2, 5]

The design of the input and output backside coplanar to topside micro-strip transitions was completed using EEsof's three-dimensional simulation tool, HFSS. With extensive modeling the package I/Os are capable of maintaining better than 15 dB of return loss up to 40 GHz. Compensation for bondwire inductance is included in the package micro-strip launch.

The MMIC is assembled in the package using automated bonders while still in panel form. Lids are then epoxy attached forming an air cavity above the device for maximum performance. Last, the panel is 100% tested at microwave frequencies to ensure performance for the customer.

Figure 4 shows a 3 dimensional representation and 2 dimensional side view of the package and MMIC. Figure 5 shows the MMIC in the package as assembled. The package design was developed at Agilent for use up to 60 GHz [1].

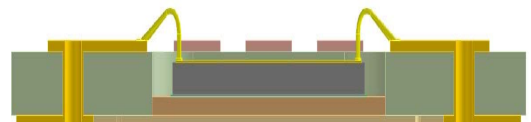
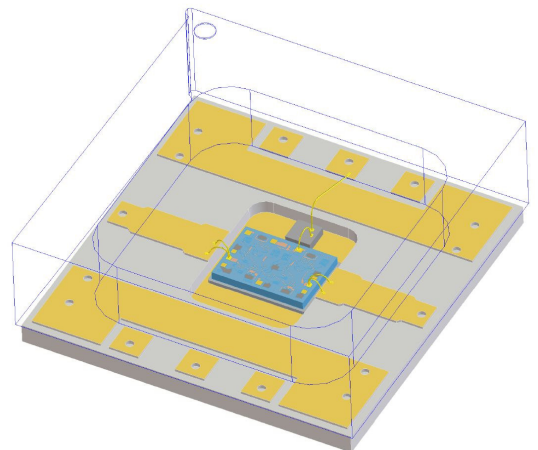


Figure 4. DC-40 GHz low cost package

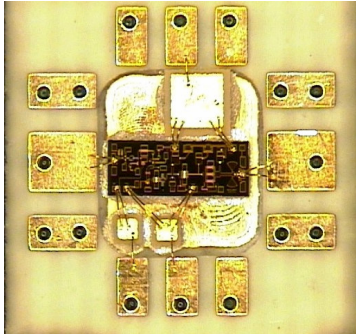


Figure 5. QMMP-6130 as assembled

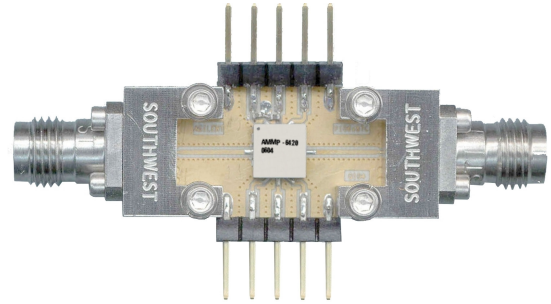


Figure 7. Evaluation module

V. Measured Results

Large signal and small signal measurements were taken on the QMMP-6130. A HP8565E spectrum analyzer and HP83650A power source were used to take harmonic measurements and a HP8510C was used to take all small signal measurements. All measurements described in this section were taken at $V_{ds}=4V$, $V_{g1}=-1.2V$ and $V_{g2}=-0.5V$. Figure 6 shows the pin configuration for the RF and bias lines. The evaluation board used in these measurements is made out of the Rogers 4350 material, and is shown in Figure 7.

It is important to note that the QMMP-6130 is designed for the input power level to drive the frequency multiplier into saturation. This requires the input power to be contained in a narrow range, for this part 0 to +5 dBm. The resultant output power range is approximately +17 to 21 dBm. There is no small signal gain value for this part as it must be in large signal compression (with about 17 dB of gain) to operate.

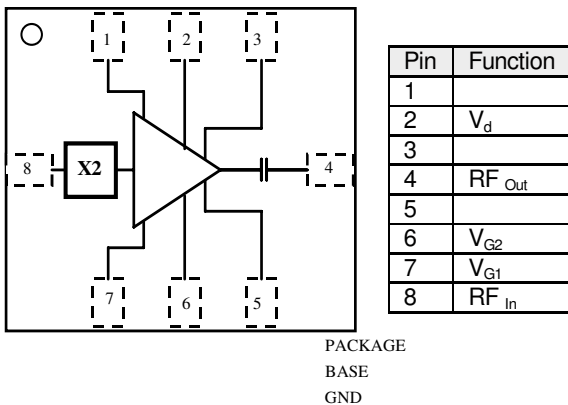


Figure 6. RF and DC pin configuration

Figures 8 and 9 describe the large signal response of the QMMP-6130 MMIC. At 5dBm (15GHz) input power, the output power is 21.10dBm at 30GHz. 2H-1H, or the fundamental suppression is approximately 45dBc. Also shown are 1H, 2H and 3H vs. frequency (see figure 9). The 2nd harmonic signal peaks slightly around 30.5GHz and the fundamental and 3rd harmonics decrease as frequency increases.

Pin (dBm)	Pout (dBm)	H1 Suppression (dBc)
0.00	16.80	44.50
1.00	18.30	44.70
2.00	19.30	45.60
3.00	20.10	46.60
4.00	20.80	47.70
5.00	21.10	48.70
6.00	21.40	49.00
7.00	21.60	48.90

Figure 8. Output Power and Fundamental Suppression

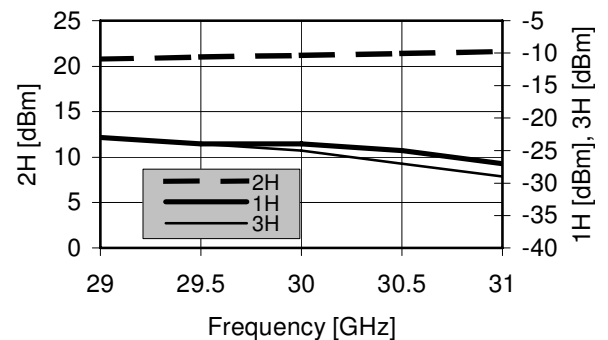


Figure 9. 1H, 2H and 3H Output Power vs. Output Frequency

Figure 10 shows the spectrum of the MMIC where the 15GHz input signal power is 5dBm. The fundamental and 3rd harmonic are far lower than the 2nd harmonic, and there are no spurs or signs of oscillation present. In fact, the spectrum, at -40c, is clean for a wide range of Vds values (1.8 to 4.5V) at all power levels. Figure 11 shows the input and output returnloss of the MMIC. The output is matched from 20GHz to 33GHz and the input is matched close to 15GHz.

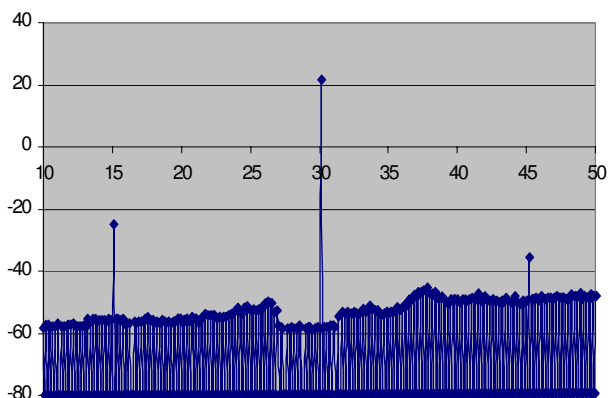


Figure 10. Spectrum $P_{in}=5dBm$ at 15GHz

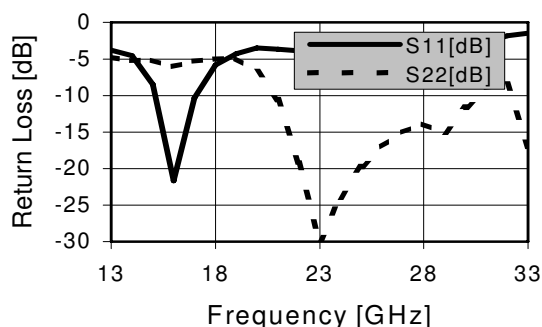


Figure 11. S_{11} and S_{22} of the QMMP-6130

VI. Conclusion

An SMT integrated frequency doubler and power amplifier for 30GHz commercial communications systems has been designed, fabricated and characterized. With an input power level of 5dBm (15GHz), this MMIC provides 21dBm of output power at 30GHz. The fundamental suppression is 45dBc and the QMMP-6130 is stable across a wide range of Vds values at all power levels and temperatures down to -40c. It is designed for low cost utilizing an innovative

SMT package and a volume 6" wafer fabrication facility. The MMIC provides a cost effective alternative to discrete FET designs and chip-and-wire hybrid MMICs. This frequency doubler and power amplifier MMIC provides the best combination of cost, performance, and ease of application than any known product advertised or published.

The authors wish to thank all the people that made this product. This includes: Agilent Technologies, San Jose, California, USA: Hue B. Tran, Michael Vice, Sushil Kumar, and Kohei Fujii

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