A 4.8-6 GHz IEEE 802.11a WLAN SiGe-Bipolar Power Amplifier with On-chip Output Matching

Winfried Bakalski[1], Andriy Vasylyev[2], Werner Simbürger[1], Marcus Käll[1], Alfons Schmid[1], Krzysztof Kitlinski[1]

[1] Infineon Technologies AG, P.O. Box 80 09 49, 81609 Munich,
Germany, Tel. +49 89 234 27961, Winfried.Bakalski@infineon.com
[2]Brandenburg University of Technology Cottbus, Chair of Circuit Design, Cottbus, Germany

***Abstract*— A fully integrated 4.8 - 6 GHz Wireless LAN SiGe-bipolar power amplifier chip requiring no external components was realized using the small die size of only 1 x 0.9 mm^2. At 1 V to 2.4 V, the maximum output power level is 19 dBm (22 % PAE) to 26.3 dBm (28.5 % PAE) at 5.25 GHz with a maximum small signal gain of 33 dB. The maximum average output power for a maximum 3 % Error Vector Magnitude (EVM) is 16 dBm. The PA survives a VSWR of 50.**

I. Introduction

Wireless LAN is one of the increasing high-volume production markets. First found as network adapter only, the next step will be the integration in mobile phones and other handheld applications, also with reduced power supply voltage levels. Furthermore more data throughput at low price is desired, so that additional IEEE 802.11a functions in the 5 GHz band for WLAN chipsets have become available [1]. Today, wireless LAN for 5 GHz IEEE 802.11a is dominated by III/V-HBT based power amplifier (PA) solutions with a single-ended topology such as [2]. Linear Power Si and SiGe Amplifiers for the 5 GHz Wireless LAN band have been reported so far in [3], [4], using a single-ended topology and external output matching network. However, a single-ended structure requires a good ground connection, realized by flip-chip or on-chip ground connection [5]. Furthermore the high impedance transformation ratio between the output stage transistor and the 50 Ω load makes it difficult to achieve a low loss match on-chip. Therefore all on-chip output matched efforts such as [6], [7] are differential circuits. There appears a 4:1 load-line impedance benefit for a push-pull combining scheme. Unfortunately all these realized approaches suffered from low linearity [6] or relatively high quiescent currents [7]. This paper presents the first fully on-chip in- and output matched power amplifier for the 5 GHz Wireless LAN band, including broadband balun function. Thus, a high bandwidth is demonstrated, so that the chip can be applied also to cordless phone applications in the 5.8 GHz range.

II. SiGe-Bipolar Technology

The SiGe bipolar technology used in this work is a 0.35 μm, 72 GHz/ 75 GHz (f_t/f_{max}) volume production process [8] with a three layer, 2.8μm thick upper layer Al-metalization. The worst-case collector-base breakdown voltage for the npn HBT is BV_{CB0} = 8 V (typical: 10 V) and the worst-case collector-emitter breakdown voltage is BV_{CE0} = 2.3 V (typical: 2.8 V). Fig. 1 shows the fully integrated PA die (chip size: 1 × 0.9 mm^2).

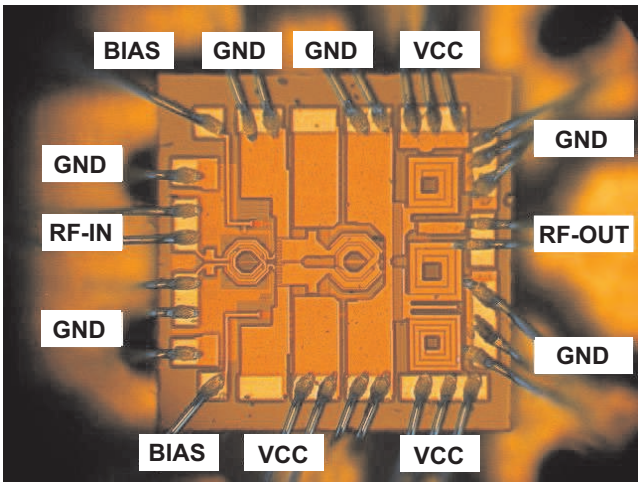

Fig. 1. Die micrograph of the power amplifier (chip size: 1 × 0.9 mm^2).

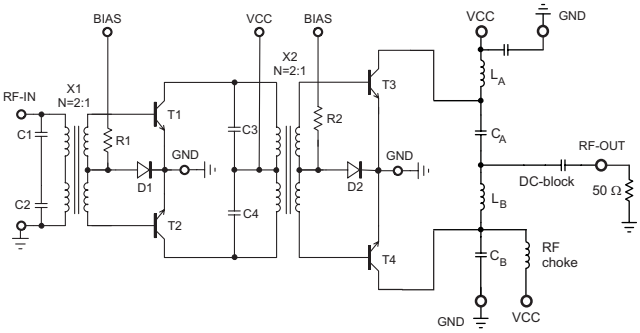

Fig. 2. Simplified circuit diagram of the power amplifier.

III. Circuit Design

Fig. 2 shows the circuit diagram of the power amplifier. At the input, an input transformer X1 is used as BALUN, matching network and low-ohmic bias interconnection. The transformer implies an integrated DC blocking function and an excellent ESD protection for the PA input. It further gives the design freedom of applying differential or single-ended input signals. Functionally, X1 is connected as a parallel resonant device with the input capacitors C1 and C2. Hence, the resonance frequency is tuned to the center frequency. As the differential circuit offers a virtual ground, the center tap of the secondary winding is used to supply the driver stage transistors T1 and T2 with the necessary bias currents. Compared to otherwise necessary bias coils or bias resistors,

the base has a low-ohmic DC connection improving the transistor ruggedness [9] and the noise performance. The turn ratio of X1 is N=2:1. The size is $140 \times 140\,\mu m^2$. The primary winding consists of two turns with a width of $10\,\mu m$ on the top metal layer. The lower two metal layers are used only for crossing purpose to reduce parasitic substrate coupling. The total coupling coefficient is k = 0.55 at 5.3 GHz. In this circuit, the primary center tap was not connected, and the chip is bonded to have a single-ended input. The input transformer X1 feeds the driver stage transistors T1 and T2 with an effective emitter area of $63\,\mu m^2$ each. The transistors are designed in a double emitter, double collector, triple base configuration to reduce the base resistance required for a high current transformation ratio of X1. In the interstage section, X2 is connected as a parallel resonant device with two capacitors C3 and C4 and the transistors T1 and T2, tuned to a resonance frequency of 5.8 GHz. C3 and C4 are connected in antiseries to short the parasitic substrate capacities to the VCC-node of the driver stage. X2 has a turn ratio of N=2:1 and with two secondary windings connected in parallel to improve the coupling coefficient. The total coupling coefficient is k= 0.65 at 5.3 GHz. The size of the transformer is $175 \times 175\,\mu m^2$. All windings are realised using the thick top metal layer. Modeling issues of monolithic transformers are presented in [10]. The output stage of the PA uses an emitter area of $155\,\mu m^2$ for T3, T4 each, matched by a LC-BALUN to the 50 Ω load. The method of designing this balun structure can be found in [7]. Further details on output balun design structures are found in [11], [12], [13].

IV. Experimental Results

The PA was characterized using a simple PCB with two 50 Ω transmission lines. For the tests, the die was attached glued and bonded directly to a PCB with two 50 Ω transmission lines (Fig. 1).

Fig. 3 shows the power transfer characteristic of the PA. Measured at 2.4 V supply voltage, a maximum output power of 26.3 dBm is obtained.

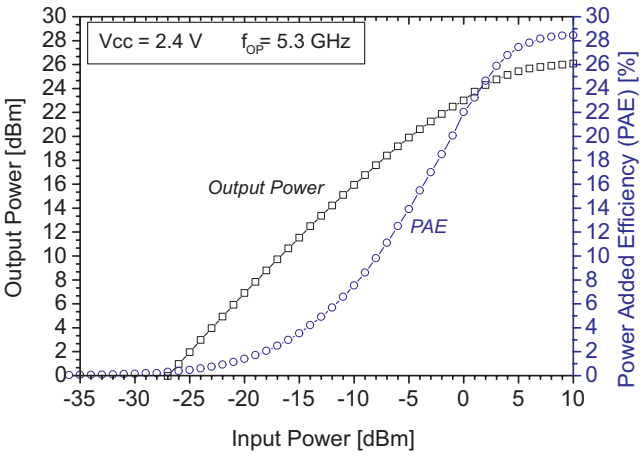

Fig. 3. Measured power transfer characteristic.

More important for WLAN is the linearity characterized by two major criterions: The Error Vector Magnitude (EVM) and the spectral mask. Fig. 4 shows the results versus frequency. The tuning to 5.8 GHz as resonance frequency of

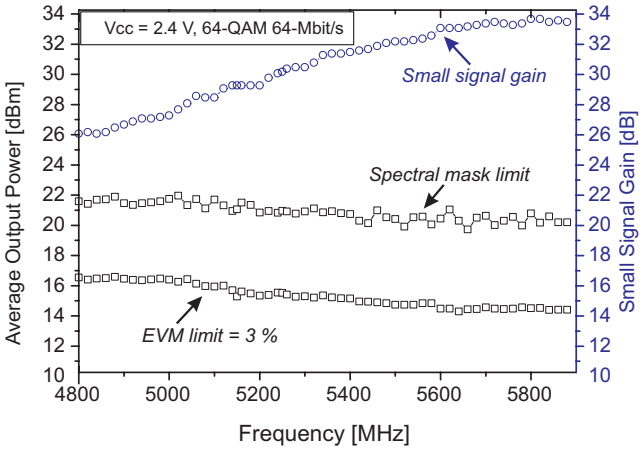

Fig. 4. Measured maximum output power for 3 % EVM, maximum spectral mask and small signal gain.

the transformers can be found in the small-signal gain plot, showing its maximum at the desired frequency. The main reason for tuning up the resonances is the decreasing output power level at higher frequencies of the RF transceiver output. Furthermore Fig. 4 shows the maximum average linear power for a maximum EVM of 3 % (54 Mbit/s, 64-QAM input signal) and the spectral mask limit. Due to the high bandwidth, it covers all 5 GHz bands. The spectral mask for 5.25 GHz is shown in Fig. 5, showing very high margins. Tab. I shows a

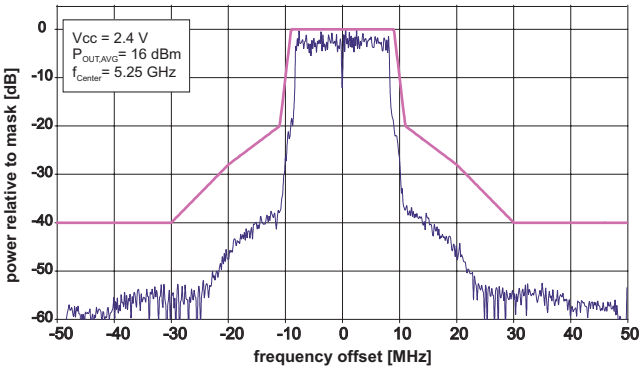

Fig. 5. Measured spectral mask for f_{Center} = 5.25 GHz

performance summary.

V. Ruggedness Measurement Results

As PAs are connected to an antenna representing a load-line mismatch, the PA has to be tested for for output impedance mismatch conditions, if degradation or destruction occurs. Especially Si-based technologies have to be tested, as the usually low breakdown voltages compared to III/V-HBT technologies limit their usage. Transistor modeling issues with the focus on the avalanche breakdown are found in [14], [15]. For ruggedness testing, the PA was connected to an automatic load-pull tuner running on the VSWR-circles (100 points per VSWR value) with an output mismatch of VSWR = 3,5,7,10,15,20 and 50. In any operation mode (linear and saturated) the PA survived the mismatch. For saturation mode at VSWR=10 and above current jumps indicating starting breakdown effects, but no damage or degradation occurred as observed by further

Operating frequency	4.8 GHz – 6 GHz			
Small-signal gain (5.8 GHz)	33 dB			
Maximum average linear output power (5.25 GHz) (54Mbit/s 64-QAM, max. 3% EVM)	16 dBm			
Supply voltage	2.4	1.5	1	V
Maximum output power	26.3	22.4	19.1	dBm
Power-added efficiency (5.25 GHz, Pin=10 dBm)	28.5	24.4	21.2	%
Output stage collector current (RF on- Pin=10 dBm)	2 x 225	2 x 152	2 x 105	mA
Output stage collector current (RF off)	2 x 33	2 x 50	2 x 46	mA
Driver stage current (RF on - Pin=10 dBm)	2 x 67	2 x 77	2 x 76	mA
Driver stage current (RF off)	2 x 34	2 x 37	2 x 36	mA

TABLE I

PERFORMANCE SUMMARY (T=300 K, INPUT AND OUTPUT LOAD: 50 Ω)

characterization. Fig. 6 shows the measured output power for a VSWR=10 and 50 mismatch.

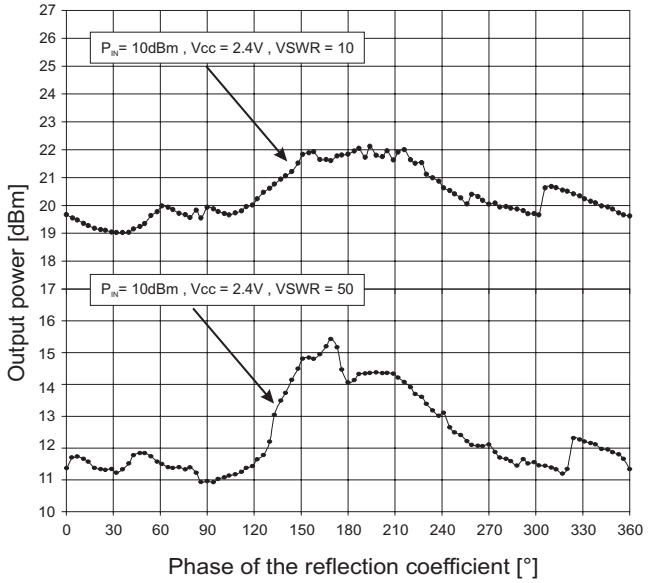

Fig. 6. Measured output power with VSWR = 10 mismatch.

VI. CONCLUSION

A fully integrated power amplifier for 4.8-6 GHz is demonstrated in a 0.35 μm-SiGe-bipolar technology. It is based on a push-pull type circuit with on-chip transformer coupling and on-chip output balun. Thus the amplifier does not require any external components and shows high ruggedness and high output power at low EVM over a large frequency range. At a supply voltage of 2.4 V the average linear output power is 16 dBm for 3% EVM at 5.3 GHz and the saturated output power is 26.3 dBm with a PAE of 28.5 % at 5.3 GHz.

REFERENCES

[1] K. Vavelidis et al., "A Single-Chip, 5.15GHz-5.35GHz, 2.4GHz-2.5GHz, 0.18mm CMOS RF Transceiver for 802.11a/b/g Wireless LAN," in *Proceedings of the 29th European Solid-state Circuit Conference*, Estoril, Portugal, September 2003.

[2] Microsemi Integrated Products, "LX 5503 Production Data Sheet," *www.microsemi.com*.

[3] W. Bakalski, K. Kitlinski, G. Donig, B. Kapfelsperger, W. Österreicher, W. Auchter, R. Weigel, and A. Scholtz, "A 5.25 GHz SiGe Bipolar Power Amplifier for IEEE 802.11a Wireless LAN," in *Proceedings of IEEE International Microwave Symposium*. Fort Worth, TX: IEEE, June 2004.

[4] W. Bischof, M. Alles, J. Berntgen, and S. Gerlach, "Fully Integrated 5-6GHz 700mW SiGe Power Amplifier MMIC," in *Proc. of European Microwave Week 2003 EuMC*, Munich, Germany, 6-10 October 2003.

[5] T. Johansson, "Wireless-trench technology for portable wireless applications," *Ericsson Review - http://www.ericsson.com/review*, vol. 1, pp. 6–9, 2001.

[6] Aoki, I., Kee, S. D., Rutledge, D., and Hajimiri, A., "A 2.4 GHz, 2.2 W, 2 V fully integrated CMOS circular geometry active transformer power amplifier," in *IEEE Custom integrated circuits conference*. San Diego: IEEE, May 2001.

[7] W. Bakalski, W. Simbürger, R. Thüringer, A. Vasylyev, and A. Scholtz, "A fully integrated 5.3 GHz, 2.4 V, 0.3 W SiGe-Bipolar Power Amplifier with 50 Ω output," *IEEE Journal of Solid-State Circuits*, vol. 39, no. 7, pp. 1006–1014, July 2004.

[8] W. Klein and B.-U. Klepser, "75GHz Bipolar Production Technology for the 21th Century," in *Proceedings of the ESSDERC 1999*, 1999, pp. 88–94.

[9] Rickelt, M. and Rein, H.-M., "Impact-ionization induced instabilities in high-speed bipolar transistors and their influence on the maximum usable output voltage," in *Bipolar/BiCMOS Circuits and Technology Meeting*. Minneapolis: IEEE, September 26-28 1999.

[10] D. Kehrer, W. Simbürger, H.-D. Wohlmuth, and A. Scholtz, "Modeling of Monolithic Lumped Planar Transformers up to 20 GHz," in *IEEE Custom Integrated Circuits Conference CICC 2001*, San Diego, May 2001, pp. 401–404.

[11] Mongia, R., Bahl, I., and Bhartia, P., *RF and Microwave Coupled-Line Circuits*, 1st ed. Norwood,MA 02062: Artech House, 1999.

[12] D. Raicu, "Design of planar, single-layer microwave baluns," in *IEEE MTT-S International Microwave Symposium Digest*. IEEE, 1998, cat.No.98CH36192.

[13] W. Bakalski, Simbürger,W., Knapp,H., and Scholtz,A.L., "Lumped and Distributed Lattice-type LC-Baluns," in *Proceedings of IEEE International Microwave Symposium*. Seattle: IEEE, June 2002.

[14] M. Rickelt and Rein, H.-M., "A novel transistor model for simulating avalanche-breakdown effects in si bipolar circuits," *IEEE Journal of Solid-State Circuits*, vol. 37, no. 9, pp. 1184–1197, 2002.

[15] M. Reisch, *High-Frequency Bipolar Transistors*, 1st ed. Springer, 2003.