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CHARACTERISATION OF ACTIVE LOADS FOR MMIC's

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Abstract

Active loads have been fabricated and tested, and their characterisation addressed for use in microwave CAD programs. The first results show that non-ideal (parasitic) effects are present that can easily be evaluated. Comparison with a three-terminal FET structure shows that a characterisation in terms of an equivalent circuit is feasible, and suggests a possible procedure for the extraction.

Introduction

In the last years the design of monolithic microwave integrated circuits has increasingly made use of configurations typical to monolithic implementations. In this area the use of active devices to replace passive elements (active loads) has the advantage of smaller dimensions and better reproducibility. For simple small-signal use the loads can be represented by an S-parameter matrix, measured at all possible quiescent voltages. It has been found that a two-port representation must be used, because of the presence of parasitic capacitances to ground (fig.1), as apparent from the asymmetry of the measured Y-matrix. In the case of large-signal applications, where for instance the dynamic range of an amplifier must be predicted and controlled, a non-linear model must be available. A natural choice is the standard equivalent-circuit model of a FET device, with the gate and source electrodes suitably connected (fig.2). Since the elements of the equivalent circuit cannot be extracted from active load measurement only, an identical active element in a two-port configuration has been fabricated on the same wafer. An analysis of the measurements shows that the different lay-out of the pad connection, required for the active-load application, implies a modification of the parasitics. A comparison between the two suggests an extraction procedure for the active load model.

The model

The model of the active load includes parasitic capacitances to ground, that can easily be extracted from the measured S-parameters of the active load only. If converted to Y-parameters, they have the low-frequency expressions:

$$Y_{11} = Y_{al} + j\omega C_{pg} \qquad Y_{12} = Y_{21} = -Y_{al} \qquad Y_{22} = Y_{al} + j\omega C_{pd}$$

where Y_{al} is the admittance of the proper active load. The values of the capacitances and of the active load admittance are easily extracted from the above equations. For the case of fig.3 (a 200-μm FET), the capacitances have the values C_{pg} = 32 fF, C_{pd} = 20 fF.
The remaining elements of the equivalent circuit are best extracted from a three-terminal FET identical to the active-load FET. The different inductive and capacitive parasitics, deriving from the shorted gate-source connection, (fig.4) are first evaluated from the comparison between the Y-matrices, prior to the extraction of the remaining elements. In our case, the values are C_{pg}=20 fF, C_{pd}=15 fF, L_g=-30 pH, L_s=-10 pH. The negative inductance corresponds in fact to a reduction of the

source and gate inductances (namely) L_s, L_g of the three-terminal FET (whose parasitics connection is indicated in fig.5).
Once these parasitics are known, a standard extraction of the remaining elements is performed, e.g. as in [1]-[3].

Conclusions

The structure of the equivalent circuit of an active load has been established, opening the way to a complete characterisation for linear and non-linear CAD applications in MMIC's.

Bibliography

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[2] G.Dambrine, A.Cappy, F.Heliodore, E.Playez, 'A new method for determining the FET small-signal equivalent circuit', IEEE Trans. MTT, vol.36, n.7, July 1988

[3] G.Leuzzi, A.Serino, F.Giannini, S.Ciorciolini, 'Novel non-linear equivalent-circuit extraction scheme for microwave field-effect transistors', Proc. 25th European Microwave Conf., Bologna (Italy), Sept.1995, pp.548-552.

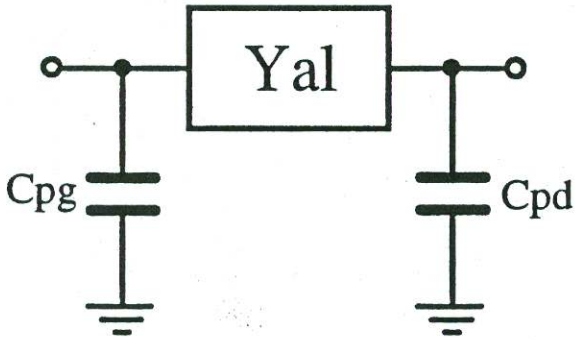

Fig.1 - The general schematic of an active load.

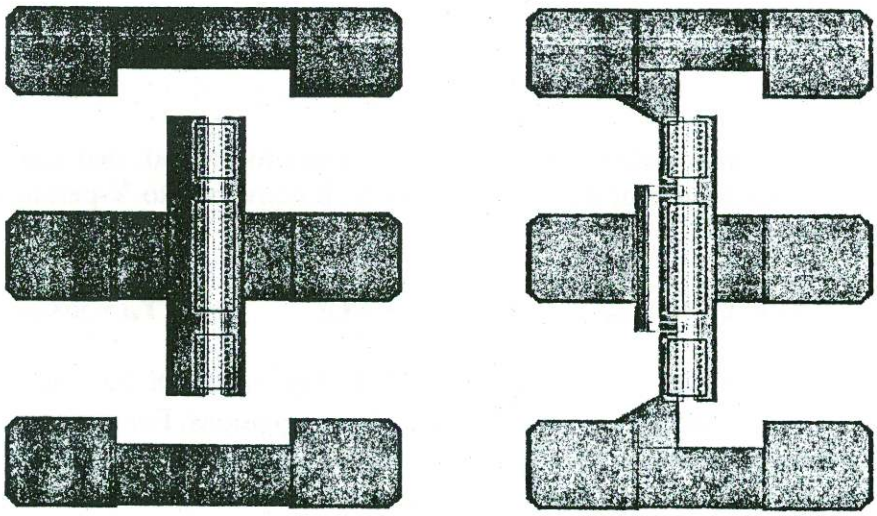

Fig.2 - The lay-out of the active load and of the identical three-terminal FET

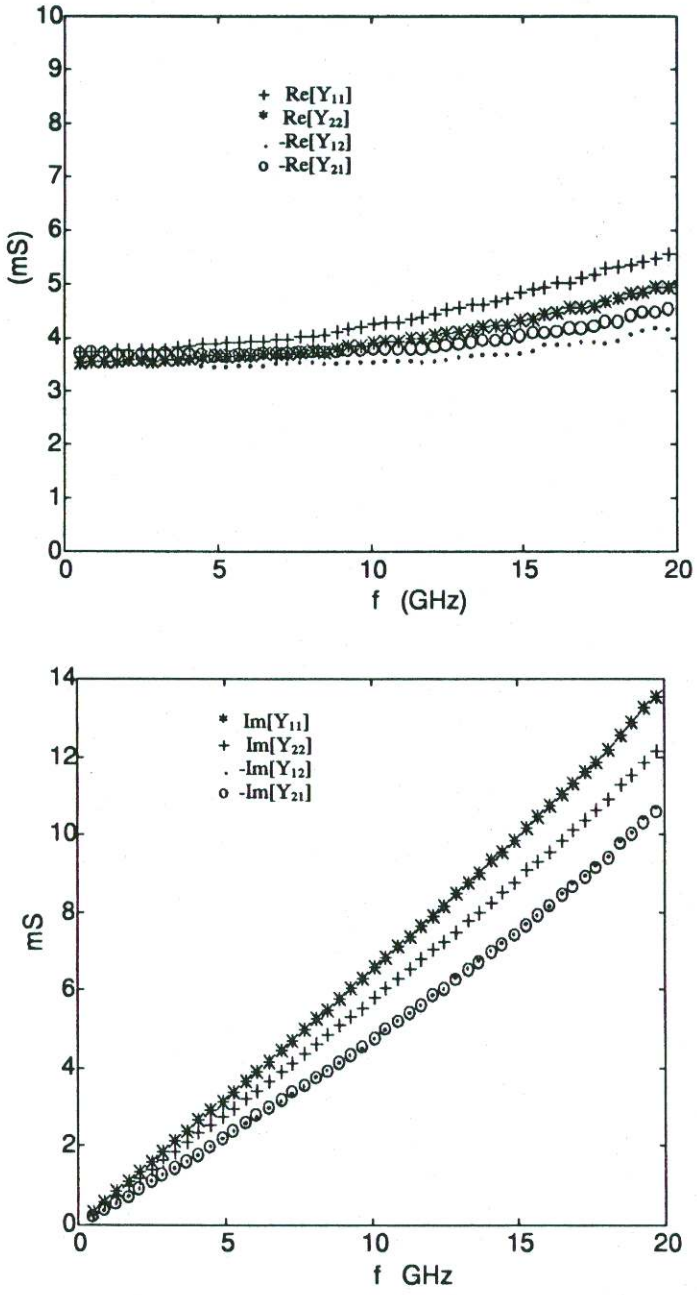

Fig.3 - Real (up) and imaginary (down) parts of the Y-matrix of the active load.

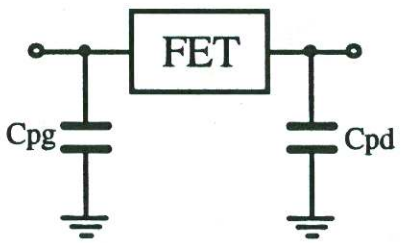

Fig.4 - The parasitics of a FET connected as active load

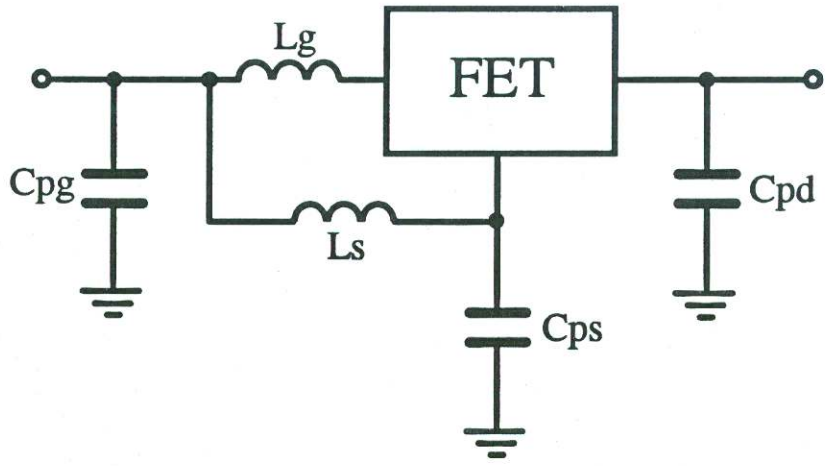

Fig.5 - The parasitics of a FET connected as a three-terminal device.