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TRANSMISSION LINE PULSE BASED RELIABILITY INVESTIGATIONS OF HBTs

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Abstract: We propose **t**ransmission **l**ine **p**ulse (TLP) stress instead of DC bias stress in order to stimulate different failure mechanisms for HBTs for wafer level reliability characterisation and show the effects of degradation on the device performance. The established Wunsch-Bell model [1] is employed for a calculation of the intrinsic device temperatures within the active region from the measured pulse voltage and current. The device MTTF can be predicted for various thermally induced failure modes. Additional degradation mechanisms related to the high current densities obtained during TLP stress show that this method is more operational than the established accelerated lifetime tests.

Introduction: GaInP/GaAs and AlGaAs/GaAs HBTs are prospective devices for high power and very high frequency amplifier applications. Nevertheless the long term stability and reliability of these devices is a critical aspect because of the high thermal resistivity of GaAs and the high current densities within the base region, although the so called "second (thermal) breakdown" typical for silicon devices is not observed in GaAs based devices. There are also still some material and technology related issues like the base ledge problem. We have realised a novel TLP based wafer level test set-up in order to characterise the reliability of HBTs and to obtain an insight into the physical mechanisms of degradation.

Measurement set-up:

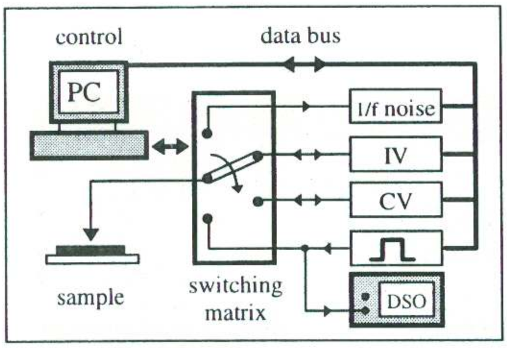

Fig. 1 Measurement set-up used for pulsed HBT stressing

The set-up used in our experiments is shown in Fig. 1 and has been described in detail in [2, 3]. We have used a special reflection free high current square pulse generator with a fixed pulse width of 100ns and a rise time between 0.7ns and 8ns for mainly electrically induced stress and a low current square pulse generator with a pulse width between 50ns and 100µs at 50Ω source impedance for combined electrical and thermal stress. The device response to the applied pulses is analyzed in order to calculate the stress current density within the HBT and the intrinsic temperatures employing the Wunsch-Bell-model. This measurement principle is a one port device response method.

The systematic selection of pulse parameters like the pulse length τ_{Pulse} , pulse height V_{Pulse} , superimposed DC-level, variation of ambient temperature etc. renders the clear distinction between various degradation mechanisms. The set-up is completely computer controlled. Employing a switching matrix, the devices can remain needle contacted during a step stress test in order to detect even slight changes in the IV or noise characteristics and to obtain the history of degradation.

Experimental results: A number of 100µm*100µm GaInP and AlGaAs test HBTs has been stressed with 100ns square pulses from the TLP generator. In order to simulate the operation in the active normal mode during the one port device response measurement a special testing procedure has been developed: In a first step square pulses were applied between base and emitter in forward operation mode in order to stress the base access region where the highest current density within the HBT structure is obtained. The specially designed circuitry of the pulse generator avoids any unintended stress in the reverse operation mode which could conceal the true failure mode. The results of this experiment are given in Fig. 2 for a pulse amplitude of 14.5V and a current density of 4.85MA/cm^2 within the base access region. As this region is driven into the saturated velocity range the major part of the pulse current flows over the reversely biased base collector diode and through the highly doped subcollector ($N_D=5*10^{18}/cm^3$) as shown in Fig. 3.

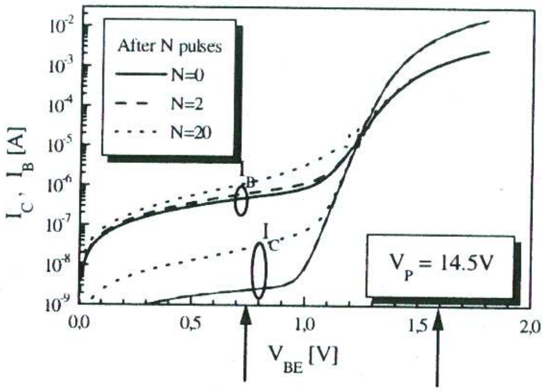

Fig. 2 Degradation of a GaInP HBT during base emitter pulse stress at 14.5V pulse amplitude and a current density of $J=4.85MA/cm^2$ (τ_P = 100ns)

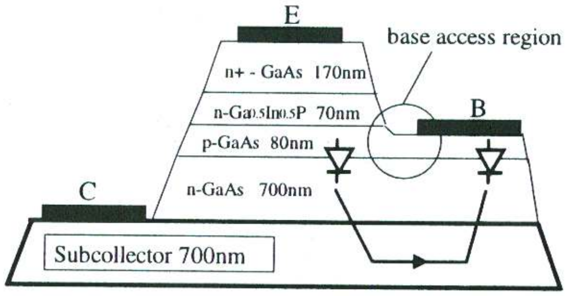

Fig. 3 Parasitic current path over the base collector interface during base emitter stress

The base collector diode is driven into the avalanche mode because of the big base emitter voltage drop. Nevertheless not only the base collector diode but also the base emitter diode is damaged under these circumstances as visible in Fig. 2:

A strong increase in base and collector leakage current has been observed during the stress and the current gain of the HBT at high bias values is reduced during proceeding stress. This degradation is caused by a defect generation at the base-emitter hetero interface. The extracted variations in base and collector current during a step stress test are given in Fig. 4 for the two base emitter voltage values $V_{BE1}=0.75V$ and $V_{BE2}=1.6V$ marked in Fig. 2 as a function of the pulse number applied.

The increase in leakage current correlates with a decrease in the collector current at $V_{BE2}=1.6V$ and the current gain, an effect that has been reported by a number of authors [4]. The collector leakage current variation at $V_{BE1}=0.75V$ shows a non monotonous behaviour which can be attributed to a generation of local base collector interface defects which can be burnt out during the application of further square pulses (N=20..60). For N>100 pulses a strong non reversible degradation has been obtained.

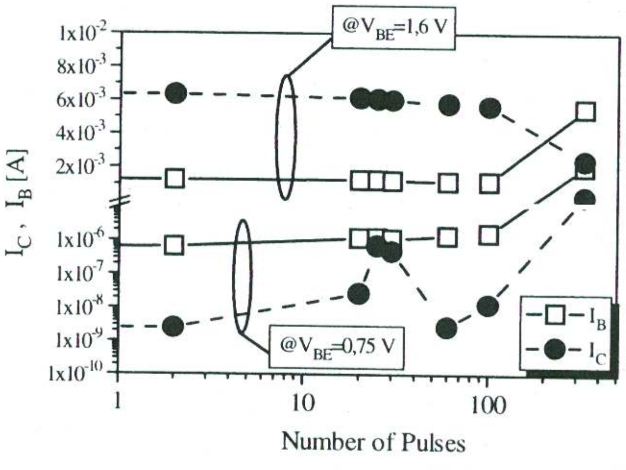

Fig. 4 Change in the base and collector current of a GaInP HBT as a function of increasing base emitter pulse stress ($J=4.85MA/cm^2$, τ_P = 100ns)

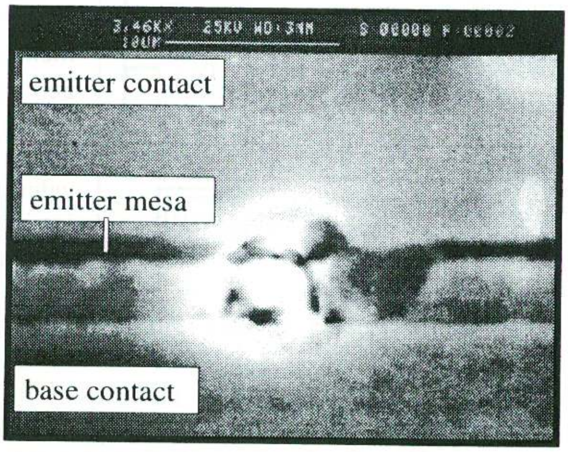

Fig. 5 Melting of the base region of a GaInP HBT after the application of N=330 square pulses of 14.5Vamplitude ($J=4.85MA/cm^2$, τ_P = 100ns)

In Fig. 5 a SEM picture of a catastrophic destruction of the base emitter diode after the application of N = 330 pulses at 14.5V amplitude ($J=4.85MA/cm^2$) is given. A thermal destruction of the semiconductor material has been observed exactly in the center region of the base layer, where the highest current density and temperature is reached as an effect of current concentration.

At the beginning of the tests the defects induced by the base emitter stress mainly influence the characteristics of the base emitter diode. As reported in many publications, this effect is attributed to the ledge problem [5], a degradation of the base access region surface. For proceeding degradation the defects extend through the base layer towards the base collector interface and reduce the base collector breakdown voltage leading to final burnout [6]. This failure mechanism has been reproduced in our experiments employing simple base contact TLM test structures showing the same degradation threshold. Taking into account Fig. 6 we have at first obtained an ohmic base contact degradation leading to a strong increase in contact resistance. During the further stressing of the base TLM structure the base collector interface is destroyed underneath the contact with the negative pulse polarity applied.

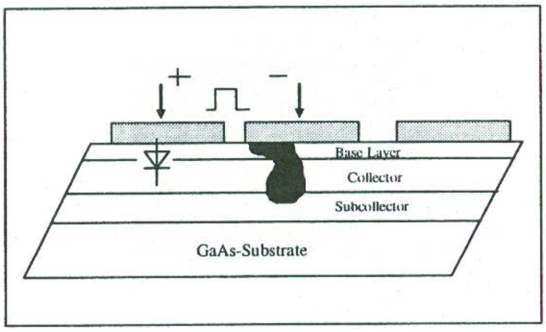

Fig. 6 Base collector interface burnout as an effect of high current base stress

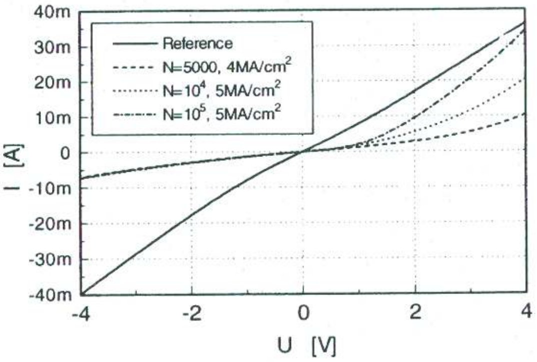

Fig. 7 Degradation of a base TLM structure during 100ns pulsed stress

Fig. 7 shows the IV characteristics of the base TLM structure during proceeding degradation. Starting from an ohmic behaviour, the contact resistance is strongly increased after N=5000 pulses at $4 MA/cm^2$ also showing a slight non-linearity. The strong current flow over the subcollector finally leads to a burnout of the base collector interface which can be perceived from the strongly asymmetric characteristics in Fig. 7.

In order to avoid this secondary degradation mechanism related to high current base stress, square pulses were applied between collector and emitter keeping the base terminal floating in a second experiment. Here the base collector diode was also driven into the avalanche mode and the threshold for stressing current density and voltage was in the same range as for base emitter stress. A reduction of the high bias collector current, a strong increase in base leakage current and a degradation of current gain have been obtained as shown in Fig. 8. The characteristics of the base collector diode remain nearly unchanged although it is stressed in reverse operation, because the current density driven over this interface is much less critical than for the base emitter hetero interface.

In these tests, an additional shift in the I_C curve of the gummelplot towards higher V_{BE} values occurs as an effect of charge storage at stress induced traps at the base emitter interface. The high current pulsed stress leads to a charge injection at the interface which is partially permanent and partially reversible and reduces the base transport factor. This effect has been reproduced with physics based finite element simulations [7].

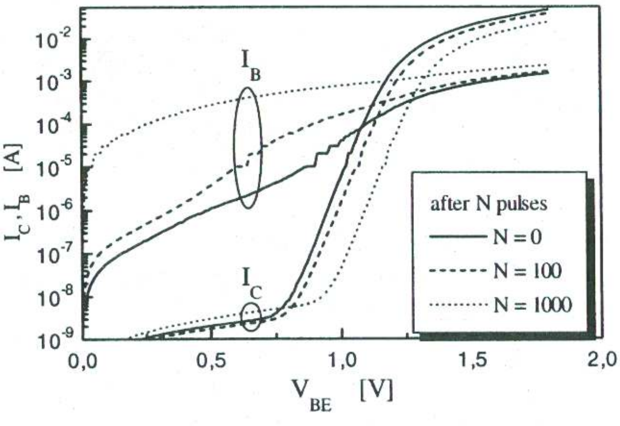

Fig. 8 Variations in the gummelplot of GaInP HBT as a function of increasing collector emitter pulse stress (V_{PULSE} = 16.5V $J=5.05 MA/cm^2$)

In order to compare our TLP stress results with existing thermal degradation experiments, we have extracted the intrinsic device temperatures related to the stress current densities applied.

Fig. 9 shows the work published by Henderson [8] for the temperature dependence of degradation effects for HBTs. Different independent failure mechanisms with characteristic activation energies can be perceived from this graph. On the right side of Fig. 9 the temperature ranges for the degradation effects observed in our experiments are plotted. The temperature is calculated employing the Wunsch-Bell equation for 1-D heat flow.

In the future the measured pulse response of the devices will be used to extract the intrinsic temperature and to obtain a built in temperature sensor. This method for a thermal characterisation, backed by a numerical electrical thermal simulation, has been described in [9].

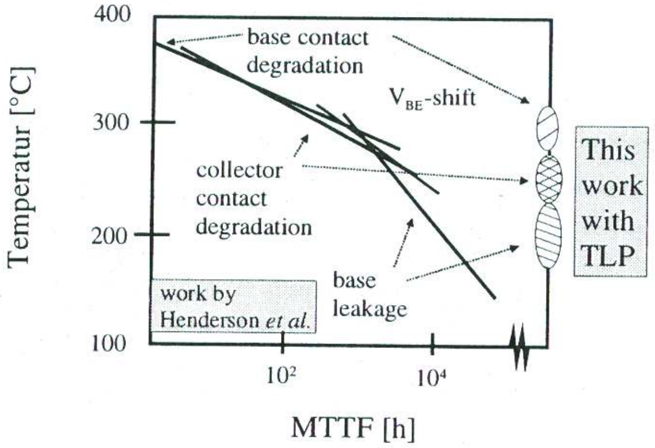

Fig. 9 Comparison of the temperature range of HBT degradation effects from this work with the work of Henderson *et al.* [8]

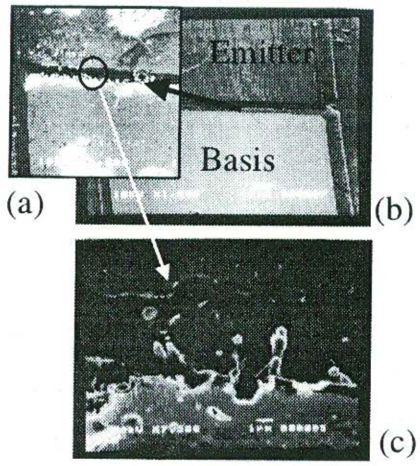

Fig. 10 Metal migration from the base contact towards the emitter

The advantage of the TLP method is that current and field induced degradation effects like the base contact degradation can be directly stimulated without a global intrinsic device heating, leading to an integral stimulation of several failure mechanisms. Even ESD related mechanisms can be stimulated as shown in Fig. 10 (c): High voltage base emitter stress at a very low pulse width leads to a non thermally induced metal migration from the ohmic Ti/Pt/Au base to the emitter contact.

Conclusion: The application of TLP stress renders the intended stimulation of various physical failure modes and the detection of critical aspects in the design of HBTs. The variation of pulse parameters is a possibility to emphasise one of the different particular physical failure mechanisms given in Fig. 9, as the related intrinsic device temperatures found from our Wunsch-Bell approach are similar to those reported in literature. This means that the TLP method can be used in order to characterise the reliability of HBTs and to obtain a built in reliability device design. At the moment the most critical failure mechanisms seem to be the thermally induced degradation of the base region, the ledge problem and the outdiffusion of dopants.

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