Highly-Integrated X-band Multi-function MMIC with Integrated LNA and Driver Amplifier

A. de Boer, J.A. Hoogland, E.M. Suijker, M. van Wanum, F.E. van Vliet

TNO Physics and Electronics Laboratory, P.O. Box 96864, 2509 JG The Hague, The Netherlands, Phone: 31.70.374.04.02, Fax: 31.70.374.06.54, Email: deboer@fel.tno.nl

The design and performance of a highly integrated X-band multi-function MMIC with integrated LNA and high output power will be discussed. The MMIC integrates all the control functions of a transmit/receive module. The integration of a Low Noise Amplifier and Driver Amplifier makes this MMIC extremely suitable for a two chip T/R module solution. The MMIC is realised in the 0.25µm PHEMT (PH25) process of UMS.

INTRODUCTION

In the next generation Transmit/Receive (T/R) Modules for phased array radar applications, cost reduction and performance enhancement are of vital importance. By using microwave monolithic integrated circuits, these demands can often be met. Phased array radars use up to thousands of antenna elements all driven by transmit/receive modules containing several functions. The volume available for these transmit/receive modules is very limited, considering $\lambda/2$ element spacing and the trend toward smart skins. The demand for size reduction of the transmit/receive modules or even integration of antenna and transmit/receive modules becomes more and more important.

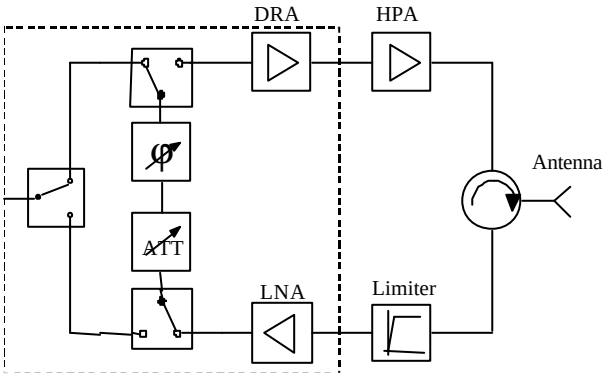

Figure1: Block diagram of next generation T/R modules.

By integrating several functions such as phase and gain control, low-noise and driver amplifiers and T/R switches on a single multi-function chip, the size of a transmit/receive module can be considerably reduced and its cost lowered. An example of the RF path of such a transmit/receive module is depicted in Figure 1 (1).

The blocks within the dashed line indicate the functional behaviour of the multifunction chip under consideration. It can be seen that in combination with a power amplifier it is possible to make a two chip transmit/receive module.

MULTI-FUNCTION CHIP DESIGN

The used topology is based on a trade-off between noise figure, third-order intercept point and insertion gain. The block diagram of the multi-function chip is shown in more detail in Figure 2. The chip consists of three transmit/receive switches, a low noise amplifier at the RX input, a 6-bit phase shifter and a 6-bit attenuator in the common leg of the chip, interstage amplifiers, a driver amplifier at the end of the TX chain, gate-bias circuits and a combined level-shifter/inverter to control the chip.

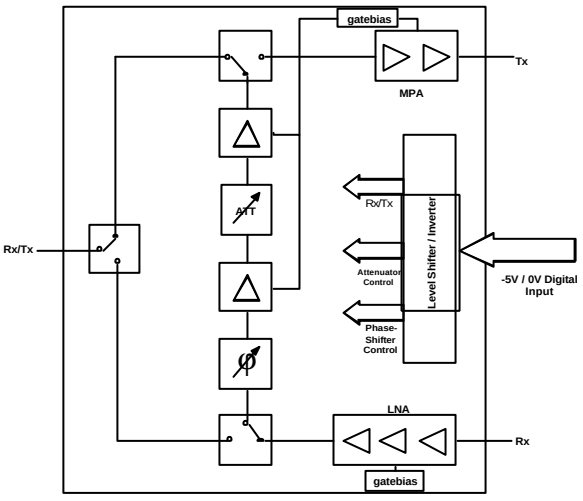

Figure 2: Block diagram of multi-function chip.

To meet all the specifications of the multi-function chip and especially the noise figure, output power and third order intercept point, the gain distribution over the chip is very important. To achieve the required noise figure, a three stage LNA is required. To improve the yield and to set the optimum bias point for the LNA with a fixed supply voltage (+4V/-4V), a gate-bias circuit is added. It can be considered to place the third stage of the LNA as first amplifier in the common leg. This isolates the phase shifter from the input in the transmit mode. Because the power levels in transmit can be up to 10 - 15 dBm at the input, the nonlinear requirements to the third stage of the LNA become unrealistic, and requires in fact a driver amplifier. Furthermore, the phase shifter and attenuator requirements have to deal with these power levels in transmit as well. For low-noise processes, this is difficult to achieve, given the available breakdown voltage of the transistors used in the switches. As a consequence, the full three stages are preferably implemented before the input switch.

The following point is the placement of the first amplifier in the common path. This must be placed after sufficient loss is encountered, to avoid the aforementioned problem. When placing this amplifier in between the phase shifter and attenuator, the power problem has become acceptable. Furthermore, the interaction between phase and amplitude setting is now minimised through the isolation of this amplifier. For a high output third order intercept point in the receive mode it is important to have an amplifier as close as possible to the output. The second common leg amplifier is therefore placed at the output of the attenuator. In transmit mode, a high output power is required to be able to drive the HPA. This power must preferably be generated after the switch, again to avoid breakdown problems. The second amplifier of the common path is therefore complemented with a two stage driver amplifier after the output switch. The output power of the multi-function chip is well over 20 dBm. To improve the yield and to set the optimum bias point for the driver and common leg amplifiers, a second gate-bias circuit is added.

The gain of the multi-function chip in receive is more than 20 dB and the bandwidth more than 30%. The six bit phase shifter is based on the switched filter principle (2,3). The control range of the phase shifter is 360º with a step size of 5.625º. The six bit attenuator, with a range of 27 dB, consists of cascaded bits of which the smallest bits are of the switched scaled T type and the largest bits of the SPDT type (4,5). Due to the large gain range and the integration of three T/R switches, the switch isolation is very important. The switches used are SPDT, with two sections to gain an isolation of better than 35 dB. The phase shifter, attenuator and T/R switches are all connected to the integrated level-shifter/inverter.

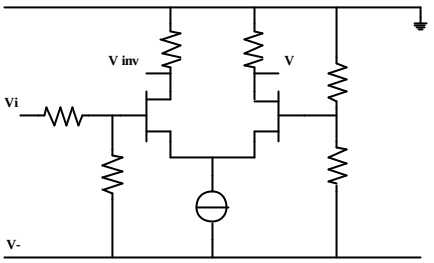

Figure 3: simplified schematic of one section of the level-shifter/inverter.

The level-shifter/inverter converts the control signals from 0V/-5V to 0V/-1.5V. It also reduces the number of chip control lines with a factor of 2 due to the complementary outputs (-1.5V/0V). To minimise process sensitivity, an accurate current reference source is designed. A simplified schematic of one level-shifter/ inverter section is shown in figure 3. The total power consumption of the level-shifter/inverter is about 72 mW. The power consumption of the total chip is less than 1.2 W.

LAYOUT

The multifunction chip is realised in the 0.25µm PHEMT (PH25) process of UMS. A photograph of the chip is depicted in figure 4.

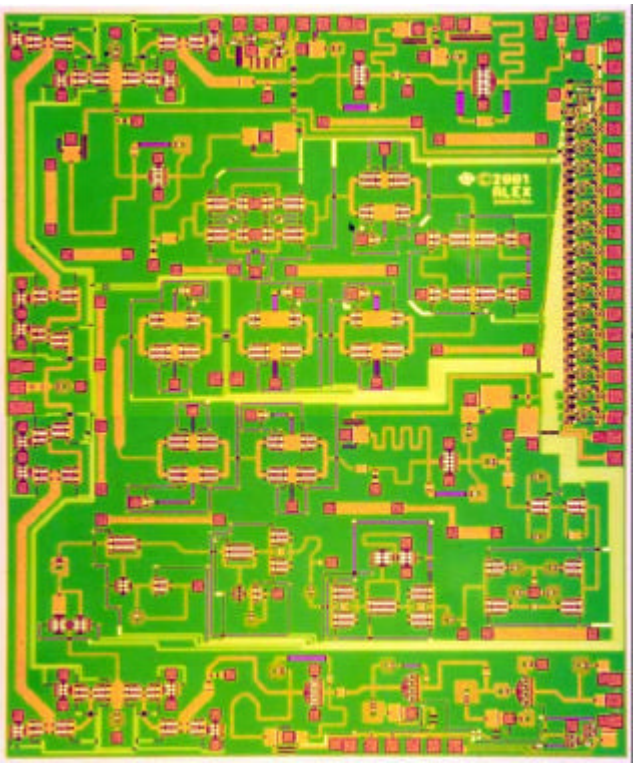

Figure 4: Photograph of the multi-function chip.

The size of the chip is 4.5 x 5.5 mm^2. A lot of attention is paid to the layout of the multi-function chip. To have an optimum isolation between the RF paths, all three T/R switches are placed at the edge of the chip. On the left side of the upper and lower corner the two-section T/R switches can be seen. The common-switch which is connected to the RF input/output pad can be found in the middle on the left side of the chip. Also the RF in- and output ports are maximum apart from each other to have a good isolation. The LNA input can be seen at the lower right side of the chip and the TX output at the upper right side. For the LNA and driver amplifier it is very important to have a good low frequency (<5 GHz) decoupling to ensure stability. For this reason the three-stage LNA and the two-stage driver amplifiers are placed at the edge of the chip. The LNA can be seen on the lower side of the chip and the driver amplifier on the upper side of the chip. In the middle of the chip the phase shifter followed by the first common leg amplifier, attenuator and second common leg amplifier can be seen. The level-shifter/inverter is designed as a strip and can be seen clearly. All control lines are routed to the right side of the chip. It must be noted that the control bus does not cross the RF path.

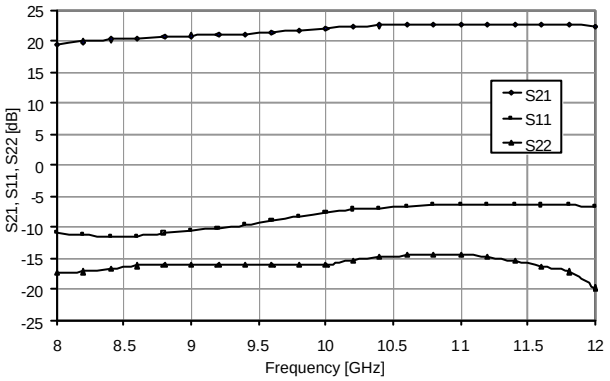

Figure 5: The measured S_{21} ,S_{11} ,S_{22} versus frequency of the MFC in the receive mode at maximum gain setting.

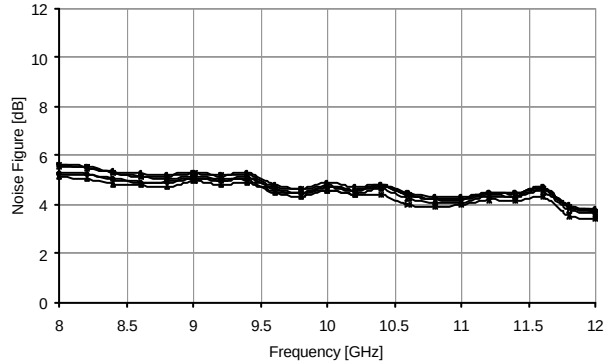

Figure 6: The measured noise figure versus frequency of the MFC in the receive mode at maximum gain setting for several chips.

MEASUREMENT RESULTS

The measurement results of the first run are shown in this section. In figure 5 the gain and the input and output return losses are shown in the receive mode. It can be seen that the gain is more than 20 dB. The gain in the transmit mode, not shown, is a bit lower and the behaviour is about the same as in the receive mode. The noise figure of the chip in the receive mode is shown in figure 6. The performance of the LNA does not comply with the simulations, in input matching and hence in noise figure. The major phase states (5.625º, 11.25º, 22.5º, 45º, 90º and 180º) are shown in figure 7.

The major attenuation states (0.438dB, 0.875dB, 1.75dB, 3.5dB, 7dB and 14dB) are shown in figure 8. The one dB compression point and the third order intercept point at the input in the receive mode for several chips are shown in figure 9 and 10. The third order intercept point at the output is about 16 to 17 dBm. The measured output power in the transmit mode is shown in figure 11. It can be seen that the output power is well in excess of 20dBm.

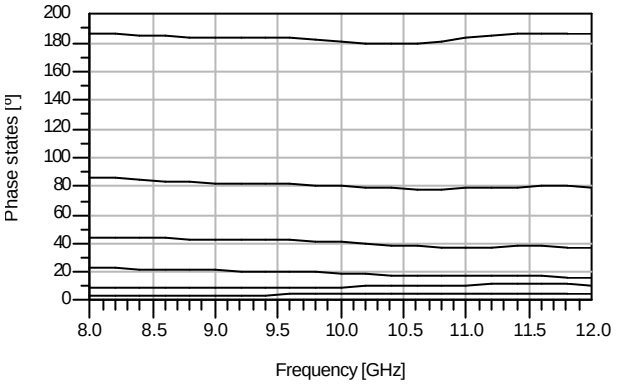

Figure 7: The measured major phase states versus frequency of the MFC.

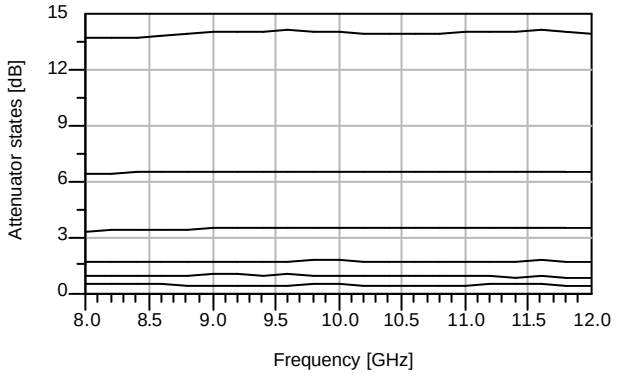

Figure 8: The measured major attenuation states versus frequency of the MFC.

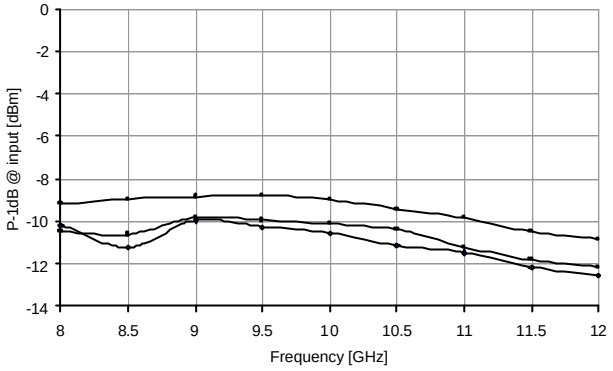

Figure 9: The measured P_{-1dB} compression at the input versus frequency of the MFC in the receive mode.

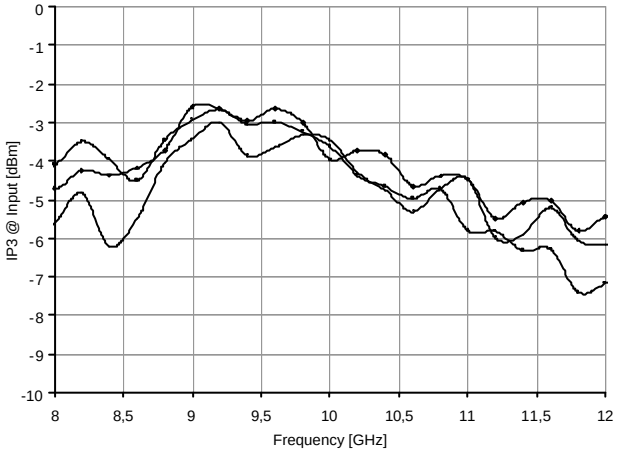

Figure 10: The measured third order intercept point at the input versus frequency of the MFC in the receive mode.

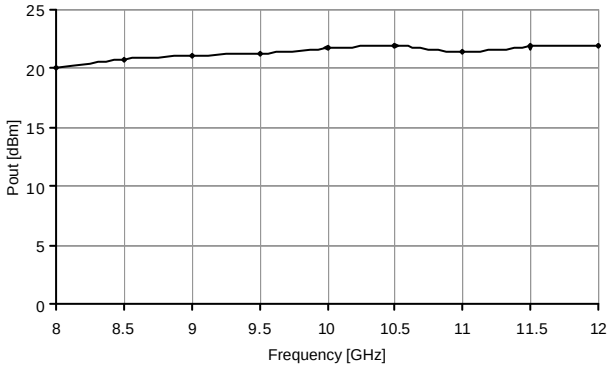

Figure 11: The measured output power versus frequency of the MFC in the transmit mode at an input power of 8 dBm.

CONCLUSION

The design of a highly integrated X-band Multi-function MMIC with low noise figure and high output power is successfully accomplished. Despite a very high functional integration and a very compact layout, the MMIC was functional in a single iteration. The level of integration makes this chip extremely suitable for a two chip T/R module solution.

REFERENCES

(1) A. de Boer, K. Mouthaan, "GaAs Mixed Signal Multi-function X-band MMIC with 7-bit Phase and Amplitude Control and Integrated Serial to parallel Converter", GAAS 2000 Symposium Digest, pp. 476-479, October 2000.

(2) J. Schindler, Y. Ayasli, A. M. Morris, L.K. Hanes, “Monolithic 6-18 GHz 3 bit Phase shifter”, IEEE GaAs IC Symposium, pp 129-132, 1985.

(3) Y. Ayasli, S. W. Miller, R. Mozzi, L.K. Hanes, “Wide-band Monolithic Phase Shifter”, IEEE Trans. on Microwave Theory and Tech., pp 1710-1714, December 1984.

(4) R. Gupta, L.Holdeman, J. Potukuchi, B. Geller, F.Assal, “A 0.05- to 14-GHz MMIC 5-bit Digital Attenuator”, IEEE GaAs IC Symposium, Digest, pp. 231-234, October 1987.

(5) A.K. Anderson, and J. S. Joshi, “Wideband constant phase digital attenuators for space applications”, Microwave Engineering Europe, pp. 25-30, February 1994.