

"Performance and reliability of GaAs based power HFETs"

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ABSTRACT

This paper reports on performance and robustness to hot electron effects of GaAs based power HFET's. The performance and the reliability provide a promise of the fabricated device to be a good candidate for practical circuit application. The effective gate length can be controlled by a selective dry etching. In the latter case particular care must be taken to avoid deep surface levels which can originate instabilities of device even if of limited amount. Transconductance frequency dispersion has been employed to analyze these deep levels and can be used to control the fabrication process in order to minimize their concentration.

I. INTRODUCTION

Simple heterostructure HFET's, based on well consolidated MESFET fabrication technique, currently represent a good compromise for obtaining, at the production level, good r.f. performance at the high end of the microwave frequency range. In fact, even though AlGaAs/GaAs based HEMT and HBT devices are yielding interesting results, their widespread use in MMIC production is still limited as a results of reproducibility, yield and reliability issues typical of less mature technologies.

The rapid introduction of HFET technology for power MMIC applications can be attributed to the following advantages: fabrication as simple as the well consolidated MESFET technology; higher output power due to the Al_{0.25}Ga_{0.75}As/GaAs bandgap discontinuity; larger input power margin due to larger Ti/Al_{0.25}Ga_{0.75}As Schottky barrier height as compared to Ti/GaAs system; low output conductance with appropriate superlattice buffer layer; improved linearity and higher gain as compared to implanted MESFET's as a result of conducting channel confinement and profile; high breakdown voltage, if necessary, by appropriate doping of the Al_{0.25}Ga_{0.75}As layer [1].

Over the past years many results have been reported on the quick degradation induced by hot carriers in GaAs based HEMT's and PM-HEMT's [2]. In this paper we show that performance and robustness to hot electron effects of GaAs based power HFET are proving this device to be a good candidate for MMIC circuits

II. SAMPLES

As shown schematically in Fig. 1, the device structure consists of: an Al/Ti gate Schottky contact (L_g ranging from 0.5 to 1 μm, W_g from 0.2 to 1 mm); an n⁺ GaAs cap layer; an n doped Al_{0.25}Ga_{0.75}As layer grown over the n⁺ doped GaAs layer, separated from the substrate by an AlGaAs/GaAs superlattice buffer layer; gate-source and gate-drain spacings were both 2 μm; a SiN passivation has been used. The structure was grown by molecular beam epitaxy.

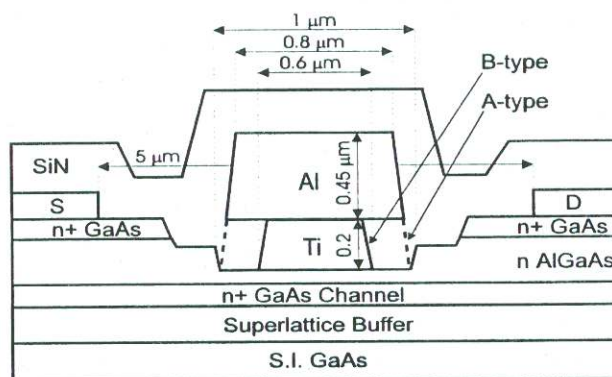


Fig. 1. Cross section of power HFET without Ti reduction (L_g = 1 μm, type A) and with Ti reduced (L_g = 0.6 μm, type B) see text.

The device comprises a Ti/Al "T-gate" structure positioned in a double-recessed channel by conventional optical lithography. Prior to final passivation by plasma deposited SiN, device gate-length (minimum 0.2 μm) is accurately determined by means of a Ti selective dry etch process. In the following we will call "A" the devices without the Ti length reduced by selective dry etching and "B" the ones with Ti length reduction.

Device design has been optimized to reduce the effect of deep levels present at the passivation interface at the edges of the gate, hot electron degradation and impact ionization phenomena. Deep levels have been characterized by means of frequency dispersion of transconductance $g_m(f)$ [3]; impact ionization by measuring the gate current induced by collection of holes generated by impact ionization in the channel [4]; robustness of devices against hot electron phenomena by step-stress in impact ionization regime [2].

III. ELECTRICAL CHARACTERISTICS AND PERFORMANCE

For 0.6 μm gate length devices a power density of

700 mW/mm with approximately 12 dB gain at 1 dB compression point is routinely obtained at 10 GHz. Figure 2 compares the associated gain vs. output r.f. power of the HFET with the one of a conventional implanted MESFET at different V_{DS} .

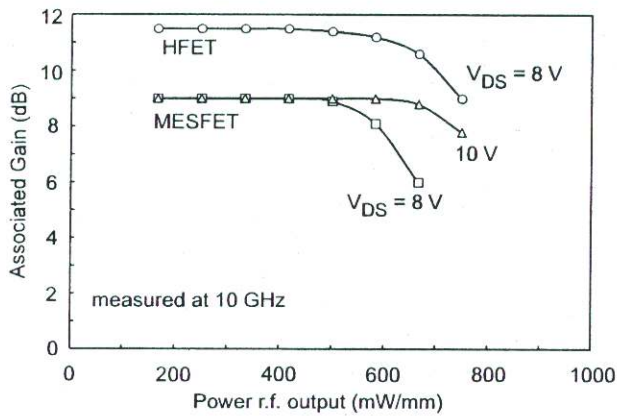


Fig. 2. Associated gain vs. power r.f. output for HFET and conventional MESFET.

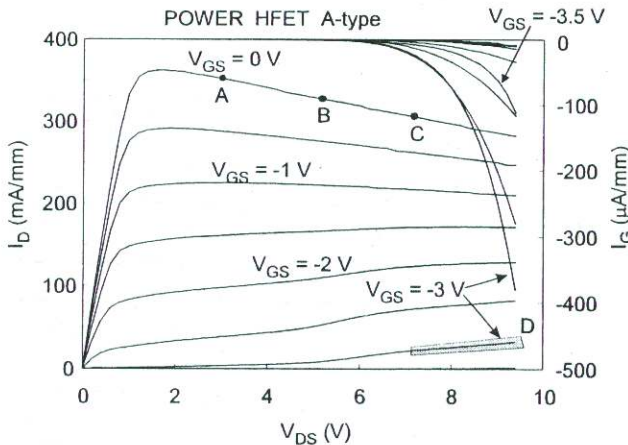


Fig. 3. Electrical characteristics of A-type device.

Data presented in the following refer to 200 μm (50 $\mu\text{m} \times 4$) gate width devices.

Figure 3 shows the output characteristics of an A type device. A small kink in the I-V curves is observed at high V_{DS} ($V_{DS} \geq 5$ V) and near pinch-off conditions (-3 V $\leq V_{GS} \leq -2$ V). In the same region of I-V characteristics the device exhibits impact ionization phenomena which can be monitored by the increase of the negative (outgoing) I_G current induced by hole collection. The kink results to be slightly increased in B type samples, with the Ti length reduced by dry etching, while the I_G induced by impact ionization appears slightly reduced.

The kink mechanisms have been classified [5] from the following three points of view :

- 1) correlated with impact ionization only, i.e. kink originates from accumulation of free holes generated by impact ionization;
- 2) correlated with deep levels only, i.e. kink originates from capture and emission of carrier through those deep levels;
- 3) correlated with a combination of impact ionization and deep levels, in this case kink shows

complicated features depending on the kind and position of deep levels and impact ionization.

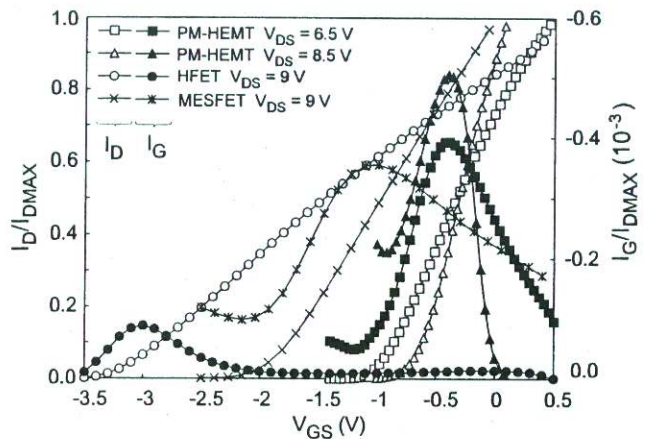


Fig 4. Normalized I_D and I_G induced by impact ionization in HFET, MESFET and PM-HEMT.

Figure 4 shows the increase of I_G induced by impact ionization, which exhibits the well known [4] bell shape and is confined in our B type devices for $V_{DS} > 5$ V and near pinch-off conditions. On the contrary in most of the power devices reported in the literature the bell shape of I_G is higher, larger and centered near $V_{GS} \approx 0$ V, i.e. in open channel conditions [2, 4].

Figures 5a and 5b report the $g_m(f)$ measured at low frequency (0.1 Hz - 10^5 Hz) in linear (Fig. 5a) and saturated (Fig. 5b) region of the A and B type device characteristics, respectively. In A type devices the frequency dispersion is negligible at all applied bias. On the contrary in B type devices a maximum decrease of g_m of 17% can be observed in the linear region and in open channel conditions ($V_{GS} = 0$ V), while the $g_m(f)$ decrease vanishes when the device is driven towards the pinch-off ($V_{GS} = -1$ and -2 V). Furthermore the $g_m(f)$ decrease is lower ($\leq 7\%$) at all V_{GS} when the device is operated in saturated regime, as shown in Fig. 5b.

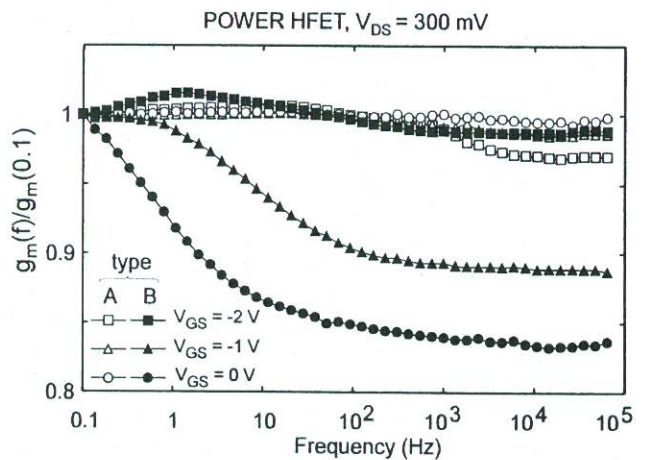


Fig. 5a. Transconductance frequency dispersion $g_m(f)$ measured at different V_{GS} , at constant $V_{DS} = 300$ mV in linear region on A-type (open symbols) and B-type (closed symbols) devices.

Data suggest that in B type devices deep levels, negatively charged, are present at the interface between the active device and the passivation layer

at the gate edges which cause a $g_m(f)$ frequency dispersion [2, 3] characterized by a decrease of g_m at increasing frequency as observed in our present devices.

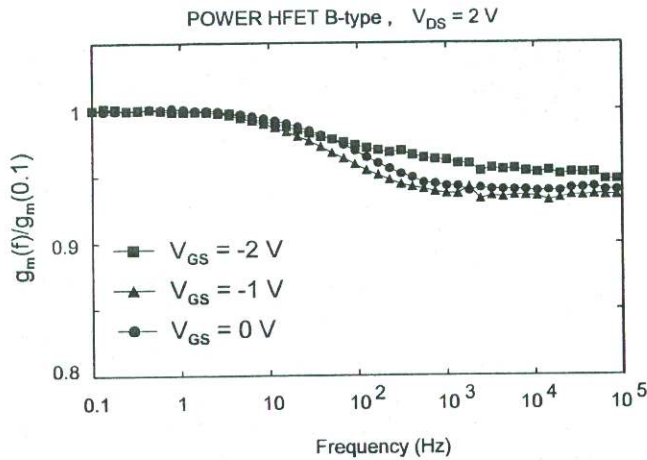


Fig. 5b. Transconductance frequency dispersion $g_m(f)$ measured at different V_{GS} , at constant $V_{DS} = 2$ V in saturated region on B-type device.

The frequency dispersion of g_m depends on the temperature; higher temperatures correspond to higher emission rates and as a consequence the decrease of g_m takes place at higher frequency. An activation energy $E_a = 0.67$ eV has been obtained for these deep levels.

IV. DEGRADATION MECHANISMS

To evaluate hot electron effect hardness, devices have been step-stressed in hot electron regime. Three different accelerated step-stresses have been used, namely:

- i) high breakdown reverse current, I_{BGDO} , between gate and drain with source floating, hereafter indicated as HBRC. Steps of 0.5 mA/mm for 20 hr. have been selected up to 3 mA/mm.
- ii) high I_G current induced by impact ionization at high V_{DS} voltages in near pinch-off conditions, hereafter indicated as HGCI. Steps of increasing I_G (125 μ A/mm) for 20 hr. have been selected up to 1.5 mA/mm. I_G was increased keeping V_{GS} constant at the value corresponding to the maximum of the I_G bell and increasing V_{DS} .
- iii) high I_D current and V_{DS} voltages in open channel conditions hereafter indicated as HCV. Devices have been biased in points A ($V_{GS} = 0$ V, $V_{DS} = 3$ V), B ($V_{GS} = 0$ V, $V_{DS} = 5$ V), and C ($V_{GS} = 0$ V, $V_{DS} = 7$ V) marked in Fig. 3 for 20 hr, respectively. All step-stresses have been performed at room temperature.

After stresses A type devices, without Ti length reduction, exhibit negligible changes of their electrical characteristics. On the contrary, non negligible changes, even if of reduced amount, have been observed after stresses in B type devices with Ti length reduction by selective dry etching. The main changes induced by accelerated stresses in B type devices are:

- a) a remarkable and permanent increase of gate-

drain breakdown voltage (often referred as *breakdown walkout*) is induced by HBRC and HGCI step stresses. As reported in Fig. 6 the breakdown voltage of gate-drain diode increases from -16 V to -19 V after the high I_{GD0} step-stress. This increase of gate drain breakdown voltage improves the leakage current and the breakdown of the HFET device when operated as transistor.

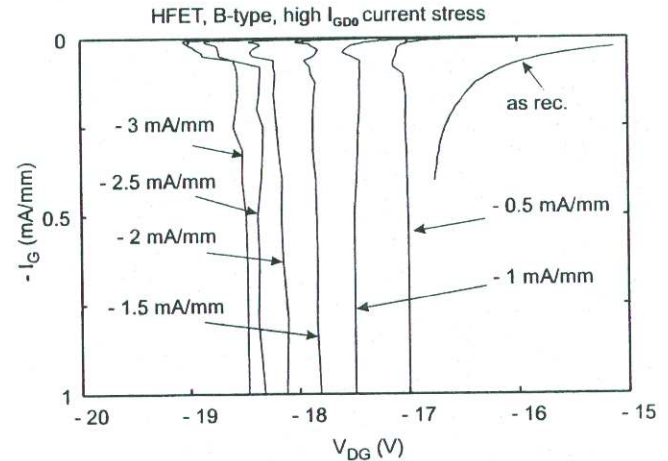


Fig. 6. Gate drain diode breakdown characteristics measured in B-type devices after step-stress at different high breakdown reverse current, I_{GD0} .

Permanent gate-drain breakdown walkout has been already reported in GaAs based HEMT [6] and PM-HEMT [7] stressed in two terminal configuration (with source and drain shorted) and three terminal configuration and biased in hot electrons and/or impact ionization conditions, respectively.

In both cases the increase of the gate-drain breakdown voltage has been attributed to an accumulation of negative charge in deep-surface states located at the edges of the gate.

Furthermore we have measured an increase of the breakdown voltage of the device operated in closed channel conditions at increasing temperature suggesting that impact ionization in the channel is the main reason of breakdown.

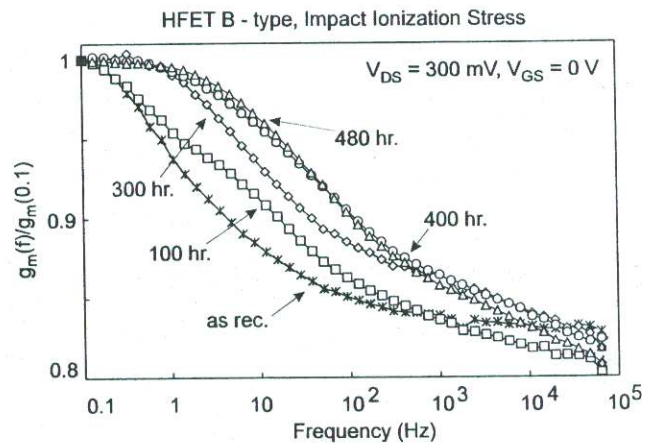


Fig. 7. Transconductance frequency dispersion $g_m(f)$ measured in linear region ($V_{DS} = 300$ mV and $V_{GS} = 0$ V) of B-type device after high I_G current induced by impact ionization step-stresses.

b) A change of transconductance frequency dispersion was observed after high current induced by impact ionization stress. As reported in Fig. 7 after the stress the fall down of $g_m(f)$ shifts towards higher frequencies. Furthermore the temperature dependence of $g_m(f)$ exhibits an activation energy of 0.4 eV suggesting that a new deep level is created by hot carriers at the drain side gate edge which dominates the $g_m(f)$ frequency dispersion.

c) A decrease ($\leq 6\%$) of I_D in particular at low V_{DS} , due to a decrease ($\cong 200$ mV) in the absolute value of the threshold voltage (ΔV_T) has been observed after high I_D and high V_{DS} stress in open channel conditions. These decreases are consistent with an increase in the negative charge trapped in the space charge region under the gate and extending under the region at the gate edges due to the presence of surface states. A strong correlation between the current decrease, ΔI_D , and the product of the transconductance and the threshold voltage shift, $g_m \Delta V_T$, measured either in linear ($V_{DS} = 0.1$ V) or in saturated region ($V_{DS} = 4$ V) has been observed as reported in Fig. 8, [8].

Most of this last degradation recovers if unbiased device is stored at 100(125) °C for 10(36) hr. as shown in Fig. 9.

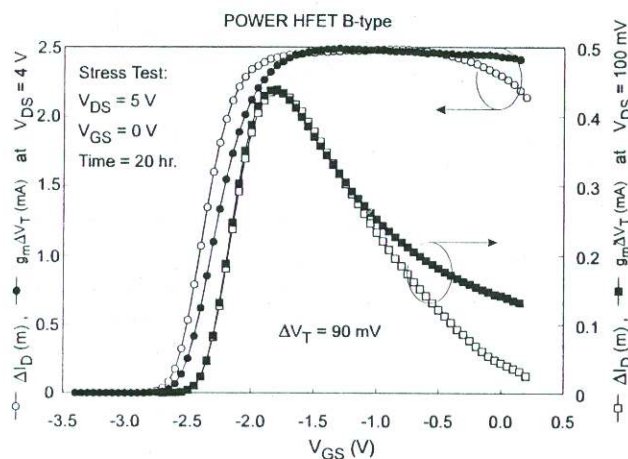


Fig 8. Drain current decrease, ΔI_D , measured at $V_{DS} = 100$ mV and $V_{DS} = 4$ V after HCV step stress up to $V_{DS} = 5$ V for 20 hr.

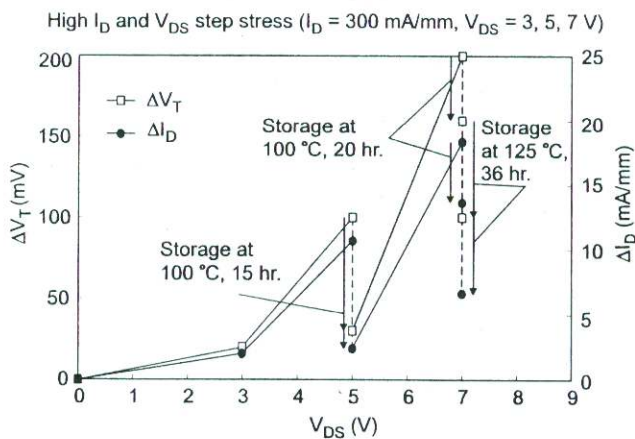


Fig 9. Changes of threshold voltage, ΔV_T and drain current, ΔI_D , induced by high I_D and V_{DS} step stress and their recovery after unbiased thermal storage.

This recoverability of ΔI_D and ΔV_T is an indication that these degradations are due to preexisting deep levels that get negatively charged during the stress (and move back to the equilibrium condition as the device is stored after the stress is over).

The hot electron degradation observed in the present HFET's is much lower than the one reported in the literature for power HEMT and PM-HEMT based on GaAs [2, 4].

V. DISCUSSIONS AND CONCLUSIONS

We have designed and developed a process for GaAs based HFET which results to be suitable for large production, weakly affected by deep levels at the edges of the gate, able to reduce impact ionization induced I_G and to confine it in a small part of I-V characteristics. Furthermore developed devices appear more robust against hot electron effects than those reported in the literature [2, 4, 8]. In fact small changes of device characteristics have been observed after hot electron step stresses only in devices where Ti gate length was reduced by selective dry etching and the $Al_{0.25}Ga_{0.75}As$ surface results in direct contact with SiN passivation. Changes are permanent when new deep levels are generated at the interface between the active device and passivation layer at the gate edges, while changes are recoverable when hot carriers modulate the charge trapped in the space charge region laying under the gate and the AlGaAs recessed area at the gate edges. Transconductance frequency dispersion has been proved to be an excellent analytical technique for monitoring the deep levels induced by the process and to allowing us to optimize device design and processes.

References

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