Two-Stage Adaptive Power Amplifier MMIC for Handset Applications

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***Abstract* — A high-linearity and high-efficiency MMIC power amplifier is demonstrated adopting a new on-chip adaptive bias circuit, which improves efficiency at the low output power level and linearity at the high output power level automatically. The intelligent two-stage W-CDMA power amplifier using the newly proposed adaptive bias circuit extends the maximum linear output power of 0.6dB and exhibits an improvement of average power usage efficiency by 1.85 times with a quiescent current of 36mA.**

I. Introduction

W-CDMA is one of the leading standards for the 3G wireless communication systems and adopts a spectrally efficient HPSK (hybrid phase shift keying) as a digital modulation scheme. But a non-constant envelope of the W-CDMA signal results that the power amplifier operates with a large amount of back-off of the output power to achieve a high linearity. Also, power amplifiers need a high-efficiency characteristic over a wide output power range for the overall power efficiency because the most frequently used power level is not the maximum output power but ranges from –20dBm to 15dBm [1]. A back-off of the output power to the most probable output power makes a significant decrease in efficiency with a fixed dc power supply. The techniques for achieving the high efficiency at the most probable output power are being highlighted recently as the most significant issues in designing power amplifiers for mobile handsets. The power amplifier employing DC-DC converters [2]-[4] operated in near saturation region at all power levels with a variable supply voltage to the input power, generating higher efficiency. Switched gain stage power amplifier [5] bypasses the power stage for the high efficiency at the low output power level. However, these techniques need additional components such as DC-DC converters or switches, which result in a significant increase of the module size and cost that make the power amplifier not suitable for the mobile terminals. The dual chain power amplifier [6] uses a smaller P1dB amplifier for the high efficiency at the low output power region, but the parallel architecture resulted in a large MMIC size.

With the conventional Class AB bias, power amplifiers are hard to exhibit the high efficiency at the low output power level and the high linearity at the high output power level. To overcome these problems, we propose an on-chip adaptive bias control circuit in this work. The proposed adaptive bias control circuit supplies a low quiescent current at the low output power level for the high efficiency, and the quiescent current increases adaptively with the input power to supply higher quiescent current at the high output power level for the high linearity. The circuit has been successfully implemented to the W-CDMA power amplifier together with the shunt capacitor linearizer [7]. The power amplifier shows an average power usage efficiency increase by 1.85 times and a maximum linear output power by 0.6dB with the adaptive bias control circuit.

II. Adaptive Bias Control Circuit

The conventional Class AB power amplifier with a fixed bias current exhibit inherently low efficient and high linear characteristics at the low output power level, and high efficient and low linear characteristics at the high output power level. Therefore adaptively biased power amplifiers according to the output power level, such as a low quiescent current at the low output power level and the increased quiescent current with the increased output power level, is designed for both high linear and efficient characteristics simultaneously over a broad range of the output power.

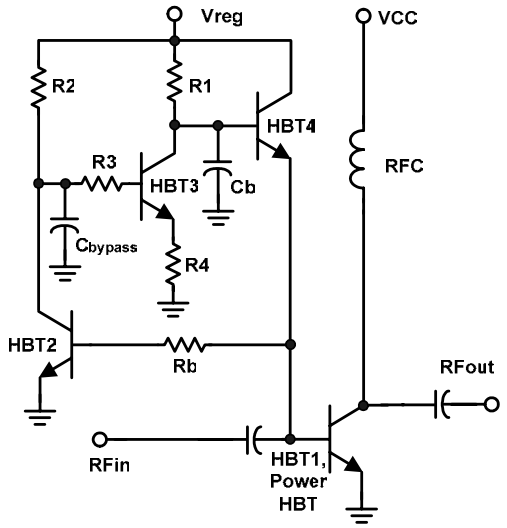

Fig. 1. Schematic diagram of the adaptive bias control circuit for the power stage.

Fig. 1 shows the proposed adaptive bias control circuit for the power stage. Transistor HBT2 senses the

incoming input power, and the resistance of Rb and emitter area of the HBT2 determine the amount of the incoming power to the transistor HBT2. The base voltage of the HBT3 and HBT4 is determined as follows:

$$V_{B3} = Vreg - (I_{C2} + I_{B3})R2 - I_{B3}R3 \quad (1)$$

$$V_{B4} = Vreg - (I_{C3} + I_{B4})R1 \quad (2)$$

The transistor HBT1 and HBT2 are biased to the Class AB with a low quiescent current for the high efficiency at the low output power level, and thus the collector currents are increasing function to the input power. Therefore, the collector current of the HBT2(I_{C2}) increases with the input power and the amplified power are bypassed through the capacitor C_{bypass}. The increased current of I_{C2} decreases the base voltage of the HBT3(V_{B3}) in equation (1), hence the collector current of the HBT3 decreases. Then, the decreased I_{C3} makes in the increase of the base voltage of the HBT4(V_{B4}) in equation (2), causing the emitter current of HBT4 and the collector current of the HBT1 to increase. Therefore the quiescent current of the adaptive bias control circuit is increasing function to the input power, and supplying higher quiescent current than the conventional fixed bias at the high output power region will result in high linearity with the trade-off efficiency. Finally, high efficiency at the low output power level and high linearity at the high output power level can be achieved simultaneously.

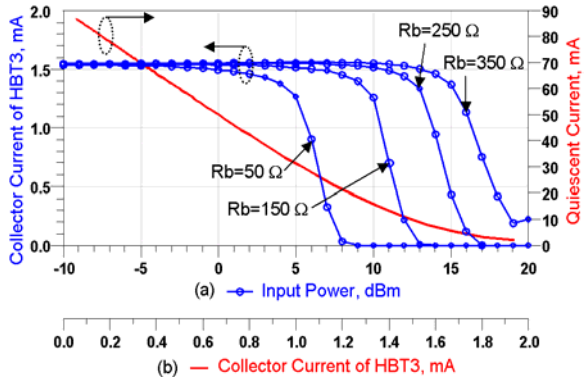

Fig. 2. (a) Simulated collector current of HBT3 as a function of input power to the power amplifier for the different four resistor values of Rb. (b) Simulated quiescent current of HBT1 as a function of the collector current of HBT3.

The resistor Rb and emitter area of HBT2 affect the overall operation of the adaptive bias control circuit. With a 50Ω of Rb, the sensing transistor HBT2 has a sufficient incoming RF power, then, I_{C2} starts to increase at the small input power of -2dBm, decreasing the I_{C3} as shown in Fig. 2 (a). But with a 350Ω of Rb I_{C3} starts to decrease at the high input power of about 11dBm. The collector current of HBT3 directly affects on the quiescent current of HBT1 as shown in Fig. 2 (b). Fig. 3 shows the dependence of the collector current of HBT3(I_{C3}) on the emitter area of HBT2 as a function of the input power. Because the increase ratio of I_{C2} under Class AB operation is proportional to the emitter area of the HBT2, the decreasing ratio of I_{C3} with the input power is the smallest when the emitter area of the HBT2 is 30μm^2. The optimum value of Rb and emitter area of HBT2 have to be chosen by maximizing the linearity/efficiency trade-off because the variation of I_{C3} directly affects the quiescent current of HBT1 as shown in Fig. 2 and Fig. 3.

The shunt capacitor Cb (the function of which is described in detail at [7]) at the base node of HBT4 in Fig.1 is used as a linearizer. The capacitor with the base-emitter diode of the transistor (HBT4) compensates the decreased base bias voltage of the HBT1 caused by the increased input power.

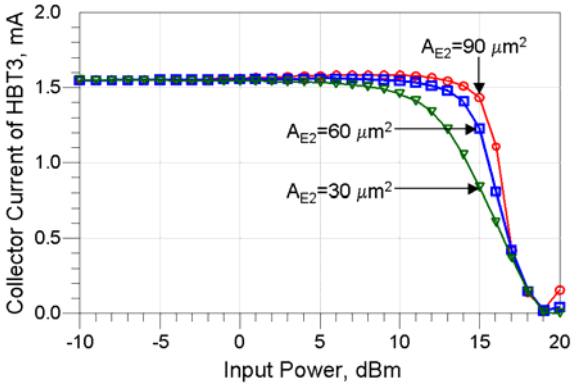

Fig. 3. Simulated collector current of HBT3 as a function of input power for the three different emitter areas of HBT2.

III. Implementation to MMIC Power Amplifier

A two-stage W-CDMA MMIC power amplifier that implements the proposed adaptive bias circuit is fabricated as shown in Fig. 4. The MMIC power amplifier is demonstrated using multiple fingers of unit transistor of 60 μm^2-emitter-area InGaP/GaAs HBT : 1,920 μm^2 for power stage and 480 μm^2 for drive stage. The total chip size of the MMIC was as small as 1,050x750 μm^2 including input matching, inter-stage matching, and the adaptive bias circuits with a shunt capacitor linearizer[7].

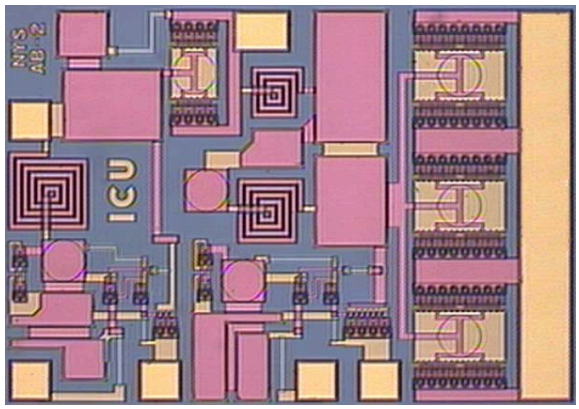

Fig. 4. Photograph of the fabricated two-stage MMIC power amplifier.

IV. Measurement Results

Fig. 5 shows the measured adjacent channel leakage ratios (ACLRs) for the adaptive bias circuit with a

quiescent current of 36mA and the conventional one adopting the shunt capacitor linearizer [7] with a quiescent current of 86mA. The ACLR is measured using a 3.84Mcps W-CDMA modulated signal (DPCCH+1DPDCH) in a 5 MHz offset frequency band under a 3.4V supply voltage. The maximum output power meeting the ACLR of –33dBc is 28.3dBm for the adaptive one and 27.7dBm for the conventional one, exhibiting 0.6dB increase of maximum linear output power.

The measured quiescent current of the power amplifier with the adaptive bias circuit is 36mA, and the measured collector current as a function of output power is shown in Fig. 6 in comparison with the conventional Class AB power amplifier with the quiescent current of 86mA. In addition, the power amplifier Probability Distribution Function (PDF) [1] based on an IS-95 CDMA urban environment is illustrated in Fig. 6. The adaptively biased power amplifier operates with the collector current at less than half of the fixed bias under the 5dBm output power, thereby generating more than two times higher efficiency in the most probable output power range.

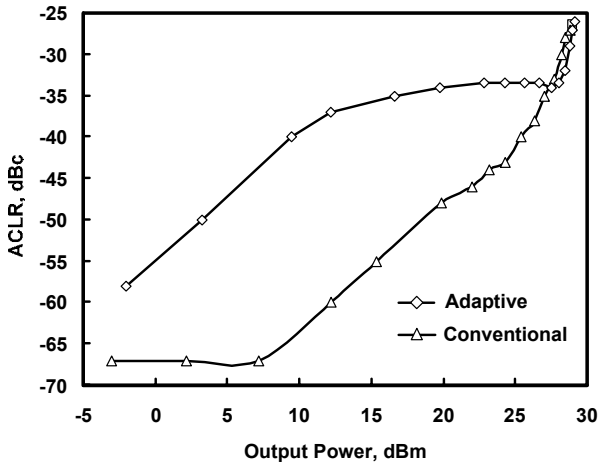

Fig. 5. Measured ACLRs of the power amplifier with adaptive and conventional bias circuit.

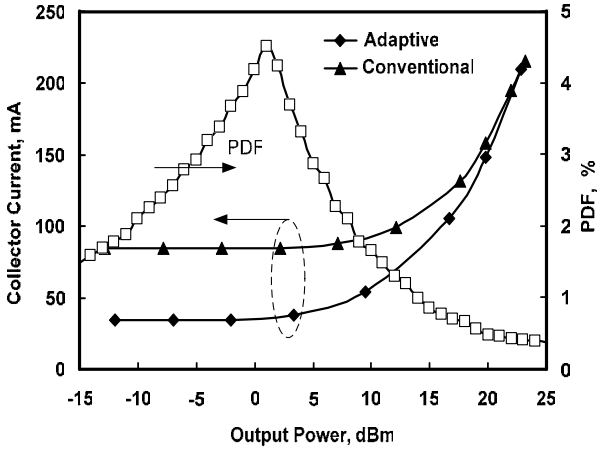

Fig. 6. Measured collector current of the power amplifier with the adaptive bias and the conventional bias circuit. And, power amplifier probability density function based on an IS-95 CDMA urban environment [1].

The simulated quiescent current was 120mA over a 26dBm output power for the adaptively biased power amplifier. Fig. 7 shows the measured gain and power added efficiency (PAE) of the power amplifier with the adaptive bias and fixed bias circuit as a function of output power. The gain is 23dB for the low output power and increases 29.7dB at the output power of 26dBm with the adaptive bias circuit. A gain expansion of up to 6.7dB occurs at the high output power region due to the high quiescent current of 120mA with the adaptive bias circuit. PAE is measured as 46% (49.5%) at the 28.3dBm output power with the adaptive (conventional) bias circuit. The 3.5% decrease of PAE, which negligibly affects the overall efficiency because the power amplifier PDF shows a low value at that power level, is a trade-off with the ACLR increase of 4dB.

To evaluate the efficiency improvement, average power usage efficiency in [2] is defined by:

$$\eta_{usage} = \frac{\overline{P_{out}}}{\overline{P_{in}}} \qquad (3)$$

, where $\overline{P_{in}}$ and $\overline{P_{out}}$ are the average RF output power and input DC power with the power amplifier PDF, respectively. The average power usage efficiency is calculated as high as 7.44%(4.03%) with the adaptive(conventional) bias circuit, generating 1.85 times increase of the battery usage time.

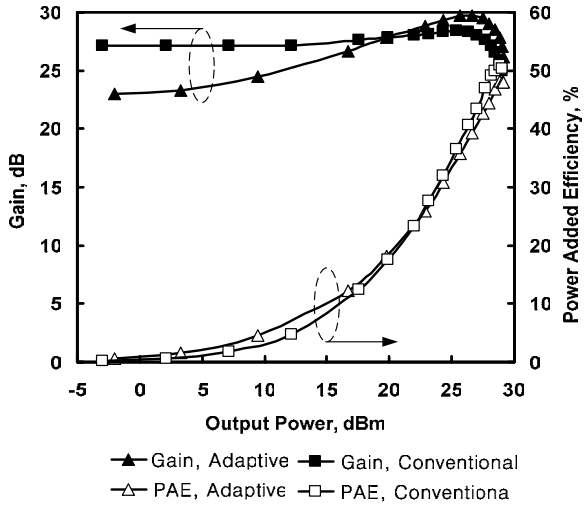

Fig. 7. Measured gain and power added efficiency of the power amplifier with the adaptive bias and the fixed bias circuit.

Table 1 summarizes the measured output power and power added efficiency for ACLR of –33dBc with W-CDMA modulated signal for two different conditions along with the average power usage efficiency.

Table 1. Measured results of the W-CDMA power amplifier under an ACLR of -33dBc

Bias Condition	Pout, dBm	PAE, %	η_{usage}, %
Conventional	27.7	46.7	4.03
Adaptive	28.3	46	7.44

V. CONCLUSION

An on-chip adaptive bias circuit controlling the quiescent current adaptively to the power level is proposed for both high efficiency and linearity. The adaptive bias control circuit supplies a low quiescent current to the power amplifier when the input power is small and this current increase according to the power level automatically. A W-CDMA MMIC power amplifier with the proposed adaptive bias control circuit achieves an average power usage efficiency improvement by 1.85 times with a small quiescent current of 36mA under a 3.4V supply voltage. The adaptive bias circuit is very attractive in mobile handset power amplifier because it is integrated on a chip with small area.

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