Low cost MMIC chipset for VSAT ground terminals

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***Abstract* — This paper presents results of a Ka-band VSAT Ground Terminal MMIC chipset developed in a cost reduction context. The first one, a Low Level Multifunction designed for up-conversion with high gain driver, exhibits a 17dB conversion gain with an associated P_{1dB} output power close to +18dBm. The second one, a High Power Amplifier with embedded power detection, delivers 2W RF output power associated with 24dB of linear gain. This chipset combines performance, integration and low cost.**

I. Introduction

The rapid growth of multimedia applications leads manufacturers and involved parties to furnish cheaper and more efficient equipment, in a competitive and difficult business context. The Very Small Aperture Terminal (VSAT) development fits this dynamic to address a mass market and to provide residential and professional users with real-time interactive satellite communications solutions : telephony, videoconferencing, internet, collaborative work …

The Satellite Terminal Architecture (Figure 1) consists in two main units : the Input Door Unit (IDU) providing the modem and baseband functions, the power supply and the interface with the user equipment, and the Output Door Unit (ODU) containing the antenna and the RF electronics.

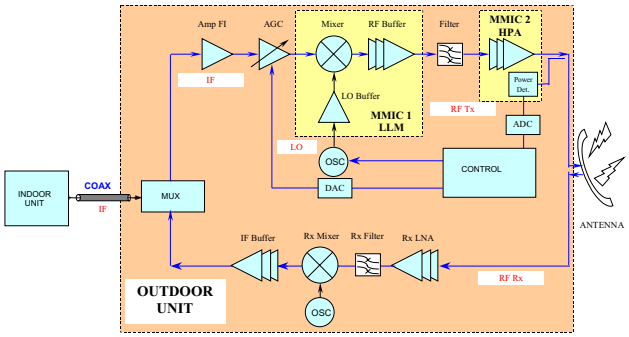

Fig. 1. Terminal architecture

If there is no getting away from the use of MMIC technology, to cost reduction point of view, it becomes essential to integrate several functions. The analysis of ODU TX path, which constitutes certainly the most expensive part, shows that the best way to minimise terminal cost is to design a chipset of two specific MMICs : one called Low Level Multifunction for the up-converter including high gain driver, and the other one called High Power Amplifier, for the output power stage with embedded power detection. Designs and results of these two MMICs are described and presented hereafter.

II. Low Level Multifunction MMIC

The leading role of the multifunction circuit is to up-convert L and S Intermediate Frequency (IF) bands to Ka Radio Frequency (RF) band, by ensuring both a high conversion gain with sufficient output power level, in order to drive directly the terminal output power MMIC. The mixer part, based on subharmonic topology, avoids on the one hand, the use of a frequency doubler for the Local Oscillator (LO), and on the other hand, allows to naturally reject the second LO harmonic (2LO), which appears close to the useful RF signal. A Ku-frequency band LO buffer is integrated on MMIC to reduce down to +6dBm the required input LO power. This LO stage is designed to operate in compression regime, in order to maintain global performance regarding to possible drive input level variations. The main topology of the Low Level Multifunction MMIC is presented on figure 2.

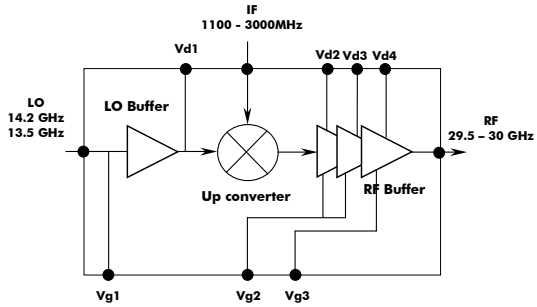

Fig. 2. Topology of LLM MMIC.

We intentionally chose a topology without image rejection, because an external selective filter cancels or drastically reduces this parasitic signal.

MPA2 process from TOSHIBA foundry has been retained to obtain the best trade-off between performance and low cost. This 0.3µm gate length double δ-doped PHEMT technology is dedicated to medium power applications. The current gain cut-off frequency is about 32GHz, the Maximum Available Gain is 10 dB @ 30 GHz, the current density is greater than 200mA/mm and V_{DSmax} reaches 12V.

An intensive characterisation of passive and active test elements have been performed, in order to develop an accurate electrical models library. On-wafer measurements have been systemically done in the input and output plans of device under test. Figure 3 shows a I(V) response of 8x50µm FET measured under pulsed conditions.

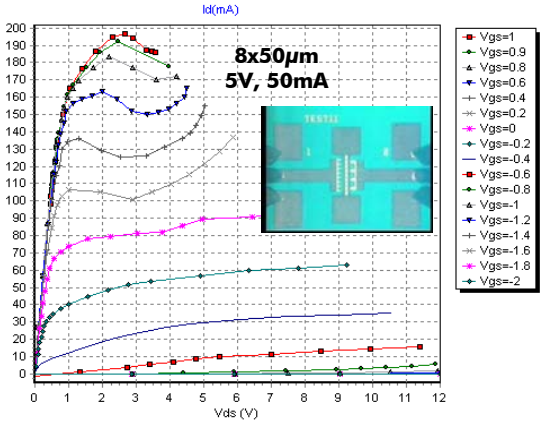

Fig. 3. Measured pulsed I(V) of 8x50µm FET.

In addition to electrical modelling, the circuit has been designed with intensive ElectroMagnetic (EM) simulation, in order to take into account the potential coupling effects due to the high integration (in particular with output RF buffer). Specific test patterns have been measured and compared to EM simulations performed with MoMentum software (ADS Agilent), in order to accurately define and calibrate the simulation parameters. Figure 4 compares Σ Sij errors (relative to measurement) obtained from electrical and ElectroMagnetical simulations, of a test structure including coupled lines and gaps. It clearly appears that EM results are always better and so confident to measurement.

$$\sum_{ij} \left| \frac{Sij_{\text{sim}} - Sij_{\text{mes}}}{Sij_{\text{mes}}} \right|$$

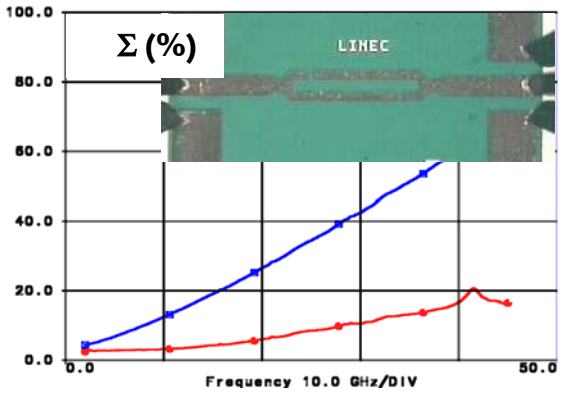

Fig. 4. Σ Sij errors versus frequency
(→ electrical simulation, → ElectroMagnetical simulation).

The LLM surface area is 6.5mm^2, and its DC consumption is less than 1W under 5V. Figure 5 presents the layout of the circuit.

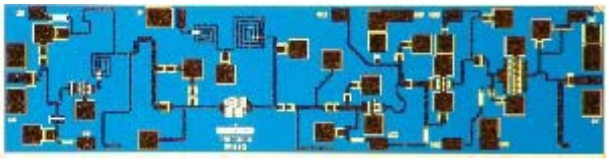

Fig. 5. Layout of LLM MMIC.

The one-stage Ku frequency band LO buffer drives the subharmonic mixer part based on cold antiparallel diodes. The [1.1-1.6 GHz] and [2.5-3 GHz] input IF bands are converted to [29.5–30 GHz] RF band. Then, output Ka signals are largely amplified by a 3-stages buffer to reach both high conversion gain and sufficient output power for last stage terminal driving.

20 functional dice have been measured on-wafer to appreciate and to quantify the spread of performance. Conversion gain and output P2LO leakage versus IF frequency and conversion gain versus IF power, measured at LO=13.5GHz, are presented on Figure 6. The LLM exhibits a 1dB output power greater than +18dBm with an associated average linear conversion gain of 17dB. Output P2LO leakage is less than –10dBm.

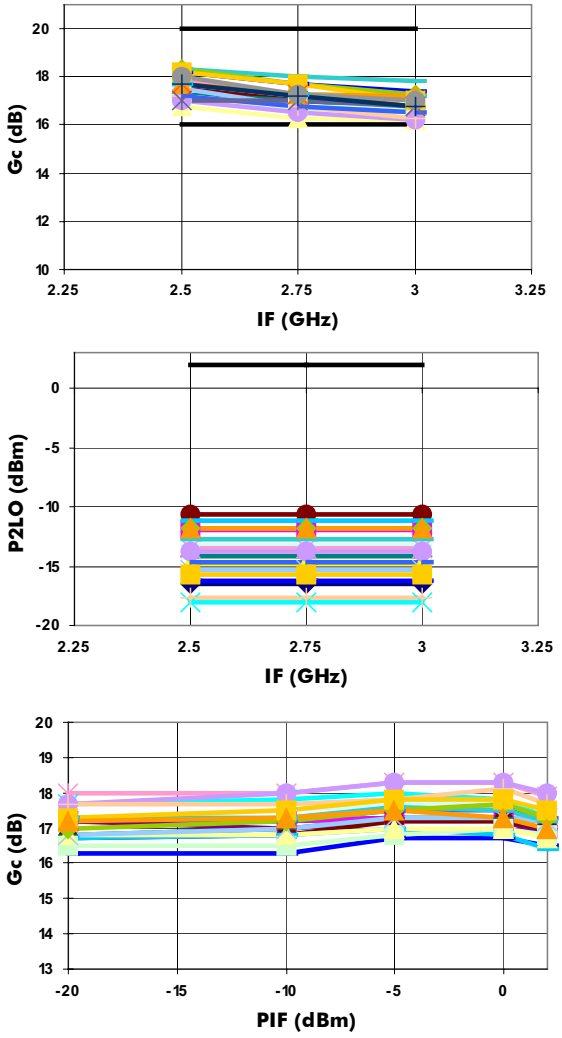

Fig. 6. Measured conversion gain and output P2LO leakage versus IF frequency and conversion gain versus IF power @ LO=13.5GHz.

This Multifunction MMIC, including LO buffer, subharmonic mixer and output RF buffer, combines performance, integration and low cost.

III HIGH POWER AMPLIFIER MMIC

The 3-stages High Power Amplifier MMIC (HPA) supplies over 2W of output power with 24dB of linear gain in the 28-30 GHz VSAT frequency band. This circuit is produced on a very low-cost, high performance, commercially available 0.15µm power-PHEMT process. The HPA has the highest gain/stage ratio at Ka-band reported to date [1, 2].

The high gain eliminates the costs associated with using another amplifier to drive the HPA. The HPA uses less chip area than comparable amplifiers that uses more stages of gain [2]. The high output power and gain in a small chip area along with the inexpensive 0.15um process make this low cost HPA very attractive for a VSAT terminal application.

The power amplifier was designed using measured small-signal S-parameters of transistors and simulated load-pull in the useful frequency band. The output gate periphery is 6.4 mm, stage 2 gate periphery is 2.56 mm, and the input stage gate periphery is 0.96 mm. The stability is ensured by proper compact R//C networks in the gate access of each transistor, odd mode stabilizing elements were optimized with the current probe method described in [3]. All the design was performed using AWR MWO 2003 software.

A layout of the high power amplifier is shown in Figure 5. The chip size is 3.5x 3.5mm². The process uses transistors individual source vias and adjacent PHEMTs share outside source vias to reduce chip width. It also includes a diode power detector associated with its reference voltage.

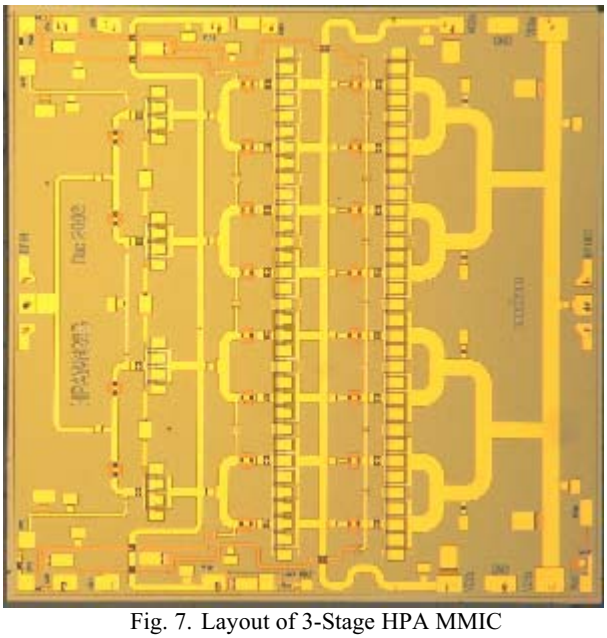

Fig. 7. Layout of 3-Stage HPA MMIC

The prototype amplifier was fabricated at Win Semiconductor on their 0.15µm power-PHEMT process with a substrate height of 100µm.

Small signal measurement has been performed under reduced bias conditions (V_{DS}=2V,V_{GS}=-0.9V leading to P_{DC}<1.5W) on 30 chips randomly picked on two wafers. Every tested circuit is fully working leading to 100% yield, thanks to the high reproducibility of the process. On-chip power measurements has also been performed in the same bias conditions, these results are shown in Figure 6. A difference of 0.7dB on the average P_{1dB} value can be noticed between the two wafers : average P_{1dB}=22.9 dBm on wafer A and average P_{1dB}=22.2 dBm on wafer B. This is linked to a small difference on the pinch off voltage for the two wafers as the circuits are biased with a constant gate voltage.

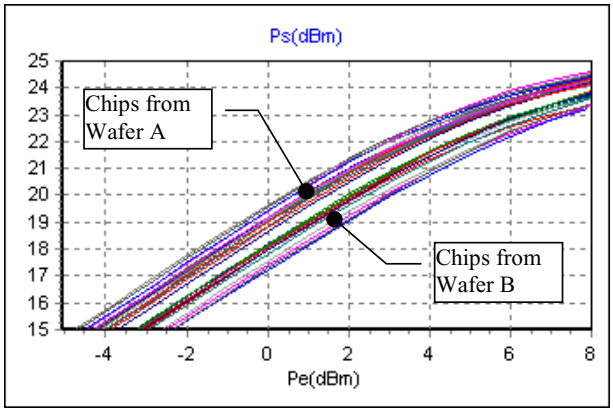

Fig. 8. . Measured Output power at 29 GHz under reduced bias conditions

Some chips were mounted on CuW carriers for better heat spreading (as shown in Figure 9) and then measured on a probe station at ambient temperature. The quiescent bias is V_{DS}=5V, I_{DS}=2A. As the effect of the RF wiring has been taken into account in the early stage of the design, we added 50Ω small lines on alumina substrate to be able to wire the 25µm RF connections.

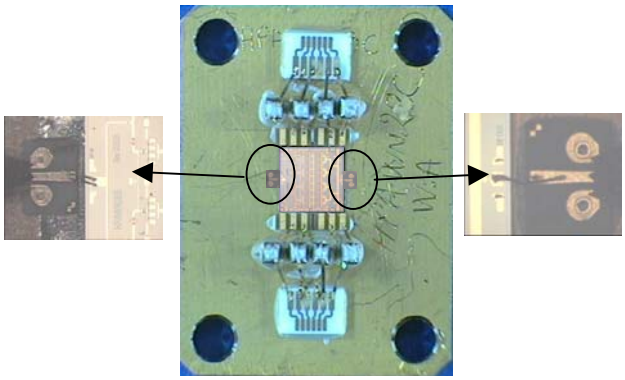

Fig. 9. HPA in test fixture

The measured S-Parameters of two samples are shown in Figure 10 : the I/O return loss are better than -12dB in the useful bandwidth and the S21 is greater than 24 dB and remains fairly flat.

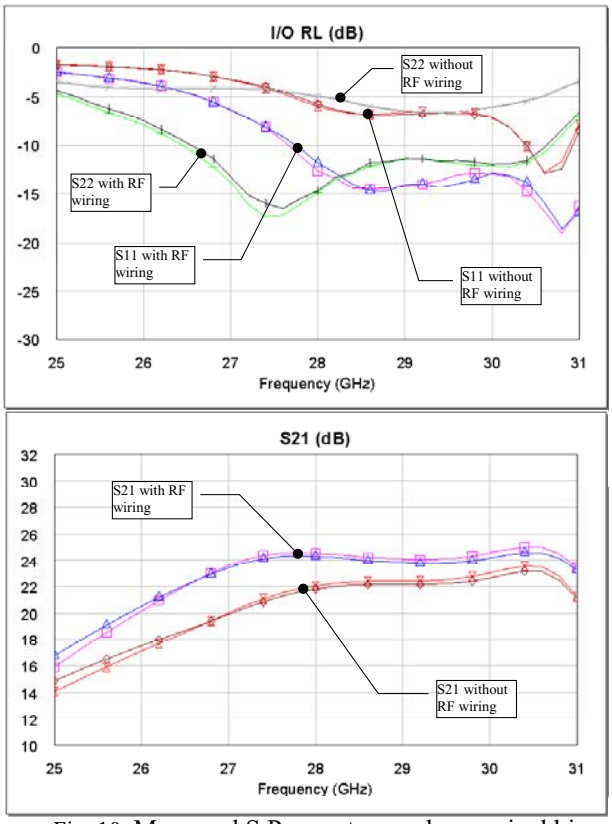

Fig. 10. Measured S Parameters under nominal bias conditions including RF wiring effects

The measured output power vs. input power of the amplifier is shown in Figure 11. As can be seen the amplifier supplies an output power of 2W at 28 and 29 GHz.

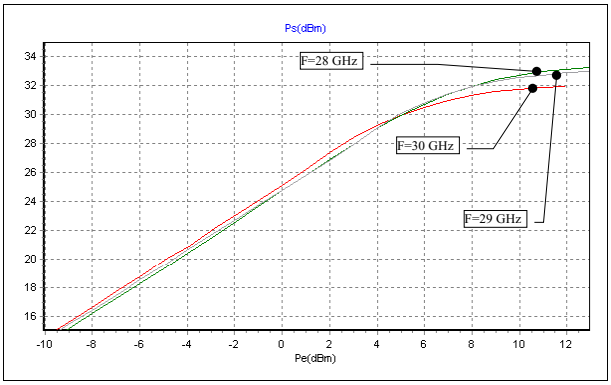

Fig. 11. Measured power performance under nominal bias conditions at 28,29 and 30GHz including RF wiring

The power gain and the output power vs. frequency are shown in Fig. 9 an 10. The measurement have been performed in linear conditions (Pin=-10dBm) and for an input power leading to 1dB gain compression at 28GHz (Pin=10dBm). For the higher frequencies, the output power decreases and the compression increases, this is due to an optimum impedance mismatch that has been clearly located in the output combiner. This mismatch can be easily corrected for a future production run.

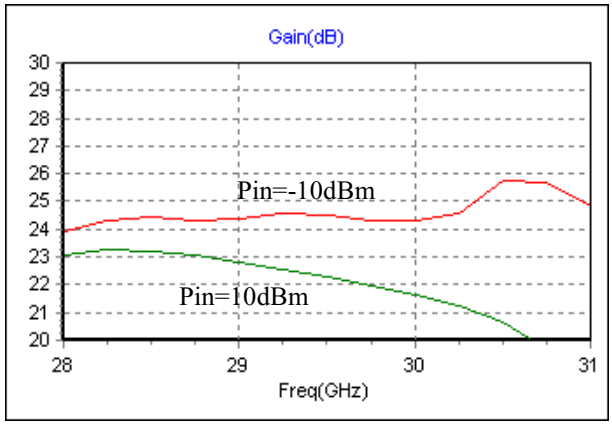

Fig. 12. Measured power gain vs. frequency under nominal bias conditions including RF wiring

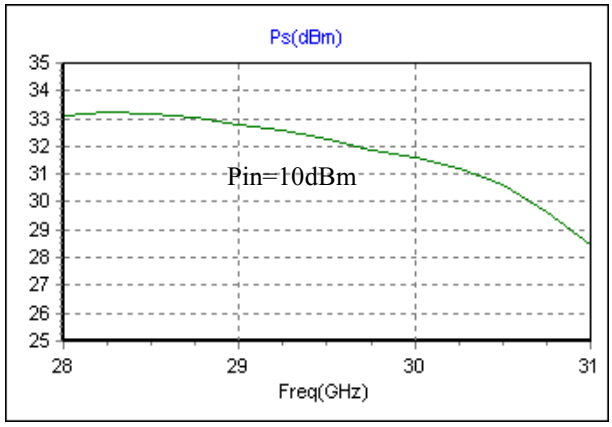

Fig. 13. Measured output power vs. frequency under nominal bias conditions including RF wiring at Pin=10dBm

IV. Conclusion

A new challenging architecture for the RF chain of VSAT ground terminals has been demonstrated. Due to the high performance of the developed MMIC, the RF Tx chain only uses 2 MMIC instead of at least 3 in our competitor's architecture. The surface cost of the chipset is reduced, thanks to the high integration of the MMIC functions : 12.25mm² for the HPA and 6.5 mm² for the LLM

References

[1] A compact 30GHz MMIC High Power Amplifier in Chip and Packaged form. K.S. Kong, et al.; 2002 IEEE GaAs Digest, 37-39

[2] A Balanced 2 Watts Compact PHEMT Power Amplifier For Ka-Band Applications. S. Chen, et al.; 2003 IEEE MTT-S IMS Digest, 847-850

[3] Analysis and elimination of parametric oscillations in monolithic power amplifiers. A. Anakabe, et al.; 2002 IEEE MTT-S IMS Digest, 2181 – 2184