A High-Efficiency HBT-based Class-E Power Amplifier for 2 GHz

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***Abstract* — A Class-E power amplifier (PA) based on a GaAs heterojunction bipolar transistor (HBT) is presented. The single-ended single-stage PA delivers 24 dBm of output power at 2 GHz, achieves a peak power added efficiency (PAE) of 68% and exhibits an excellent transducer power gain higher than 16 dB. The PAE remains high over a wide output power range. The circuit contains the standard 50-Ohm input and output match and is capable of high-efficiency power amplification of constant-envelope signals, which has been demonstrated with the GMSK signal. Both lumped- and distributed-components concepts for the practical implementation of the load network are presented and discussed.**

I. Introduction

High-efficiency RF power amplifiers are required for many sorts of wireless applications. Among several types of switching-mode amplifiers, the Class-E configuration is the most suitable for RF operation. Since its introduction [1], the Class-E has aroused a lot of interest in the scientific circles and a significant amount of research has been done on this intriguing type of circuit. It has been implemented in different technologies and at different frequency bands [2]-[7].

In many papers it is shown that, when a Class-E PA is designed with a finite value of the DC-feeding inductance, the circuit elements deviate from their nominal values. The same holds for variations in the duty cycle, in the Q-factor of the load network, or in the transistor current rise- or fall-time. However, when all these effects are simultaneously combined, a fully analytical and exact approach to the Class-E PA design becomes very difficult. Basically, the designer faces an analytically intractable problem and needs to employ other design techniques.

In this paper, we present a Class-E PA design for operation at 2 GHz and an output power level of 24 dBm. The circuit is designed by combining the well-known theory of the Class-E operation with an experimental approach based on load-pull simulations. The paper is organized as follows. In section II, the design procedure is described in details. In section III, major details concerning the technology and the practical implementation of the circuit are given. Section IV reveals the measurement results, and the conclusion is drawn in section V.

II. Design Procedure

The Class-E PA circuit with conceptual input (IMN) and output (OMN) matching networks is depicted in Fig. 1. By means of a heavy overdrive, the transistor is operated as a switch, i.e. it is in saturation during the ON state, and in cut-off during the OFF state of the RF cycle. The circuit is designed for a conventional 50% duty-cycle operation, and the transistor is biased by V_{BB} to be at the verge of conduction. Inductors L_c, L_b and L_e represent the parasitic inductances of the collector-contact bondwires, base-contact bondwires and emitter back-side vias, respectively. It is important to take these parasitics into account, for accurate simulation. The parasitic L_e should be reduced to a minimum possible value, because it represents one of the sources of loss and spoils the Class-E operation.

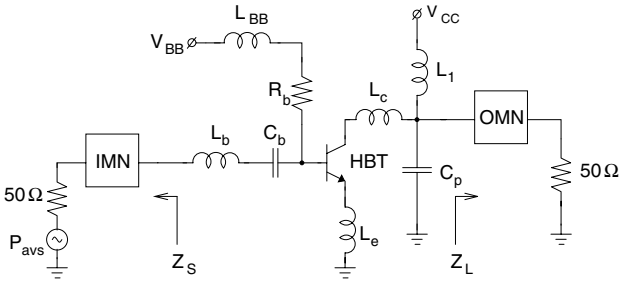

Fig. 1. Class-E PA circuit with conceptual input and output matching networks.

The elements R_b and C_b are the base-ballasting resistor and the DC-blocking capacitor, respectively, and they have been implemented on-chip. The DC-feeding inductors L_1 and L_{BB}, the shunt capacitor C_p, and the input and output matching networks are implemented off-chip, on the laminate substrate. This approach has been chosen to obtain greater flexibility in the design of matching networks and in the subsequent fine-tuning of the circuit.

The design of matching networks is a crucial part in the design of any power amplifier. For the Class-E operation in particular, it is necessary to provide the desired impedance not only at the fundamental, but at the harmonic frequencies as well. First we will focus on the design of the output matching network (OMN), which transforms the 50-Ohm termination to the desired load impedance, Z_L. The optimal load impedance is determined in the following manner. The conventional, ideal Class-E operation requires the following conditions in the load network:

$$Z_L(j\omega_c) = R_L(1+j1.152) \quad (1)$$

$$Z_L(jn\omega_c) \rightarrow \infty,\ n = 2, 3, 4\ldots \quad (2)$$

$$C_p = 0.1836/(\omega_c R_L) \quad (3)$$

where $\omega_c=2\pi f_c$ is the frequency of operation and R_L is the load resistance, determined by the supply voltage and the target output power as $R_L=0.577(V_{CC})^2/P_{OUT}$. By taking

P_{OUT}=250 mW (24 dBm), V_{CC}=3.6 V and f_c=1.95 GHz, we have calculated the values of $Z_L(j\omega_c)$ and C_p and used them as initial point for extensive load-pull simulations.

In Advanced Design System (ADS), we have created an interactive load-pull setup, and while keeping C_p constant, we have swept $Z_L(j\omega_c)$ across a range of values in the complex impedance plane. During this procedure, the load impedance values at higher harmonic frequencies, $Z_L(jn\omega_c)$, were kept at high (reactive) values, in accordance to (2). By performing load-pull simulations through harmonic balance type of analysis, we have monitored the simulated power, efficiency and gain, as well as the collector voltage and current waveforms, in order to be sure that the circuit remains in the Class-E operation.

In Fig. 2, the constant power added efficiency (PAE) and constant output power contours, obtained by the load-pull simulations, are plotted in the 50-Ohm Smith impedance chart. The two optimal impedance points are clearly indicated, but they do not coincide. This is a normal behavior of the Class-E PA. In our design, we have focused on obtaining an optimum efficiency.

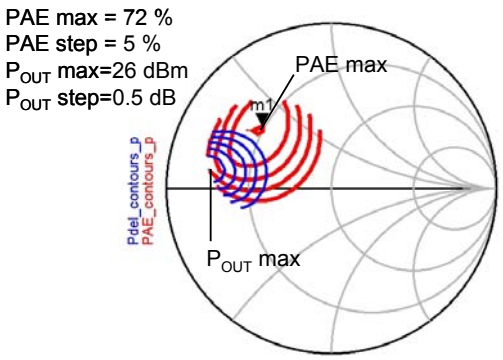

Fig. 2. Load-pull simulation of the Class-E power amplifier.

Once the optimum load impedance has been found, the output matching network can be designed to transform the standard 50 Ohm termination to this optimum value. However, a real matching network will not produce infinitely high impedances at higher harmonics, as we initially assumed. Therefore, it is necessary to perform some additional fine tuning of the final load impedance value, by replacing the real values for the harmonic impedances $Z_L(jn\omega_c)$ in the load-pull setup, and carrying out several more iterations to find the optimal $Z_L(j\omega_c)$.

Having established the optimal value of the load impedance, we proceed with the design of the input matching network. Similarly to the load-pull simulations, we have performed extensive source-pull simulations, by varying the complex source impedance Z_S presented to the PA (see Fig. 1), and observing the circuit waveforms and key performance parameters. Again, an iterative procedure is performed here, because it is necessary to change Z_S, but to adapt the available source power P_{avs} as well. Basically, the goal is to drive transistor just sufficiently strong, so that it satisfactorily operates as a switch. Too much drive power can be detrimental, because it spoils the operation, due to the slow recovery of the transistor from saturation (the turn-off transient). Once the transistor is properly driven, further increase in P_{avs} does not bring any benefit, but rather leads to a drop in the PAE and gain of the PA.

When final optimal values of $Z_S(j\omega_c)$ and $Z_L(j\omega_c)$ are established, the input and output matching networks can be designed. In Fig. 3, the schematic of the input matching network is depicted. The elements in the lowpass L-section matching network are dimensioned to transform the 50 Ohm source impedance to the optimal source impedance of 1.9+j5.1 Ohms at the operating frequency of 1.95 GHz.

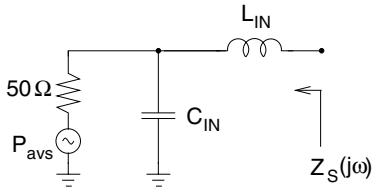

Fig. 3. Input matching network of the Class-E PA.

We have designed three versions of the output matching network. In principle, as long as the required load impedance is presented to the transistor, the PA will function properly, regardless of the implementation of the matching network. Therefore, we have demonstrated the high-efficiency Class-E operation with both lumped- and distributed-components output matching networks. In Fig. 4 – 6, the topologies of the designed and implemented load networks are shown. Load network LN1 is based on lumped components and is implemented by SMD 0201 discrete passives. The network provides an impedance transformation from 50 Ohm to the optimal load impedance of 14+j*10 Ohms at f_c=1.95 GHz, and also has a relatively high suppression of harmonics at the output.

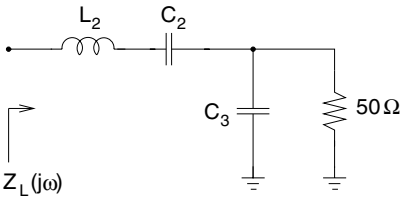

Fig. 4. Load network LN1.

Load Networks LN2 and LN3 are based on distibuted components, i.e. transmission lines, and are implemented by microstrip lines on the laminate substrate. LN2 is designed by the approach similar to that described in [7]. The open-circuit shunt stubs TL2 – TL5 have been sized such to correspond to λ/4 transmission lines at harmonic frequencies of $2f_c$ to $5f_c$, respectively. In this way, a low harmonic content will be obtained at the output of the PA, despite a harmonic-rich signal at the collector of the transistor. At the same time, the length and characteristic impedance of the series sections TL1 and TL6 are chosen such to provide the optimal load impedance at the fundamental frequency.

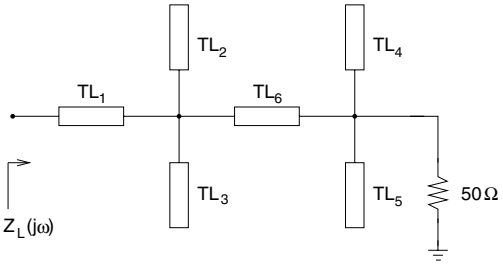

Fig. 5. Load network LN2.

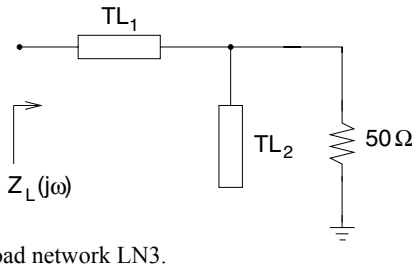

Fig. 6. Load network LN3.

LN3 is also based on distributed components, but provides a significantly simpler topology and occupies less space than LN2, while the PA performance is almost identical in terms of the output power and efficiency, with somewhat higher level of harmonics at the output.

III Technology and Implementation

For the active device an InGaP/GaAs Heterojunction Bipolar Transistor has been designed. The transistor is fabricated in a commercial GaAs HBT process (f_T=30 GHz) for power amplifiers. The process has 3 metal layers and supports back-side vias. In Fig. 7, a photo of the chip is shown. The HBT device consists of four basic transistor cells in parallel, with the total emitter area of 1620 μm^2. The transistor size is based on the estimation of the peak collector current (for the given supply voltage and output power level) and the maximum allowable current density of the process.

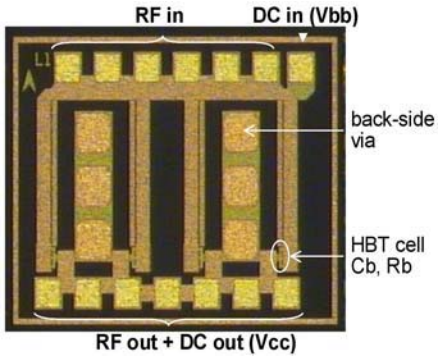

Fig. 7. Photo of the GaAs die.

Each basic cell has three emitter fingers of 45 μm length each. The transistor cells are placed along one side of the die, in the vicinity of the collector bondpads, in order to decrease the parasitic inductance of the metal tracks between the internal collector of the device and the external collector contact. There are six backside vias providing low-inductance ground connection to backside metalisation of the die. It is of major importance to minimize the emitter lead inductance (L_e, see Fig. 1), hence multiple vias have been used. The die has been attached by a conductive epoxy glue to the metallized die seat on the laminate substrate. This glue also provides a good thermal conductivity. The chip is connected to the rest of the circuitry by 30 μm thick gold bondwires. In order to decrease the series inductance, multiple bondwires have been used. The thickness of the laminate substrate is 460 μm. A photo of the entire PA circuit (version with load network LN1) is shown in Fig. 8.

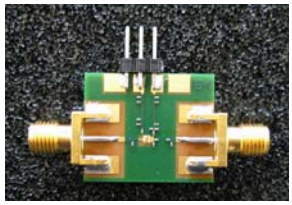

Fig. 8. The implemented Class-E PA circuit.

IV. Measurement Results

In this section, we will present the measured performance of the Class-E PA based on load network LN2. The measurements are performed at f_c=1.95 GHz and with the drive level fixed at 8 dBm (6.31 mW). Since Class-E is a switching type PA, the output power can be controlled by changing the supply voltage rather than by changing the input power. The measured P_{OUT} vs. V_{CC} characteristic is shown in Fig. 9. Due to the effect of the "knee" voltage (V_{CEsat}≈0.35 V), the output power is proportional to $(V_{CC}-V_{CEsat})^2$. The non-zero knee voltage of the device is at the same time one of the main sources of loss. Theoretically, the output (collector) efficiency is limited to $\eta=(V_{CC}-V_{CEsat})/V_{CC}$, but other losses in the circuit exist too. The measured output efficiency and power added efficiency are shown in Fig. 9.

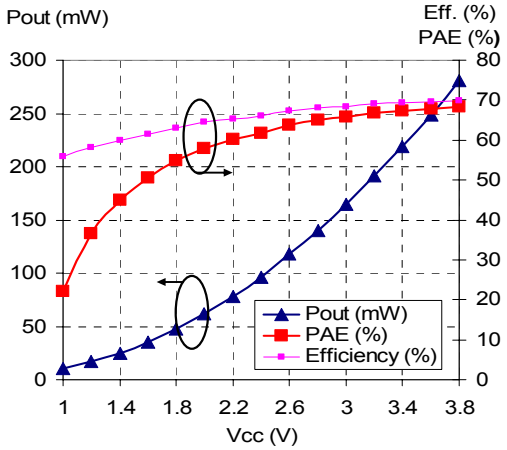

Fig. 9. The measured output power and efficiency performance of the Class-E PA (CW operation).

These two efficiencies are defined as $\eta=P_{OUT}/P_{DC}$ and $PAE=(P_{OUT}-P_{avs})/P_{DC}$, where P_{OUT}, P_{avs} and P_{DC} represent the output power, available source power and DC consumption power, respectively. The measured peak values are PAE=68.5 % and P_{OUT}=281 mW at V_{CC}=3.8 V. The decrease in the PAE in Fig. 9 for lower values of V_{CC} is primarily due to the drop in gain. When V_{CC} is decreased, P_{OUT} is also decreasing (approximately by the square low), but since the drive power P_{avs} is kept constant, the PAE rapidly drops. However, it remains above 50 % for the huge range of output power of almost 10 dB. In our opinion, this is an exceptional performance.

Being a switching type PA, the Class-E is inherently incapable of amplifying amplitude modulated (i.e. variable envelope) signals. However, it can be used with constant envelope modulation formats, e.g. GMSK, GFSK or analog FM signals. In Fig. 10, the spectrum of the amplified GMSK signal is displayed. The GMSK signal with a symbol rate of 270 kHz and BT=0.3 is generated by

WinIQSIM software in conjunction with AMIQ vector modulator and SMIQ vector signal generator, and then amplified by the Class-E PA. We have not noticed any significant spectrum regrowth in comparison with the input signal to the PA.

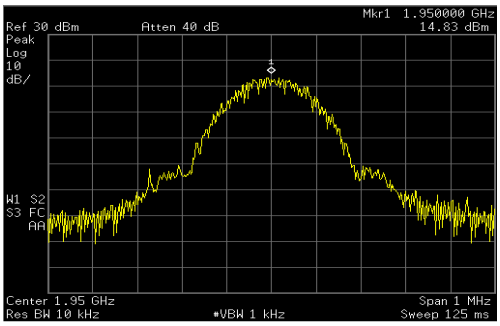

Fig. 10. Amplification of the GMSK signal.

The presented PA is essentially a narrowband, tuned circuit, but we have measured the output power and efficiency over a bandwidth of at least 50 MHz. The variations of the output power and efficiency with frequency are given in Fig. 11, for drive power fixed at 8 dBm and V_{CC}=3.8 V. The highest harmonic in the output signal is second and it has always been lower than -35 dBc. The designs based on load networks LN1 and LN3 achieved a very similar performance, with only a few percents lower efficiency.

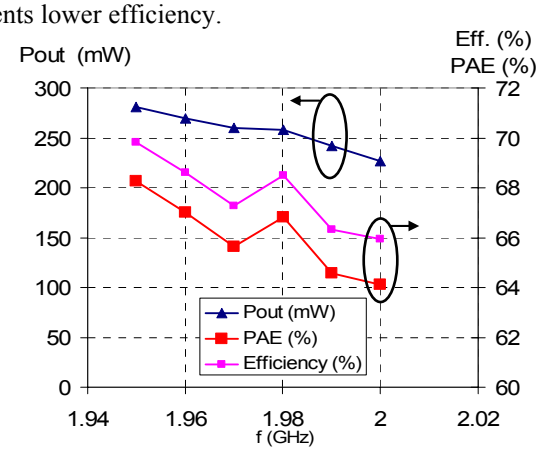

Fig. 11. Output power and efficiency as a function of frequency.

In Table I, we review the achieved performance in comparison with the relevant work of other authors. In the literature, surprisingly few Class-E PAs based on HBT technology and for 2 GHz frequency can be found. Therefore, we will also look at some of the designs implemented in other technologies and for other frequency bands. In [2], a PAE of 74 % is reported, but at more than a factor of two lower frequency and with a 3 dB lower gain. The work in [3] represents a two-stage amplifier, with the driver stage operating in Class-F. The reported gain is remarkably high, but with significantly lower PAE and also at a much lower frequency. Designs in [4] and [5] are differential CMOS Class-E PAs employing the mode-locking technique. The reported gain and output power are high, but either at lower frequency [4] or with low PAE [5]. Finally, the work in [6] achieves high output power and an outstanding PAE at 5 GHz, but the reported gain is poor.

Ref. #	Class	Technol. and device	f_c (GHz)	P_{OUT} (dBm)	Gain (dB)	PAE (%)
This work	E	GaAs HBT	1.95	24	16	68
2	E	GaAs HBT	0.8	21.3	13	74
3	F+E	GaAs MESFET	0.835	24	20	52
4	E diff.	0.35 um CMOS	0.7	30	18	62
5	E diff.	0.35 um CMOS	1.9	30	20	48
6	E	GaAs MESFET	5	28	9.8	72

TABLE I
PA PERFORMANCE BENCHMARK

V. CONCLUSION

A Class-E power amplifier based on a GaAs HBT is designed and implemented. A peak PAE of 68 % and a power gain higher than 16 dB are achieved, which represents the state-of-the-art performance for a single-ended single-stage GaAs HBT Class-E PA at 2 GHz. The PAE remains above 50 % over the range of output power of almost 10 dB, which is an exceptional performance, in our view. The PA is designed by combining the well-known Class-E theory and an experimental approach based on the load-pull principle. Both lumped- and distributed-component concepts have been demonstrated. The PA is capable of amplifying constant envelope RF signals, which has been successfully demonstrated with GMSK signal.

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