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GaAs MMICs for cost-effective insertion in digital radio link transceivers.

M.Pagani, M. Remonti, S. Velati and A. Panzeri

ALCATEL TELECOM - RSD ITALIA
Via provinciale per Monza, 33 - 20049 Concorezzo (MI) - ITALY.

Abstract

This paper describes the design and realization of three different GaAs monolithic gain blocks developed with the specific aim of representing a cost-effective solution for manufacturing modular power amplifiers in radio link applications. Various techniques and methodologies have been addressed to reach this goal and they are herewith presented. The proposed solutions to several problems regarding technology, device characterization, modeling and circuit design are discussed.

Introduction

The introduction of the Synchronous Digital Hierarchy (SDH) technology in transmission networks has represented a new interesting challenge for microwave digital radio systems to allow a successful integration into modern synchronous networks. Although fiber optics has increasingly become the preferred medium for long-haul high capacity transmission systems, SDH microwave radio is still strongly required by networks planners due to its intrinsic benefits in terms of security, speed of deployment and economics. To maximize the effect of these benefits, the radio systems must be able to complement a synchronous fiber network. High capacity SDH radio based on increasingly complex QAM modulation methods has been developed, realizing the growing spectral efficiencies needed for existing channeling plan preservation. Besides, the advantages deriving from the adoption of an Automatic Transmitted Power Control (ATPC) scheme, that allows the maximum transmitted power to be reached only during unfavourable fading conditions, has been greatly exploited in digital radio systems, due also to its intrinsic improvement in terms of outage performance and interference control.

As a consequence of the above facts, more sophisticated radio equipment design, requiring very highly linear operation within a high dynamic range, has been undertaken by some of the telecommunication system manufacturing companies. On the other hand, because of de-regulation, markets are globalizing and the number of aggressive competitors is constantly increasing even in the radiocommunication arena, so that to survive and grow in such environment, manufacturing costs must be continously reduced. To this aim, a new family of modular MMIC-based power amplifiers for digital radio link transceivers has been developed and produced in our company.

This work gives an overview of the most important issues related to the MMIC development procedure documenting our efforts for assessing a reliable approach to their cost-effective insertion in hi-tech equipments. After a brief description of the main technology aspects, the basic development background is described and analyzed with particular reference to three different MMIC, one wideband high dynamic Variable Gain Amplifier (VGA) and two highly linear power amplifiers, that are currently produced in volume and successfully integrated in cost-effective SDH radio equipments.

Technology aspects and basic development background

When the primary driver for a design is cost-effectiveness then device technologies that make use of straight forward, low cost processing and low cost materials have a clear competitive advantage over higher cost technologies. To achieve low cost fabrication a 3" wafer ion-implantation technology was chosen .

As well known, the capability of efficiently producing low cost high performance power MMIC is strongly related to the development of a reliable, simple and well controlled (i.e. mature) high yield manufacturing process. Further on, for high power digital radio transmitters applications, FETs with a high drain-source break-down voltage, reduced on-resistance and high linearity are essential.

As reported in [1] and [2], the wide and systematic theoretical and experimental work on material fabrication and wafer topside and backside

processing, has produced specific technology features allowing to increase the FET gate and drain break-down voltages and keep the gain as much as possible constant under increasing level of signal operation. To maximize the synergies and reduce the R&D investments almost the same foundry process has been adopted for GaAs discrete devices and power MMICs production. This process is based on 0.6 um gate lenght depletion-mode MeSFET technology using C-Si co-implanted structure for a better carrier confinement and suppression of substrate leakage current. It was demonstrated [3] to be particularly suited to obtain good performances in terms of power gain, output power, power efficiency and linearity, but the achievement of good MMIC characteristics, as needed for cost-effective insertion in digital radio systems, has involved the solution of specific problems other than those concerning technology such as optimum devices topology selection, measurements and modeling. The horizontal topology of the interdigitated FET was optimized as a trade-off between increasing power handling capability and reducing gate line attenuation, transversal phase unbalancing, total source inductance and thermal resistance.

Device characterization and modeling

For a consistent reduction of project cycle time and, as a consequence, developing cost, some efficient characterization procedures and an accurate modeling strategy are essential. In particular, when dealing with MMIC power amplifiers, the load-pull experimental characterization together with a large-signal model are very powerful tools for an optimum amplifier design. A load-pull based load impedence analysis was performed for several FET operating conditions by means of "directly on-chip" measurements made with RF micro-probes and semi-automatic test set that sped up the procedure [4]. To reproduce the actual thermal, mechanical and electrical operating condition, the chip is thinned to 100 um, via-holes connected to the back side and mounted onto a heat-sinking carrier, using the same die attach materials and methods of the final MMIC packaging process. Several standard cells of different dimensions were designed and characterized so that scaling rules could be defined by interpolation.

The large-signal model was obtained from on-chip S-parameters, DC and load-pull measurements and enabled the accurate prediction of output power at any gain compression, at any frequency in the operating band (from 2 to 12 GHz) and for any load condition.

Yield-driven design centering

Statistical modeling and design centering techniques based on Monte Carlo methods have been appointed [5] to improve the circuit yield and make MMIC cost-effective system insertion affordable. A statistically meaningful data base including FET equivalent circuit, S-parameters, 3rd order intermodulation distortion (IM_3) and output power at 1 dB gain compression point (P_{1dB}) was developed through continous data gathering of routine in-process measurements of process control monitor (PCM) devices. As described in [6], by using a small set of mutually uncorrelated process dependent parameters and by making reference to a phisically based semi-empirical FET model a process tolerance analysis is made possible, accounting for the statistical foundry process variations that directly affect manufacturability success. For the yield-driven design centering, during multiple yield analysis, the data-base is randomly accessed retrieving different device data sets for each circuit performance evaluation trial. The nominal values of the circuit elements more affecting the design yield are adjusted after each yield analysis iteration to maximize the final yield estimate.

By applying this technique more robust designs resulted, being able of both relaxing process requirements and increasing producibility and cost-effectiveness.

MMICs design

Three of different MMIC amplifiers recently developed as specific products for cost effective insertion in digital radio link transceivers are presented. Due to the objectives of manufacturing modularity, component standardization, short testing time and reliability improvements requested for the Solid State Power Amplifier cost reduction, a unique MMIC design methodology was pointed out. Although these MMICs are intended for use as narrowband gain blocks, they perform as broadband devices being able of advantageously replace, in terms of costs, sizes, weight and reliability, several existing MIC hybrids in the 3.4÷8.5 GHz band. They are single-ended amplifier, with 100 um substrate thickness and via-holes ground connections, designed in class A operating mode for linearity. Their output matching networks were designed to simultaneously satisfy requirements of P_{1dB}, linear gain and IM_3 in the whole operating band. To minimize assembly, wiring and tuning work, complete matching networks and bias circuitry were on chip.

Variable Gain Amplifier (VGA)

A wideband high dynamic VGA was designed to fulfil the ATPC request of the transmitter power amplifier design, with more than 25 dB of gain control over the 3.4÷8.5 GHz frequency band. The nominal gain is 17 dB, while the P_{1dB} is greater than 20 dBm. Zero-biased FETs are utilized as voltage controlled variable resistors in a double T configuration attenuator followed by a three self-biased stage amplifier. Very careful design of the interstage matching networks is required to insure that the driver stages do not make worse the intermodulation distortion figure of the output stage, in a so wide passband. The first stage uses lossy matching network for a good input VSWR over the whole band, while in the second stage there is a feedback for a better gain flatness. The current consumption is typically 140 mA. The chip size is 2.8 by 1.8 mm and the fabricated amplifier is shown in figure 1.

1 W power amplifier

This power amplifier is made with 3 stages and provides typically more than 25 dB gain with 1dB gain flatness in 3.4÷5.0 GHz frequency band. The input stage presents an all-pass matching network that ensures a good broadband input VSWR. The output stage consists of two 1.5 mm gate width FETs and the P_{1dB} is greater than 30 dBm (1 W) under CW condition. We designed a compact structure for this three stage amplifier to reduce its production cost. The final chip is shown in fig. 2 , its size is 3.65x1.7 mm, while its total current consumption is 500 mA, at 8 V of drain voltage.

2 W power amplifier

A very compact and higly linear amplifier covering a 42% frequency band , from 5.6 to 8.5 GHz, was designed with more than 12 dB gain, a typical P1dB of 33.5 dBm (2.3 W) and a third order intercept point of 43 dBm. The chip size is only 3.7 by 2.5 mm and the fabricated amplifier is shown in fig. 3. Typical gain curves from 6 chips of 3 different production wafers are reported in fig. 4. Four 1.8 mm wide FETs opportunely paralleled are used for the output stage, keeping a distance of 250 um from one to the other. A particular care was posed to the thermal aspect and loss of the output matching network, being the more critical task of this design. A map of the termal distribution of the MMIC mounted in a suitable package is reported in fig. 5. With the package temperature of 70 ^{o}C, the maximum FET channel temperature is 144.7 ^{o}C, at an enough low value for the reliability aspect. The bias conditions and the gate widths of the FETs are also optimized for a given output power and intermodulation distortion objective over the overall operating temperature range. More then a thousand of these power amplifiers have just been fabricated with good yield results.

Conclusion

The design and realization of three different GaAs monolithic gain blocks developed with the specific aim of representing a cost-effective solution for radio link applications has been presented. Various techniques and methodologies have been addressed to reach this goal. The proposed solutions to several problems regarding technology, device characterization, modeling and circuit design have been also discussed.

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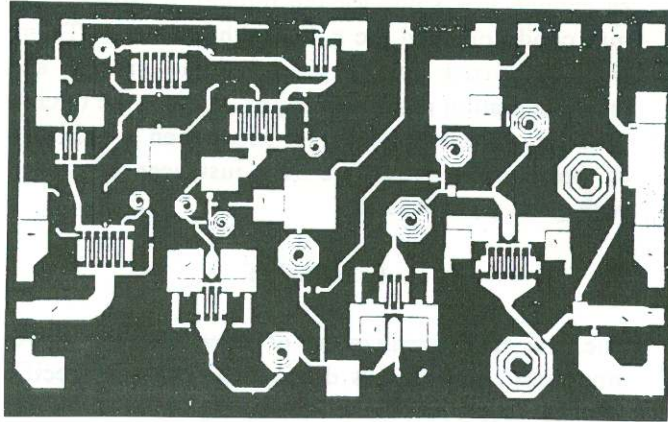

Fig. 1 - TVG39, Variable Gain MMIC amplifier.

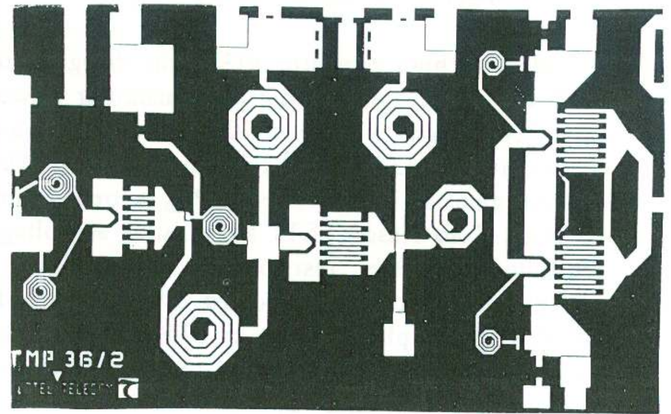

Fig. 2 - TMP36, 1W power MMIC amplifier

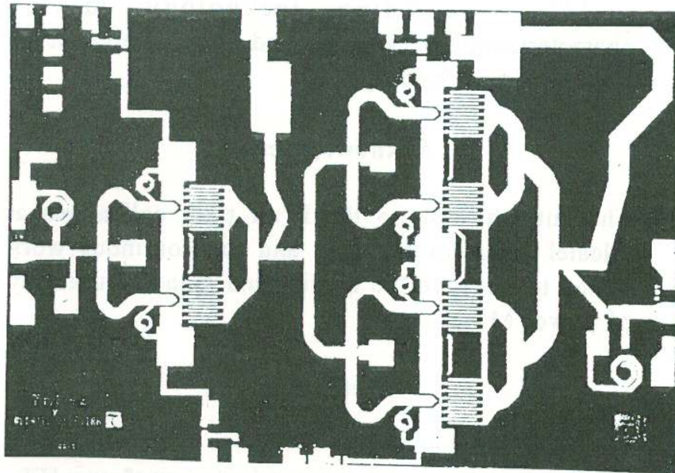

Fig. 3 - THP48, 2 W power MMIC amplifier

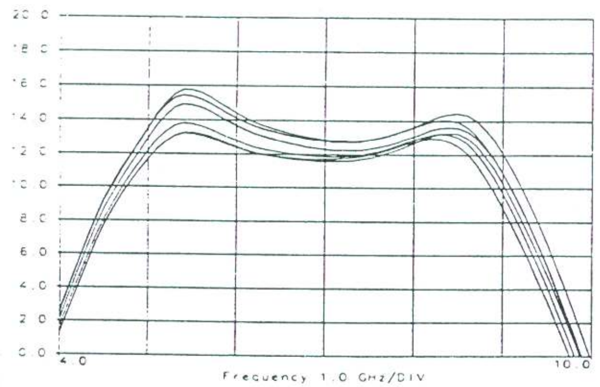

Fig. 4 - Gain curves for 6 different chips from 3 production wafers.

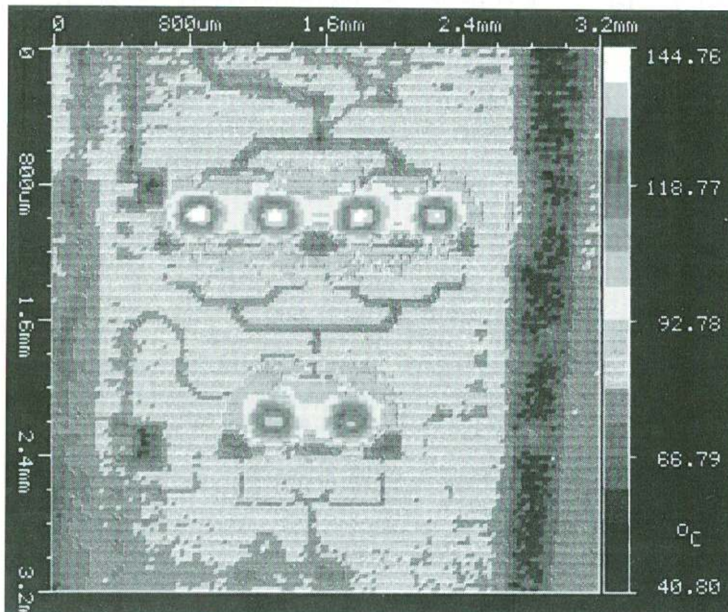

Fig. 5 - Thermography of the THP48 mounted in a package (Chuck temperature 70 ° C) .