A Wideband Fully Integrated SiGe BiCMOS Medium Power Amplifier

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***Abstract* — In this paper, a wideband 3.0GHz–5.5GHz Medium Power Amplifier has been designed and fabricated using 0.8um SiGe BiCMOS process technology. Passive elements such as parallel-branch spiral inductor, metal-insulator-metal (MIM) capacitor and three types of resistors are all integrated in this process. This Medium PA is a two stage design with all matching components and bias circuits integrated on-chip. A P1dB of 16.5dBm has been measured with a power gain of 8.5dB at 4.2GHz with a total current consumption of 130mA from a 2.5 V supply voltage at 25℃. The measured 3dB bandwidth is 2.5 GHz, which is a very good result for a fully integrated Medium PA. The fabricated circuit occupies a die area of 1.7mm × 0.8mm.**

I. Introduction

To meet the growing demand for multi-gigabit data communication systems and wide bandwidth radio communication systems, devices achieving both high speed digital operation with sophisticated functions and high frequency analog operation are the key components for ICs LSIs constructing such systems. SiGe hetero-junction bipolar transistor (HBT) and HBTs with CMOS transistors (BiCMOS) technologies play an important role in optical transmission and wireless communication systems [1]. SiGe BiCMOS devices are used in such a wide range of applications because they are superior to conventional homojunction silicon bipolar devices in every important performance metric. In fact, SiGe with bandgap engineering enables process designers to satisfy product requirements for simultaneous high cutoff frequency (f_T), maximum oscillation frequency (f_{max}), current gain, power consumption, Early voltage (V_A), and breakdown voltage (BV_{CEO}) [2]-[3]. These advantages are originated from two factors; one is the smaller band gap of SiGe than that of Si, and the other is the epitaxial growth of SiGe layers that realizes the base of high doping concentration and small width.

Recently, SiGe HBT power amplifiers have been demonstrated for 802.11b applications at 2.4 GHz and are emerging as a contender for RF power amplifier applications at higher frequencies [4].

In this paper, a wideband 3.0GHz–5.5GHz Medium Power Amplifier has been designed and fabricated on-chip, using the ETRI SiGe BiCMOS process. All matching components and bias circuits were integrated on the chip, requiring no external tuning components.

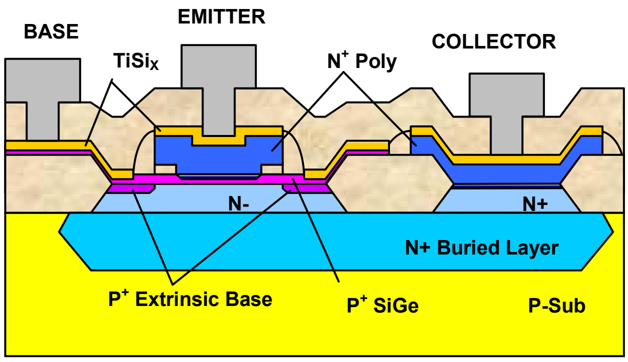

Fig. 1. Schematic of the SiGe HBT fabricated.

II. Characteristics Of SiGe HBT And Passive Devices

The technology used in this work is a 0.8um SiGe BiCMOS process with 2 metal layers and conventional local oxidation of silicon (LOCOS) process to define and isolate the active regions.

Figure 1 shows the cross-sectional view of the SiGe HBT fabricated. We have used the reduced pressure chemical vapor deposition (RPCVD) system to grow Si/SiGe/Si base layers and other Si epitaxial layers. In-situ heavily doped base layer is composed of the 35nm thick cap Si layer, the 35nm thick SiGe layer, and the 35nm thick seed Si layer. The Ge concentration is gradually increased from the cap layer to the seed layer, reaching to the maximum of 20 atomic percent. Boron (B) is in-situ doped in the SiGe layer, and its maximum concentration is 4×10^{19} atoms/cm^3. Heavily doped buried layers are fomed by As implantation, and the definition and the isolation of active regions are achieved by conventional LOCOS process. Self-aligned Ti silicide on Si/SiGe/Si base is formed in a rapid thermal annealing (RTA) chamber by the two step annealing composed of the first annealing and the second annealing [5]. The maximum f_T and f_{max} values of SiGe HBT with 0.5 × 6 um^2 emitter area are 41 GHz and 42 GHz, respectively.

In addition, passive elements used for MMIC amplifier are Metal-Insulator-Metal (MIM) capacitor, parallel-branch spiral inductor, resistors composed of metal, emitter poly-silicon, and base poly-silicon.

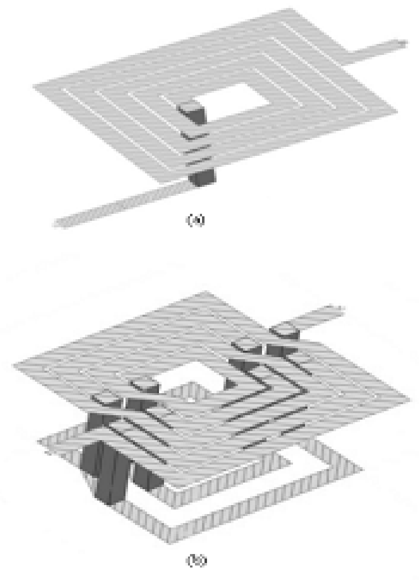

Fig. 2. Schematic diagram of the (a) conventional and (b) parallel-branch spiral inductor structure.

High-Q on-chip passive devices are required to meet the demanding requirements of RF circuits and to achive the " system-on-a-chip" integration levels that are possible with a SiGe BiCMOS process. The MIM capacitor consists of an underlying 1um Alumium metal layer, 75nm thickness of isolator SiO_xN_y, and 2um Al metal with TiN over/under. This capacitor has low resistance and parasitic capacitance of the metal plates. Therefore, this device is preferred in RF applications where high Qs and low parasitic capacitances are required.

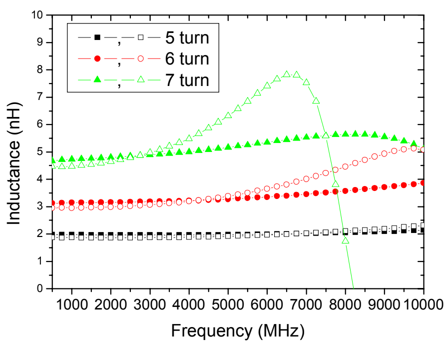

Fig. 3. Inductance variation of the conventional (solid) and the parallel branch (vacancy) inductors along the frequency.

Inductors integrated in this work used Q factor enhanced parallel-branch spiral inductors. Substrates used in SiGe BiCMOS processes have a medium substrate resistivity. Due to the interaction of the electric and magnetic fields of the spiral inductor with the substrate, parasitic substrate currents can be established in the substrate material. Parasitic currents occurred from the electric-field interaction with the substrate will cause power losses in the inductor, lowering Q [6]. Parasitic currents induced from the inductor's magnetic field will not only cause power losses but reduce the net inductance of the spiral due to a reduction in the net magnetic field.

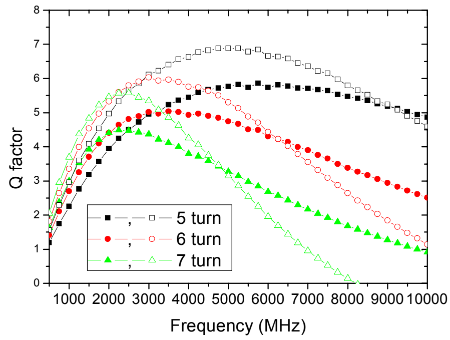

Fig. 4. Q factor variation of the conventional (solid) and the parallel branch (vacancy) inductors along the frequency.

Figure 2 shows the structures of the conventional spiral inductor and parallel-branch spiral inductor. The highest percentage improvement in inductor peak Q is achived by reducing the series-resistive losses of the spiral metal lines. To decrase the spiral-metallization sheet resistance, the second matallization has a 2um thickness, which is the optimum value in our condition. When the second metallization has over 2um, little improvement of Q was observed.

The inductor strip starts at the upper metal, branches off in the upper and lower metal strips with the same direction, and terminates at the opposite upper metal. Branching the inductor in parallel with the same direction, a mutual inductance is maximized and parasitic capacitances between lower metal and substrate are caused [7]. Therefore, the Q factor of parallel-branch inductor is enhanced. Also, it is possible the frequency of peak quality factor f_{QMAX} to be tuned, and the higher quality factor can be obtained. Figure 3 shows that the f_{QMAX} of the parallel-branch inductor is lower than the conventional due to the parasitic capacitances by the lower metal. In Fig. 4, the quality factor is higher because the self and mutual inductance of the lower metal is added and metal resistance R_S is decreased by the parallel branch of the two metal strips.

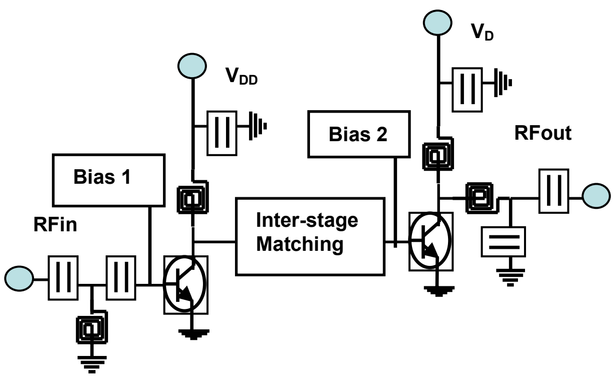

Fig. 5. Simplied Medium Power Amplifier schematic.

III . Medium Power Amplifier Design

The MMIC amplifier is a single-ended two stage design with all matching components integrated on-chip. The LOCOS process has merits of the economical process but, is suffering RF performance limitation. Hence, the emitter areas of the driver stage and output stage transistors are optimized to provide the power gain and output power.

The simplified schematic of the designed is shown in Fig. 5. The first stage amplifier is designed with effective emitter area of 108 um^2 transistor to improve the power gain. This first stage is matched to the input using a shunt inductance and the input DC-block capacitor and to the output using a inter-stage matching to the second amplifier. The second stage amplifier is matched to the output using two inductors and a capacitor. To improve the operating bandwidth of the amplifier, shunt-series peaked matching network has been used. Also, low pass output matching is adopted for diminishing the other harmonics, which helps the improvement of the amplifier linearity.

The bias currents are supplied using a resistor connected to the current-source to prevent thermal runaway in large signal operation.

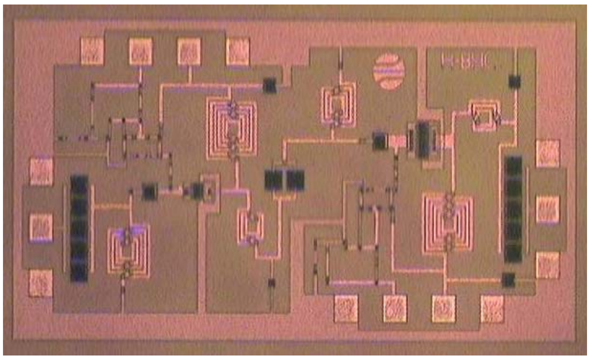

Fig. 6. Die photograph of the fully integrated medium Power Amplifier.

VI. Mesurements Results

The medium power amplifier occupies 1.7mm × 0.8mm of die size, including the bias and probing pads. This demonstrates the size advantage of full integration. Figure 6 shows the die photograph of the fully integrated medium power amplifier.

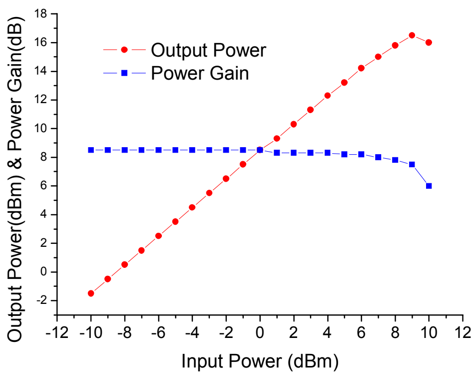

Fig. 7. Measured power gain and output power.

Figure 7 presents the single-tone compression characteristics and the power gain of the amplifier. From the data in this figure, we find that the 1 dB compressed output power of the amplifier is approximately 16.5 dBm into a 50 Ω load.

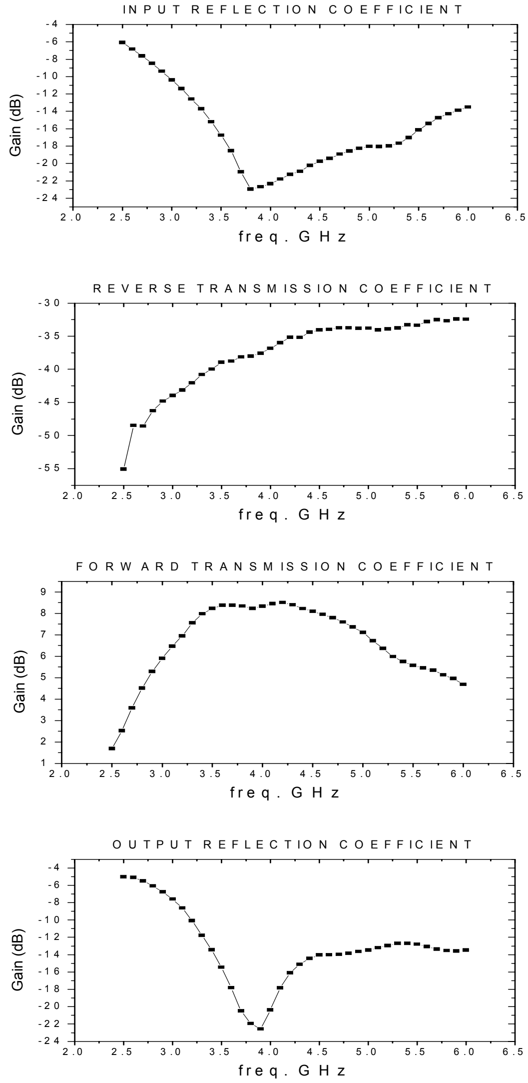

Fig. 8. Measured Small-Signal S-Parameters.

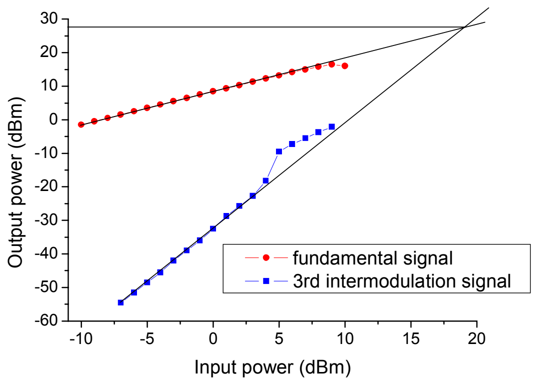

Fig. 9. Measured power intermodulation product.

Scattering Parameters of the amplifier in the 2.5 GHz - 6.0 GHz frequency range are shown in Fig. 8. From the data in Fig. 8, we find that the amplifier provides a small-signal power gain of 8.5 dB, an isolation of 35 dB, and the input and output return losses are better than 15 dB at 4.2GHz. The measured 3 dB bandwidth of the amplifier covers 3.0 GHz to 5.5 GHz. This wide bandwidth is a very good result for fully integrated medium power amplifier [8].

The two-tone compression characteristics of the medium power amplifier are shown in Fig. 9. Output IP3 of the amplifier has been measured driving the input of the MPA with 10MHz spaced two tones signals. From this figure, we find that an output IP3 of 27 dBm.

The fabricated medium power amplifier consumes a current of 130 mA for a 2.5 V supply voltage.

V. CONCLUSION

We have demonstrated a fully integrated medium power amplifier for 3.0-5.5 GHz in a 0.8um SiGe BiCMOS technology. This single-ended 2-stage amplifier has no need for external matching circuits and has a broad operation range with adopting shunt-series peaked matching network. The measured results obtained from the fabricated medium power amplifier show an 8.5dB power gain, a P1dB of 16.5dBm at 4.2GHz with a 2.5GHz bandwidth. This implies that a fully integrated medium power amplifier enables the realization of a single-chip transceiver for broadband wireless applications.

ACKNOWLEDGEMENT

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