

S and C band Over 100W GaN HEMT 1-chip High Power Amplifiers with Cell Division Configuration

Koji Yamanaka¹, Kazuhiro Iyomasa¹, Hiroshi Ohtsuka¹, Masatoshi Nakayama¹,
Yoshinori Tsuyama², Tetsuo Kunii³, Yoshitaka Kamo³, and Tadashi Takagi¹

¹Mitsubishi Electric Corporation, Information Technology R&D Center, Ofuna 5-1-1, 247-8501 Kamakura, Japan,
Phone : +81-467-41-2683

²Mitsubishi Electric Corporation, Communication Systems Center, Tsukaguchi-Honmachi 8-1-1, 661-8661
Amagasaki, Japan

³Mitsubishi Electric Corporation, High Frequency & Optical Device Works, Mizuhara 4-1, 664-8641 Itami, Japan

Abstract — In this paper, GaN HEMT 1-chip high power amplifiers at S and C bands are presented, which are featured by the cell division configuration. Spurious oscillations, which often occur for large gate periphery microwave transistors, were suppressed by dividing 8 transistor cells in a single chip into 4 blocks each consisting of 2 cells and placing isolation resistors on matching circuits. 120W and 140W output powers were successfully extracted from single chip GaN HEMT transistors with 3.8W/mm and 2.8W/mm power densities at S and C bands, respectively. These are top-level output powers from single chip GaN HEMT transistors over 3GHz.

To address problems of spurious oscillations, we employed the cell division configuration for over 100W output power GaN HEMT transistors. This configuration enabled us to effectively suppress spurious oscillations, which might have caused for the case of conventional style chips. As a result, S and C band GaN HEMT 1-chip power amplifiers managed to produce 120W and 140W output powers associated with 3.8W/mm and 2.8W/mm power densities respectively without any undesired oscillation. These are the state-of-the-art output powers from single chip GaN HEMT transistor over 3GHz to the best of our knowledge.

I. INTRODUCTION

Recently, GaN HEMTs have attracted much attention for next generation microwave power transistors due to their high voltage and high power density capabilities. Some over 100W output powers have already been reported around 2GHz band, which aim for cellular base-station amplifiers [1-4]. However, no over 100W output power has been reported over 3 GHz frequency regimes. One of the reasons is as follows. As the operation frequency become higher, dimensions of the chip widths become comparable to the wavelength and oscillation loops are formed nearby the chip. When these oscillation loops satisfy the oscillation conditions, spurious signals appear and prevent stable operations of the amplifiers. It should also be noted that GaN HEMTs are considered to tend to suffer from this kind of oscillations more likely than GaAs device for two reasons. One is that, for saturation velocity of electrons in GaN is faster than that in GaAs, GaN HEMTs can oscillate at higher frequencies. The other is that, due to high power density, GaN HEMTs may exhibit large temperature difference within a chip if good thermal treatments are not given. Therefore, thermally induced electrical unbalance between inner cells and outer cells can cause unbalanced -mode loop oscillations. To make the most of high power density capability of GaN HEMTs, development of circuit techniques for one chip high power amplifier is essential together with device technologies.

II. CONFIGURATION

A schematic of high power amplifier with the cell division configuration is shown in Fig.1. It consists of one multi-cell transistor chip (8 cells for this case) and matching circuits. Unlike a conventional multi-cell chip, whose cells share one large drain electrode pad, 8 transistor cells are divided into 4 blocks consisting of 2 cells. Number of transistor cells in a block was determined so as that the size of the loop formed in a block is as small as oscillation conditions are not met while maintaining manufacturability. To avoid another oscillation that comes from unbalance mode between blocks, so-called isolations resistors were placed on the matching circuits nearby the chip.

Circuit topology of the amplifier is schematically shown in Fig. 2. 2-stage quarter lambda impedance sections are employed for both input and output matchings. The first matching sections consist of parallel 4 transmission lines, each of which is connected to transistor cells with wires. The second matching sections divide (input side) or combine (output side) the high frequency signals. Two kinds of loop oscillations are possible for the case of the circuit of Fig. 2, i.e. larger loop A and smaller loop B. Among of two, suppression of oscillation at loop B is more important because loop B is inherently asymmetric both electro-magnetically and thermally, while loop A is symmetric.

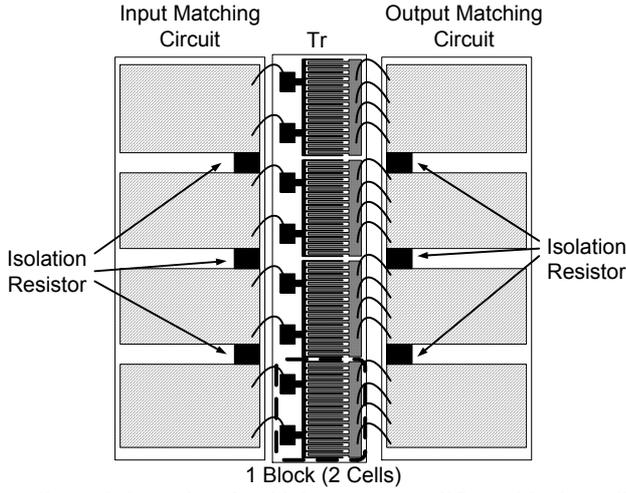


Fig. 1. Schematic of a high power amplifier with the cell division configuration. (near by the transistor chip)

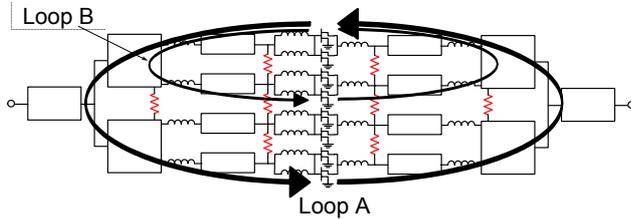
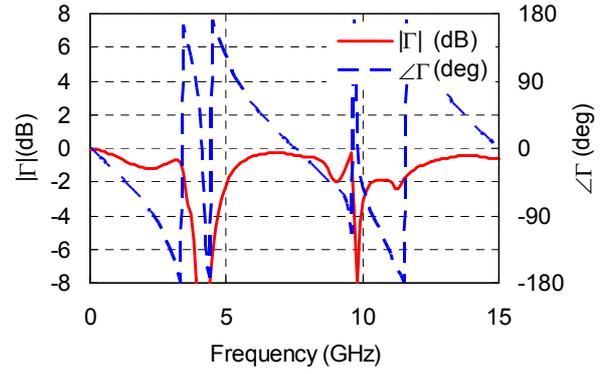


Fig. 2. Circuit topology of the amplifier.

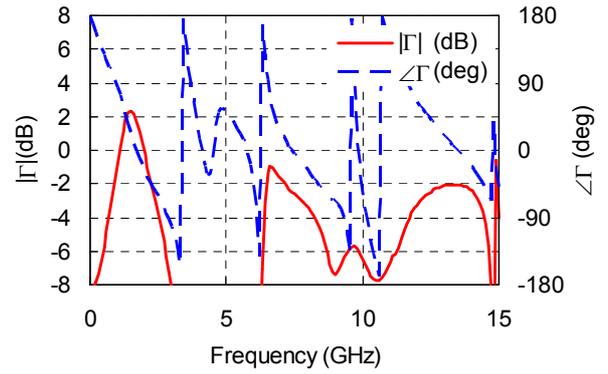
To investigate effectiveness of the cell division configuration, odd mode loop gain of loop B was calculated using small signal data of unit cell transistors using the isolator insertion method [5]. Fig. 3 shows odd mode loop gains and loop phases of loop B for the case of (a) conventional multi-cell transistor, (b) the cell division configuration without isolation resistors, and (c) the cell division configuration associated with isolation resistors, respectively. Conditions for possible loop oscillations are denoted by;

- (i) loop phase $\angle\Gamma = 0$
- (ii) loop gain $|\Gamma| > 1$ (0 dB)

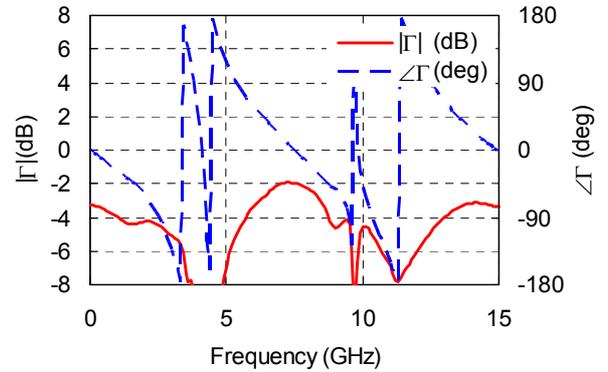
For the case of conventional multi-cell transistor (Fig. 3 (a)), there is no frequency regime which satisfies oscillation conditions. However, loop gain margin is only 0.4 dB at 7.5 GHz where loop phase condition is met. Such a small margin is insufficient to ensure stable operation at high output power domains because isolation of transistors is usually become worse at near saturated operations. For the case of the cell division configuration without isolation resistors (Fig. 3 (b)), loop oscillation conditions are met at 1.7 GHz hence spurious oscillations are expected even in the small signal conditions. On the contrary, for the case of the cell division configuration associated with isolation resistors (Fig. 3 (c)), maximum loop gain is less than -2 dB up to 15 GHz. It can be deduced that combination of the cell division configuration and isolation resistors effectively lowers odd mode loop gain of small loop B and suppresses spurious oscillations. Loop gain of large loop A was also calculated in the design procedure and loop stability has been assured, although not shown here.



(a) conventional multi-cell transistor



(b) cell division configuration without isolation resistors



(c) cell division configuration associated with isolation resistors

Fig. 3. Calculated odd mode loop gain and loop phase of small loop B for (a) conventional multi-cell transistor, (b) cell division configuration without isolation resistors, and (c) cell division configuration associated with isolation resistors.

III. EXPERIMENTAL

The cell division configuration has been implemented in S and C band GaN HEMT high power amplifiers which aim for over 100W output powers from a single chip. The photograph of the S band amplifier is shown in Fig. 2. Bias circuits are formed on separate substrates for simplicity of the circuit design. The configuration of the C band amplifier is almost same as S band one except that total gate width of the C band amplifier is 50.4mm while that of the S band one is 32mm. Cat-CVD SiN

passivation technique [6] is employed to suppress so-called current slump phenomenon and enables pulse mode operation. Details of the device technologies are described in [6].

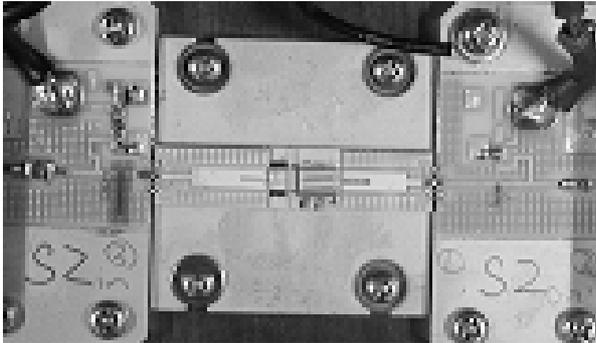


Fig. 4. Photograph of the S-band GaN HEMT high power amplifier

Output characteristics of the S and C band are shown in Fig.3 and Fig. 4 respectively. The measurements were done under pulsed bias conditions to avoid self-heating effect. The S band amplifier produced 50.8dBm (120W) output power with very high power density of 3.8W/mm at $V_d=50V$, while the C band amplifier produced remarkable total high power of 51.5dBm (140W) with power density of 2.8W/mm at $V_d=40V$. Thanks to the cell division configuration and isolation resistors, no spurious oscillation was observed over entire measurements.

In Fig. 7, typical GaN HEMT output powers reported so far are shown with respect to the operation frequency. Our results shows top-level output powers comparable to the newly reported data [7] that exceeds 150W output power from a single chip GaN HEMT amplifier over 3GHz.

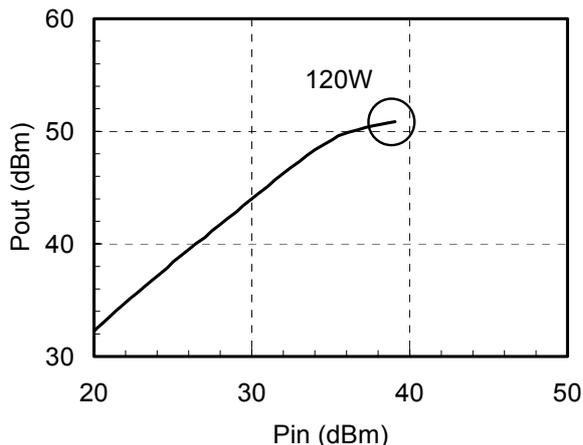


Fig. 5. Output characteristic of the S-band GaN HEMT high power amplifier

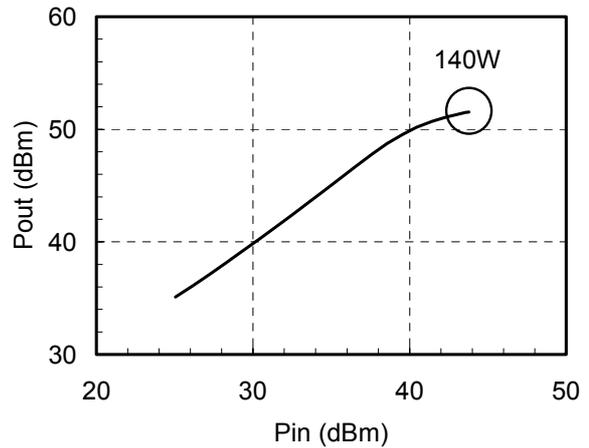


Fig. 6. Output characteristic of the C-band GaN HEMT high power amplifier.

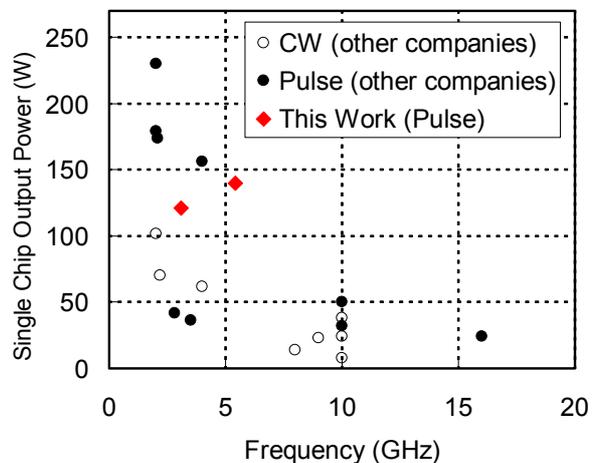


Fig. 7. State-of-the-arts of output powers from single-chip GaN HEMT transistors.

IV. CONCLUSION

In conclusion, we have developed S and C band GaN HEMT high power amplifiers with the cell division configuration. Over 100 W output powers were successfully obtained from both amplifiers without any spurious oscillation thanks to the cell division configuration.

We conceive that the cell division configuration will be one of the most effective techniques to extend the operation frequency of the large gate periphery GaN HEMT transistors beyond C band and promote widespread use of GaN HEMTs.

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