A Miniature DC-to-50 GHz CMOS SPDT Distributed Switch

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***Abstract* — A dc-to-50-GHz SPDT switch in standard bulk 0.18-µm CMOS process is demonstrated in this paper. In order to extend the operation frequency, the traveling-wave circuit topology is utilized. The switch achieves a measured insertion loss of less than 6 dB, a measured isolation of better than 38 dB from dc to 50 GHz. The measured input P_{1dB} of 17.4 dBm at 5.8 GHz and 19.6 dBm at 40 GHz is attained. The chip size is only 0.5 x 0.5 mm^2. To our knowledge, this work is the first CMOS switch operating from dc to millimeter-wave frequency with a miniature chip size.**

I. Introduction

In recent years, wireless communication systems have undergone explosive growth that is largely unanticipated. In time-division duplexing (TDD) communication systems, T/R switch plays an important role to change the RF signal flow to tramsmitter or receiver. To further increase the integration level, the SPDT switch has to be integrated in the transceiver. CMOS technology has been able to meet the more stringent cost constraints inherent in these more diverse mainstream applications. The advantages of silicon CMOS technology for RF and microwave control functions over GaAs are its low cost, and the integration potential with RF and silicon MOS-based mixed-signal circuitry.

Switches using CMOS processes were reported [1]-[4]. However, due to the limit of the CMOS process and circuit topology, the frequencies of most reported CMOS RF switches are lower than 5.8 GHz. The conventional topology for CMOS switch is series-shunt, which is only suitable for narrow band design. A different topology of narrow-band CMOS switch is reported [5]. It demonstrates the power performance of a CMOS switch, but the LC-tuned substrate bias network limits the frequency response. For broadband frequency response, a switch using 0.13-µm CMOS process based on traveling-wave concept is reported [6]. The switch combined the off-state shunt transistors and series microstrip lines to form an artificial transmission line with 50-Ω characteristic impedance and achieve wide bandwidth.

In this paper, a CMOS RF SPDT switches in standard bulk 0.18-µm CMOS process is presented. By using the traveling-wave concept, this chip demonstrated wideband frequency response. The CMOS SPDT switch exhibits lower than 6-dB measured insertion loss, with better than 38-dB isolation from dc to 50 GHz. It also accomplishes 17.4-dBm input P_{1dB} at 5.8 GHz and 19.6-dBm P_{1dB} at 40 GHz with a miniature chip size of 0.25 mm^2, including the testing pads. To our knowledge, this work demonstrates the first CMOS switch operating from dc to millimeter-wave frequency with a miniature chip size of 0.5 x 0.5 mm^2.

II. Switch Design

Figure 1 shows the circuit schematic of the conventional SPDT switch using traveling-wave concept. For a SPDT switch, the turn off path should not influence the turn on path. For the shunt distributed switches, quarter wave length transmission lines are usually applied to transform the low impedance of the turn off path to high impedance. The bandwidth is thus limited by the quarter wave length transmission lines. Instead of the quarter wave length transmission lines, a series transistor can be used for the wide bandwidth operation. However, because of the series parasitic resistor of the transistor, the insertion loss is often higher then that of the SPDT switch using quarter wave length transmission lines. The gate width of the series device can be selected to trade off between the insertion loss and the bandwidth [7].

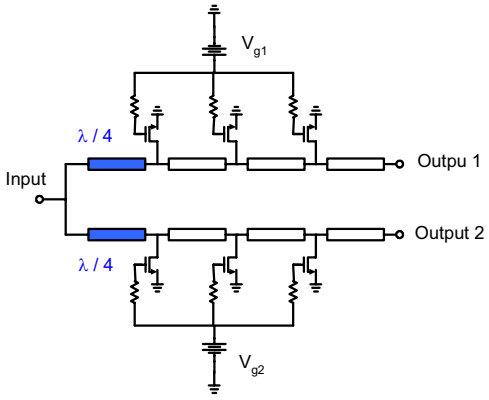

Fig. 1. Circuit schematic of conventional SPDT switch using traveling-wave concept.

In order to increase the power performance of the switch, a body floating technique and a voltage division technique of stacked transistor configuration are used [8], [9]. However, there is twice parasitic resistance of the two series transistors, which will increase the insertion loss. To solve this problem, two shunt transistors are added and the total four devices form a series/shunt cell. Figure 2(a) demonstrates the series cell of the switch, while Fig. 2(b) is the shunt cell. In the series/shunt cell, the parasitic resistance is the same as those of a single series/shunt transistor, but the power handling capability is improved.

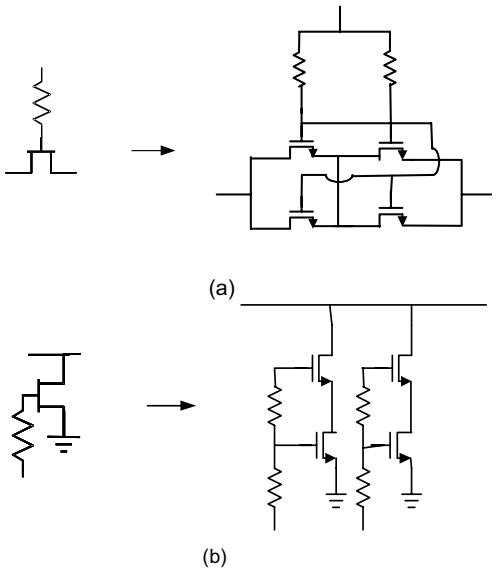

Fig. 2. The circuit schematics of the (a) series cell and (b) shunt cell, respectively.

III. Device Characteristics and MMIC Process

This CMOS SPDT switch is implemented by commercial standard 0.18-μm MS/RF CMOS technology which provides one poly layer for the gate of the MOS and six metal layers for inter-connection [10], [11]. The substrate conductivity is approximately 10 S/m. With optimized CMOS technology and deep n-well, this technology provides f_T and f_{MAX} of better than 60 GHz and 55 GHz, respectively. High-Q inductors can be formed using the top AlCu metallization layer of 2-μm thickness without additional masks. A MIM capacitor of 1 fF/μm^2 has been developed using oxide inter-metal dielectric. For the device of 40 μm gate width, the equivalent capacitance of the off state (C_{off}) is 0.05 pF, and the equivalent resistance of the on state (R_{on}) is 24 Ω.

IV. Circuit Design

Figure 3 shows the total circuit schematic of the SPDT switch. In order to improve the performances of the switch, it is important to select the device sizes of series cell and shunt cell. The relation between device sizes and simulated insertion loss at 50 GHz is shown in Fig. 4. For lower insertion loss, the gate width of 37.5 μm is selected for the shunt cell (w_1), while there are two options for series cell (w_2). One is 40 μm, and the other is 80 μm. Figure 5 presents the simulated performances of the switch in the two cases. To obtain better insertion loss and isolation simultaneously, the device size of the series cell is chosen to be 40 μm.

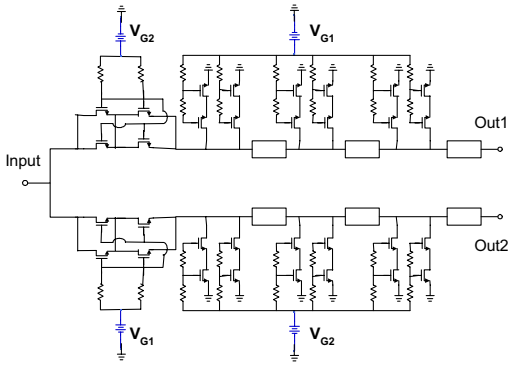

Fig. 3. The circuit schematic of the SPDT switch.

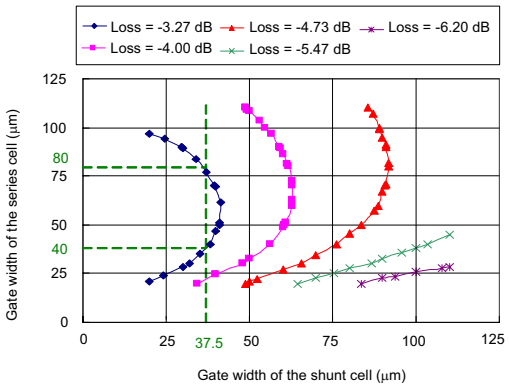

Fig. 4. The relation between simulated insertion loss and the sizes of the transistors.

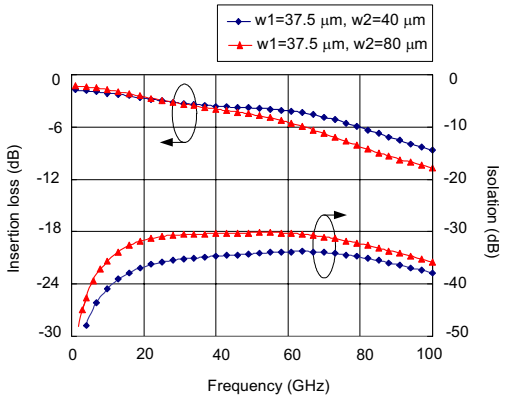

Fig. 5. The simulated insertion loss and isolation of the switch in two different cases.

V. MEASUREMENT

The die micrograph of the distributed SPDT switch using 0.18-µm CMOS process is shown in Fig. 6. The chip size is 0.5 x 0.5 mm^2 and the effective circuit area without pads is only 0.4 x 0.35 mm^2. The circuit was tested via on-wafer probing. Figure 7 shows the simulated and measured S-parameters of the switch which covers dc to 80 GHz operation frequency. The insertion loss is lower than 6 dB and the isolation is better than 38 dB from dc to 50 GHz. The P_{out} v.s. P_{in} at 5.8 GHz is shown in Fig. 8. It can be observed that the output P_{1dB} achieves 17.4 dBm at 5.8 GHz. Figure 9 presents the P_{out} v.s. P_{in} at 40 GHz. The input P_{1dB} of the switch is 19.6 dBm at 40 GHz.

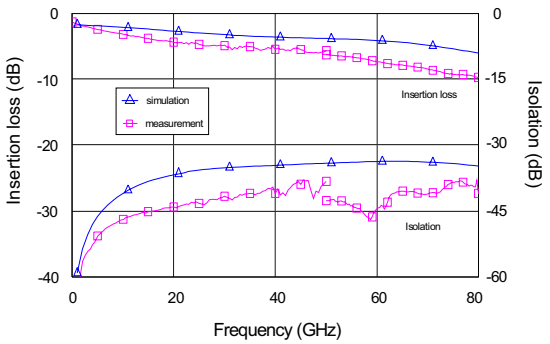

Fig. 6. Die micrograph of the SPDT switch. The chip size is only 0.5 x 0.5 mm^2.

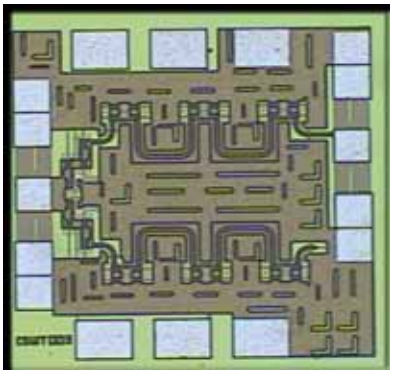

Fig. 7. The small measured signal insertion loss and isolation of the SPDT switch. The insertion loss is lower than 6 dB and the isolation is better than 38 dB in a dc to 50 GHz band.

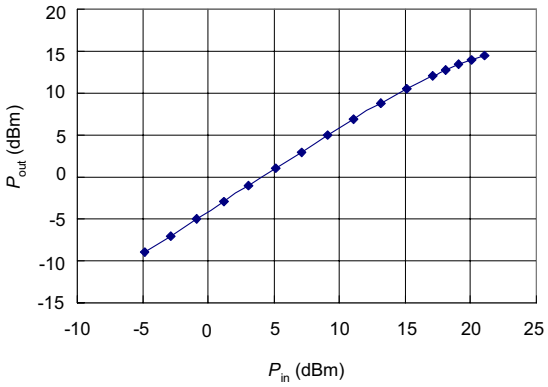

Fig. 8. The measured P_{out} v.s. P_{in} at 5.8 GHz.

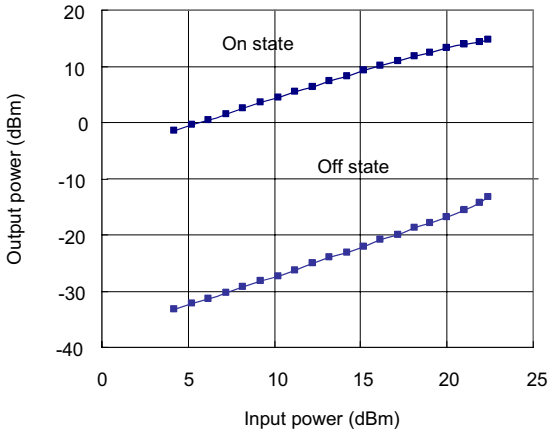

Fig. 9. The measured P_{out} v.s. P_{in} of the switch at 40 GHz.

VI. CONCLUSION

Using 0.18-µm CMOS technology, a SPDT switch has been designed, fabricated, and tested. Using traveling-wave technique, it accomplishes the wide frequency range with smallest chip size. The CMOS SPDT switch exhibits 6-dB measured insertion loss, 38-dB isolation from dc to 50 GHz. The measured P_{1dB} is 17.4 dBm at 5.8 GHz and 19.6 dBm at 40 GHz. Since the switch was fabricated using standard bulk 0.18-µm CMOS technology, it can be easily integrated with other front-end circuits to built CMOS transceivers without requiring any additional mask or post-processing steps. This is the first CMOS switch covering dc to millimeter-wave frequency with a miniature size of 0.5 x 0.5 mm^2.

ACKNOWLEDGEMENT

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