Compact and Broadband Microstrip Power Amplifier MMIC with 400-mW Output Power using 0.15-μm GaAs PHEMTs

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Abstract—**The performance of a compact power amplifier MMIC for 35 to 45 GHz applications is reported. Using a standard 6-inch, 0.15-μm GaAs power PHEMT technology on 100-μm substrate thickness, in combination with appropriate compact circuit topologies, this microstrip power amplifier achieved a linear gain of more than 24 dB over the 36 to 45 GHz frequency range. At 5 V and 500 mA bias, an output power at 1-dB compression of 26 dBm (P_{-1dB}=400 mW) was measured in the 37~40 GHz band, with a saturated output power up to 0.5 Watt (P_{sat}=27 dBm). The total chip size is only 3.6 mm^2 (2.4 × 1.5 mm^2); compared to conventional power amplifier MMICs operating at these frequencies, the combined output power and gain densities per chip area are a factor two higher.**

I. Introduction

Recent market growth in Local Multi-point Distribution Services (LMDS), Very Small Aperture Terminals (VSAT), and Microwave Video Distribution Systems (MVDS), has created a demand for cost effective power amplifier (PA) MMICs at millimeter-wave frequencies, especially in the Ku-, Ka- and Q-bands (e.g. [1-6]). For these power components, chip area is usually the bottleneck to drive the cost down [2-4]. Designers have to combine and match large gate peripheries at high frequencies, while keeping reasonable chip area, and meeting the reliable performance goals in terms of electrical properties (output power, gain, bandwidth, consumption, etc.) and thermal properties (lifetime).

Progress in fabrication processes have made shrinking the HPA MMIC size easier: higher power PHEMT device process [1,2], thin GaAs substrates (down to 50 μm), micro via-holes, and capacitors over vias [2-4]. Drawbacks still exist with such solutions: wafer robustness and handling, the need for advanced manufacturing techniques and equipment, technology reproducibility and yield (e.g. accuracy of the via-etching process for capacitors over vias, etc.), among others. All these issues directly affect the final cost of the PA MMIC die.

For these reasons, a standard commercially available 6-inch GaAs PHEMT technology, with 100-μm substrate was used for the design of the broadband 4-stage amplifier MMIC reported in this paper. The compact power amplifier MMIC was designed to address multiple applications from 35 to 45 GHz, with an emphasis on point-to-point radios in the 37~40 GHz frequency band. The high integration density was achieved thanks to compact matching network topologies, incorporating lumped elements, and with the extensive use of 2D and 3D electromagnetic (EM) simulations, to account for the strong coupling effects arising in such tight microstrip topologies on 100-μm substrate thickness. This resulted in the first-pass design performance reported here.

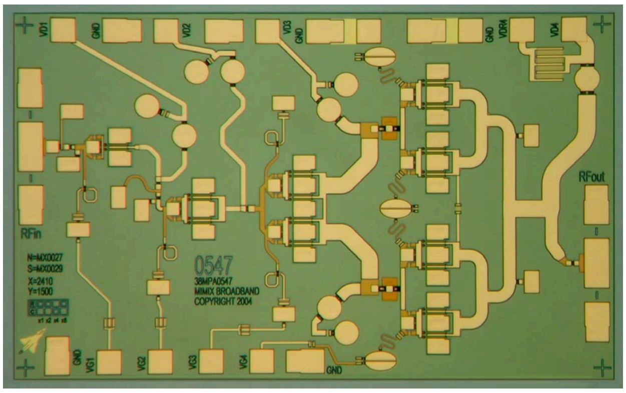

Fig. 1: Chip photograph of the 0.5-Watt Q-band Power Amplifier MMIC (chip size is 2.4 mm × 1.5 mm = 3.6 mm^2).

II. MMIC design

The MMIC fabrication is based on WIN's standard 0.15-μm 10-V power PHEMT process on 6-inch wafer with 100-μm substrate. The amplifier (Fig. 1) consists of four 4 × 75-μm devices driven by three successive stages having a gate width ratio of 2:1, for a total gate periphery of 2.25 mm. Individual source-via PHEMTs were used for their excellent electrical and thermal properties. The total chip size is only 3.6 mm^2 (2.4 mm × 1.5 mm). Such a chip area is remarkable for 100-μm GaAs ICs at these frequencies, since comparable conventional microstrip designs exhibit approximately twice this amount of area (e.g. [5-8]). Based on the optimum power transfer and dynamic load cycle approaches, rigorous design and layout methods were considered in the optimization of power, gain and bandwidth [3,4]. For flexible impedance matching and size reduction, parts of the matching networks were realized using semi-lumped elements like capacitors or small inductors fully simulated with Sonnet

3D-planar EM software. The normalized determinant factor (NDF) stability analysis [9], in combination with large on-chip bypassing capacitors and resistive loading, was used to prevent low frequency-, parametric- and odd-mode oscillations, resulting in unconditional stability of the amplifier up to and above the device maximum frequency f_{max}.

III. Measured Performance and Discussion

The MMIC amplifiers were tested on-wafer, in *continuous wave mode* (CW) for both small signal S-parameters, and power sweep. Fig. 2 shows the measured small signal gain, input and output return loss of the amplifier at nominal bias conditions of $V_{ds} = 5$ V and $I_d = 500$ mA ($V_{gs} = -0.8$ V). From 36 to 45 GHz, the linear gain averages 24 dB with a nice flatness, and relative good *on-wafer* input and output match: S_{11} is below -8 dB (typically –10 dB) and $S_{22} < -12$ dB. Excellent RF uniformity was observed as shown with 35 samples distributed across a 6'' wafer.

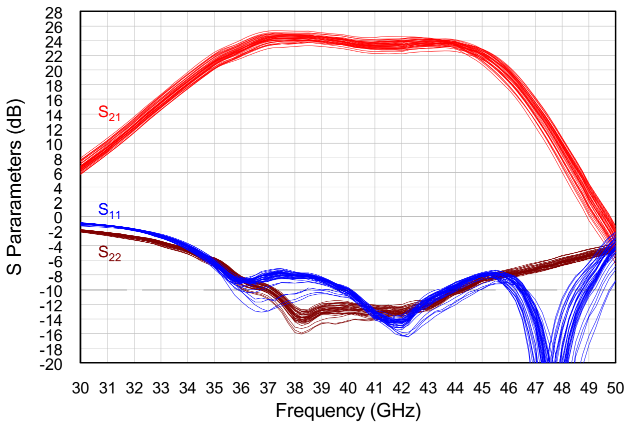

Fig. 2: On-wafer measured small signal gain, input- and output return loss versus frequency of the 36-45 GHz power amplifier at $V_{ds} = 5.0$ V, and constant $V_{gs} = -0.8$ V (I_d~500 mA, 35 samples).

Fig. 3 shows the measured CW output power versus frequency at an input power P_{in} varying from -10 to +5 dBm. At V_{ds}=5 V and for a total supply current of 500 mA, the output power is above 25 dBm at 1-dB gain compression from 35 to 43 GHz, and averages 26 dBm (400 mW) in saturation. Fig. 4 shows the typical gain and CW output power characteristics versus input power, measured in the 37 to 40 GHz radio range. In this band, P_{-1dB} is 26 dBm and $P_{sat} > 26.5$ dBm (27 dBm peak at 39 GHz). It should be noted that some of the power roll-off above 40 GHz is attributable to mismatch loss of the 200-µm RF pads during scalar power measurements. At wafer level characterization, the circuit is not compensated as designed: the 200-µm pad exists to compensate for bond wire parasitic inductance. Output power near saturation can be increased at 5.5 and 6 volts drain-bias by an amount of approximately 0.5 dB without significantly degrading amplifier lifetime. Fig. 5 illustrates the variations of the DC drain and gate currents for the four stages of the PA MMIC, as a function of the input drive: the currents are well behaved and all gate currents carry less than 1 mA/mm.

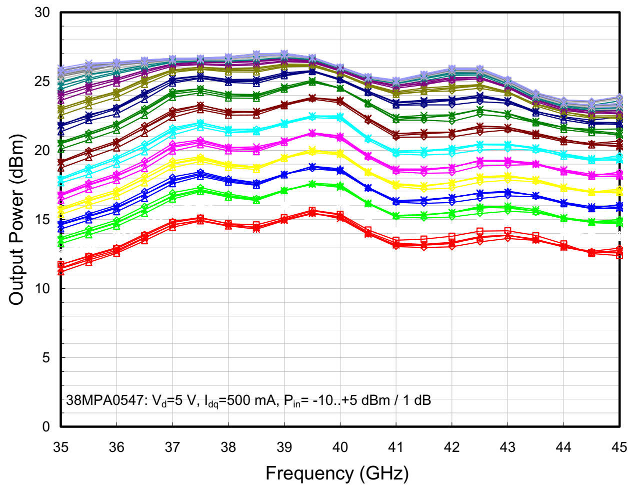

Fig. 3: On-wafer measured CW output power versus frequency at P_{in} = -10..+5 dBm, V_{ds} =5.0 V, I_d = 500 mA (5 cells).

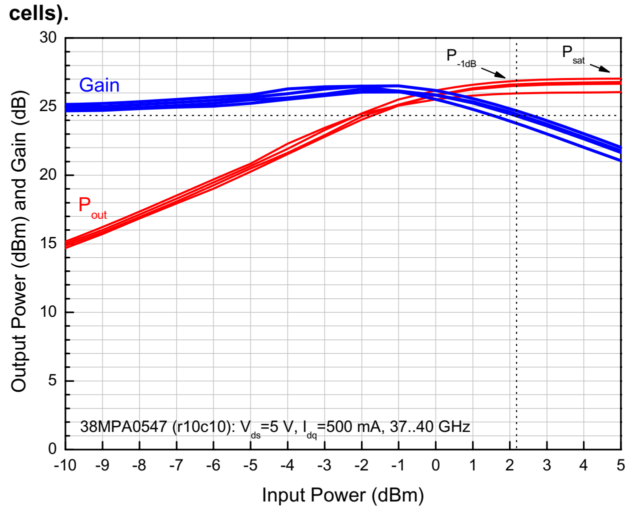

Fig. 4: Typical on-wafer measured CW output power and gain versus P_{in} at 37-40 GHz, V_{ds} = 5.0 V, I_{dq} = 500 mA.

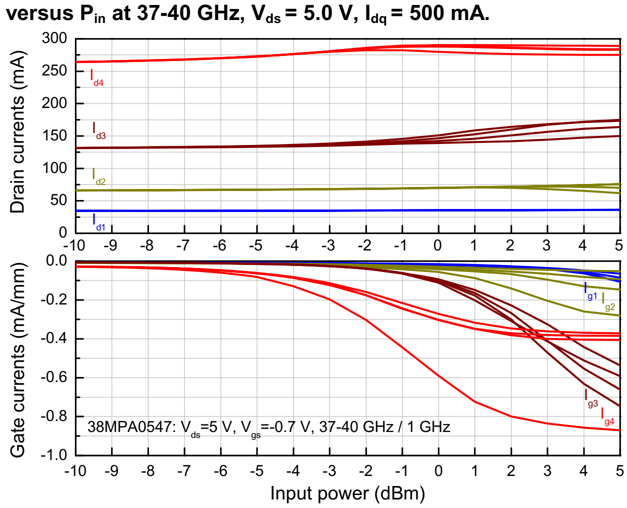

Fig. 5: Typical measured drain and gate currents versus P_{in} at V_{ds} = 5 V, V_{gs} = -0.7 V in the 37-40 GHz frequency band.

The PA MMIC can be used in highly linear applications as well with very good intermodulation characteristics. Fig. 6 shows the carrier to third order intermodulation level ratio as a function of the output power per tone. At $V_d = 4.5$ V, and $I_d = 500$ mA, the MMIC exhibits more than 55 dB C/I_3 at low output power levels, with very good output third order intercept point OIP_3, in excess of +35 dBm over the 37~40 GHz band. The C/I_3 and OIP_3 are also reasonably good at higher output power level, even close to saturation.

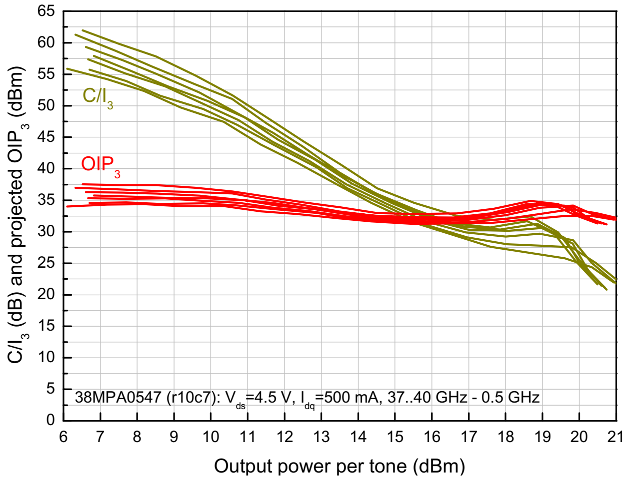

Fig. 6: Measured third intermodulation to carrier ratio (C/I$_3$) and projected OIP$_3$ as a function of output power per tone at V$_d$ = 4.5 V, I$_d$ = 500 mA in the 37 to 40 GHz band.

For use in saturated PDH (Plesiochronous Digital Hierarchy) radio systems at 38 GHz, with the maximum efficiency and the least number of external MMICs required for the chipset solution [10,11], the circuit has been designed with a unique ability to control the output power with the bias. In this way, the overall RF system output power can be controlled through the RF PA part only, without the need of external variable gain amplifier or IF gain control. This high performance design strategy places stringent requirements on the PA MMICs:

- the output power of the power amplifier PA has to be controlled through the bias supply only, with an high dynamic range in saturation
- the PA must sustain full performance in terms of output power (adjustable gain) and linearity over specified input power levels and temperature ranges
- when the PA is turned down, it must maintain acceptable IIP$_3$ with monotonic power decrease versus bias
- the PA MMIC must be stable under any I_{ds}/V_{ds} bias condition
- device lifetime requirements must be maintained under any bias condition

All these requirements have been addressed during design, especially stability and gate currents under arbitrary bias. Fig. 7 shows the variation of output power at 40 GHz as a function of the gate and drain bias, when the amplifier MMIC is driven at an input power of +5 dBm (saturation). As illustrated, the output power can be controlled (and turned off continuously) either by reducing the drain-source voltage or bringing the PA MMIC close to pinch-off (V_{gs}≈-1.4 V). Data here has been taken using combined gate and drain control (all gates and drain changed together respectively) to lower the device's output power. Although there are many possible bias paths to reduce the RF output power, some turn-down sequences are preferable: 1) From the nominal bias point (full performance at V_{ds}=5 V, I_{ds}=500 mA), the power can be turned down to -20 dBm by simultaneously bringing the gates and drains down to -1.4 V, and 0 V respectively. 2) The output power can be controlled through the drain bias only, at a constant gate voltage (e.g. V_{gs} ~ -0.75 V for high gain), and reduced down to -25 dBm, achieving more than 50-dB dynamic control, as shown in Fig. 8.

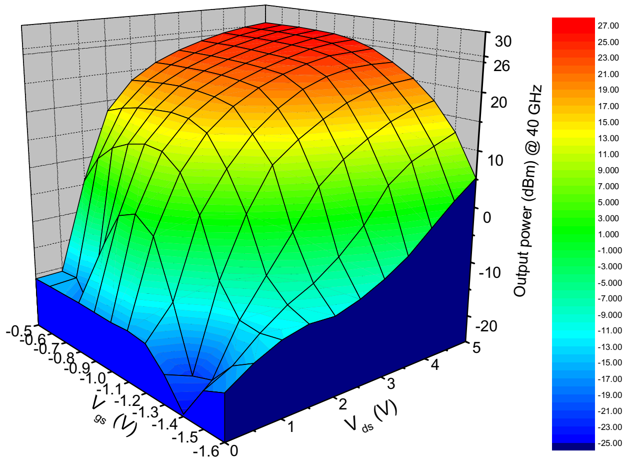

Fig. 7: Measured CW output power at 40 GHz and P$_{in}$ = +5 dBm for the PA MMIC over the DC IV space.

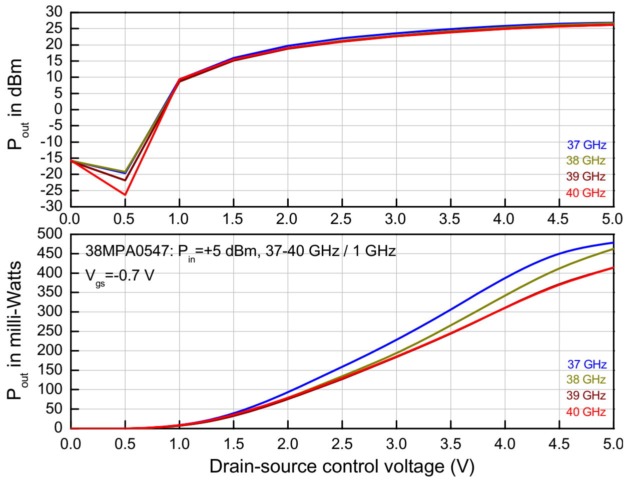

Fig. 8: Example of simple output power control sequence through the drain bias voltage <u>only</u> (P$_{in}$ = +5 dBm, V$_{gs}$ =-0.7V, 37-40 GHz).

The second bias control solution, illustrated in Fig. 8, is preferable since it is simple and allows adjustment of the output power without sacrificing much in the way of input (IIP$_3$) or output third order intercept point (OIP$_3$) as shown in Fig. 9 and 10. Fig. 9 illustrates the variation of the output third order intercept point at a center frequency of 40 GHz and P_{in} = -19 dBm per tone. The variation of the input referred third order intercept point ($IIP_3 = OIP_3 - Gain$) is shown in Fig. 10 for the same conditions. As shown in Fig. 9 and 10, whereas gate voltage control affects significantly the linearity behavior, at fixed gate voltage between $-0.9 \leq V_{gs} \leq -0.7$ V, the drain voltage can be decreased without destroying the OIP$_3$ (or IIP$_3$). Namely, OIP$_3$ stays nearly constant at +36 dBm for a V_{ds} decrease from 5 to 3 V. This behavior is consistent with the PHEMT device linearity characteristic that is (to some extent) mainly related to the transconductance profile as a function of V_{gs} and V_{ds}. Finally in linear mode, gain control is possible either by reducing the drain-source voltage or bringing the PA MMIC toward pinch-off. As shown in

Fig. 11, the power amplifier MMIC achieves more than 30-dB gain at lower drain voltage / high current. The gain can be reduced below -32 dB at $V_{ds} = 2$ V and $V_{gs} = -1.5$ V, which represent an amplifier gain dynamic range of more than 60 dB.

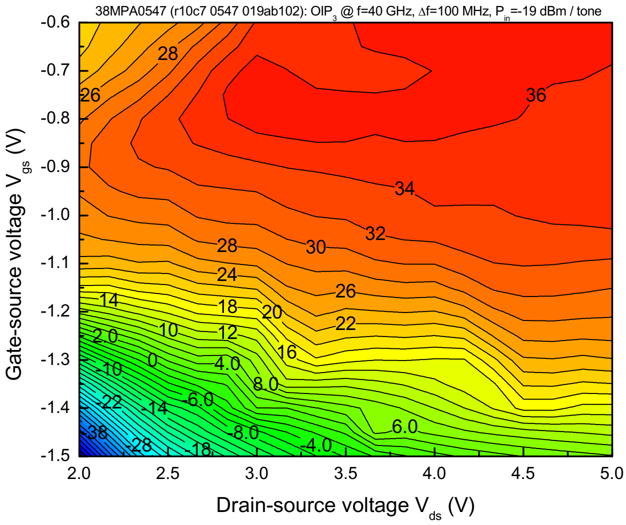

Fig. 9: Measured <u>output</u> third order intercept point (OIP_3) at 40 GHz and $P_{in} = -19$ dBm per tone (Δf=100 MHz) over the DC IV characteristic.

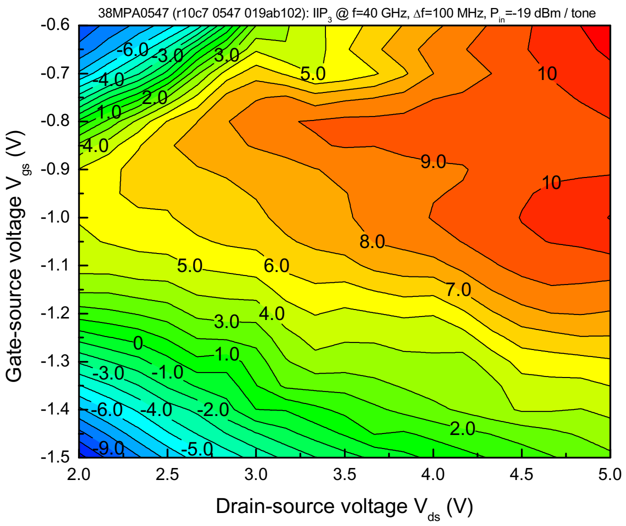

Fig. 10: Measured <u>input</u> referred third order intercept point (IIP_3) at 40 GHz, $P_{in} = -19$ dBm / tone over the DC space.

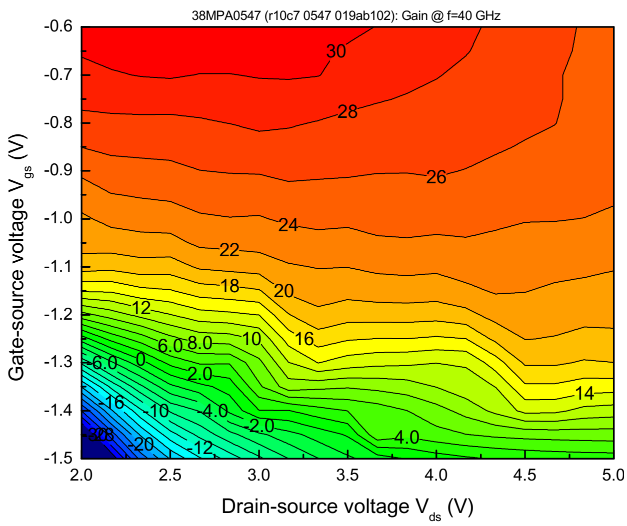

Fig. 11: Measured linear gain at 40 GHz of the PA MMIC over the DC IV space.

Finally, further improvements to the power and gain control, and IIP_3/OIP_3 behavior shown here are possible with individual gate and drain control.

VI. Conclusion

A compact 35-45 GHz power amplifier MMIC with more than 24-dB gain and an output power (near or at saturation) in excess of 400-mW has been developed. Compared to conventional power amplifier MMICs operating at these frequencies, the combined output power and gain densities per chip area are a factor two higher. The ability to control output power level by varying amplifier bias allows the elimination of additional MMIC components, simplifying greatly modern millimeter-wave radio chipsets. By using a standard 0.15-µm power PHEMT process on 6-inch wafers with 100-µm thick substrate, we obtain a significant cost reduction for millimeter-wave radios in the 35 to 45 GHz frequency range.

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