Ka-Band AlGaN/GaN HEMT High Power and Driver Amplifier MMICs

M. van Heijningen[1], F.E. van Vliet[1], R. Quay[2], F. van Raay[2], R. Kiefer[2], S. Müller[2], D. Krausse[2], M. Seelmann-Eggebert[2], M. Mikulla[2], and M. Schlechtweg[2]

[1]TNO Defence, Security and Safety, Oude Waalsdorperweg 63, 2597 AK, The Hague, The Netherlands, email: Marc.vanHeijningen@tno.nl

[2] Fraunhofer Institute of Applied Solid-State Physics, Tullastr. 72, D-79108 Freiburg, Germany.

***Abstract* — In this paper the MMIC technology, design and characterization of a high power amplifier and driver amplifier MMIC at 30 GHz in AlGaN/GaN HEMT technology are presented. The MMICs are designed using CPW technology on a 390 µm thick SiC substrate. The measured small-signal gain of the driver is 14 dB at 28.5 GHz and the measured output power is 28.6 dBm at 28 GHz. The power amplifier shows a measured small-signal gain of 10.7 dB at 25.5 GHz and output power of 34.1 dBm at 27 GHz. Both MMICs have a very good yield and performance for a first iteration design.**

I. Introduction

Gallium-Nitride (GaN) High Electron Mobility Transistors (HEMTs) grown on Silicon-Carbide (SiC) substrates are ideally suited for the realization of high-power amplifier (HPA) Monolithic Microwave Integrated Circuits (MMICs). The advantages of this technology are the high breakdown voltage, high power density and very good thermal conductivity of the semi-insulating (s.i.) SiC substrate. Examples of GaN MMICs up to Ka-Band have been presented [1-4], showing power densities up to 5 W/mm at 50 Ω load impedance. Recent improvements in the GaN HEMT technology have enabled the design of small size, high power amplifier MMICs up to Ka-Band [3,4], making this technology suitable for telecommunication, multimedia, defense and satellite communication applications. The major development activities are currently located in the USA, with a large military force behind it. The export of such technology is problematic. Europe however, is catching up fast now, with research programs funded by o.a. the ESA, national ministries of defense and civil industry. This paper presents a driver amplifier and high-power amplifier MMIC chip-set, developed for the ESA and designed in the AlGaN/GaN technology [6]. The design specifications are an output power of 37 dBm and a total gain of 27 dB from 29.5 GHz to 30 GHz. First, the performance of the AlGaN/GaN HEMT process is described, followed by the MMIC design procedure. Finally, the simulation and measurement results for these two MMICs are presented with a short analysis of the measured performance.

II. GaN HEMT MMIC Technology

The AlGaN/GaN HEMT technology is based on multiwafer MOCVD growth on 2 inch s.i. SiC substrates based on an Aixtron 2000 multiwafer reactor. The T-gate technology is e-beam defined with a gate length of 150 nm. Device isolation is achieved with mesa isolation. Devices with a gate-width of 0.48 mm yield a maximum drain current of > 1.1 A/mm and a transconductance of > 275 mS/mm at V_{DS} = 7 V. The current gain cut-off frequency f_T of the 0.48 mm device is well beyond 50 GHz at V_{DS} = 7 V. The maximum frequency of oscillation at V_{DS} = 7 V amounts to f_{MAX} > 80 GHz. Currently the maximum operational voltage is V_{DS} = 35 V with a corresponding on-state breakdown voltage of BV_{DS}> 65 V. CW loadpull measurements for a 0.4 mm device yield a saturated output power density of 4 W/mm at 30 GHz, a linear gain of 5 dB at V_{DS} = 33 V tuned for maximum output power by active loadpull in CW operation. Fig. 1 gives the details of the measurement. The thermal conductivity of the s.i. SiC substrate is found to be 350 W/mK and used for thermal simulations. The passive coplanar elements feature line, MIM capacitances, inductances and junctions.

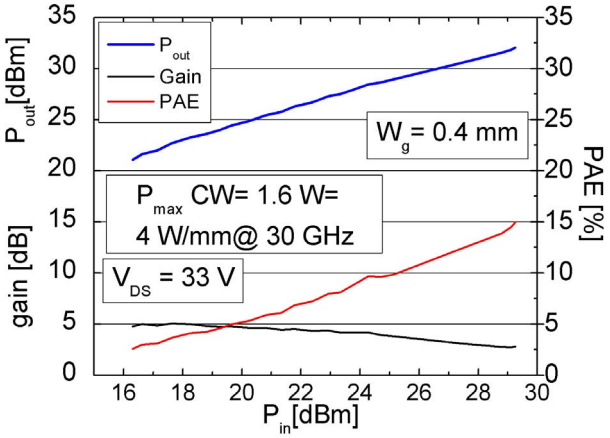

Fig. 1 Measured performance of an 8x50 µm FET at 30 GHz.

Test structures were processed in an initial run and are shown in Fig. 2. A matched transistor with a gatewidth of 8x60 µm yields an S_{21} of 6 dB at 32.5 GHz with appropriate matching of S_{11} <-10 dB and S_{22} < -10 dB.

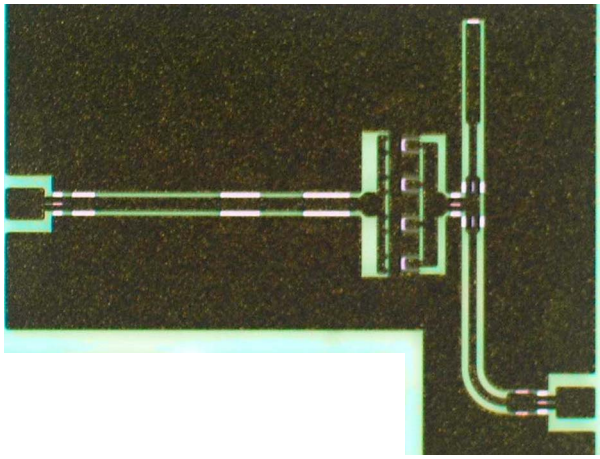

Fig. 2 Image of the 8x60 µm teststructure matched to 50 Ω.

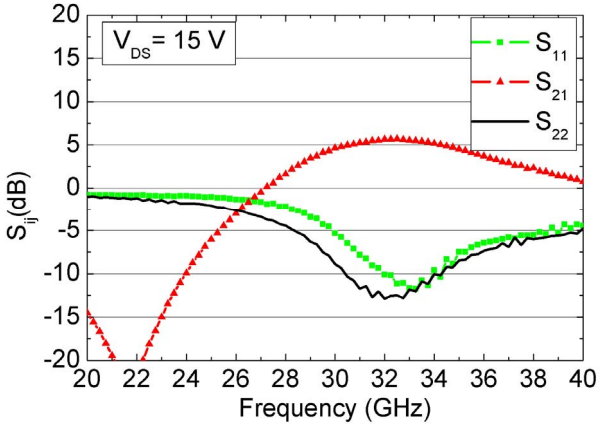

Fig. 3 Measured S-parameters of an 8x60 µm teststructure matched to 50 Ohms at V_{DS} = 15 V.

III. Modeling

For the actual design of the MMICs a full ADS design kit is available including large-signal models for the FETs [5] and models of the CPW passives and transmission lines for 2 different ground plane spacings (50 µm and 100 µm). For the large-signal modeling of the device, a proprietary large-signal model is available and extracted for the power cells of 0.48 mm and 0.24 mm including thermal effects, self-heating and low frequency dispersion.

IV. MMIC Design

The design of the amplifier has started by selecting an appropriate device for the output stage. It turned out that an 8x60 µm FET showed an optimum between gain and output power. Using the power density of 3.7 W/mm, 0.5 dB power margin for process variation and 1 dB loss in the output combiner, four of these devices in parallel are needed to deliver the HPA output power specification of 37 dBm. The first stage of the power amplifier consists of two 8x60 µm FETs. Since the targeted gain of 27 dB is too high to realize on a single chip, it has been decided to make a separate driver MMIC. The estimated performance of the power amplifier is 37 dBm output power with 10 dB gain The driver consists of three stages with a 4x60 µm, 4x60 µm FET and as output an 8x60 µm FET. The estimated performance of the driver is 31 dBm output power and 18 dB gain.

The design of the HPA and driver has been performed according to the methodology presented in [7]. First, loadpull simulations have been performed at different operating points to find the optimum between output power, gain, efficiency and intermodulation distortion. This has resulted in a class-AB operating point at V_{DS} = 30 V, V_{GS} = -3.0 V and a load impedance of 6.65 + j 20.3 Ω for the 8x60 µm FET. For GaN technology this might seem like a rather low impedance. This low impedance is caused by impedance transformation due to the extrinsic drain parasitics. The internal load resistance corresponding with this load is around 110 Ω.

Next, all devices have been made unconditionally stable by adding an RC-network in series with the gate at the expense of 0.7 dB gain loss. The output matching circuit consists of a first low-pass combining section, followed by a bias stub that has been decoupled at 30 GHz. The second combing step is also low-pass, followed by a DC block series capacitor. The drain and gate connections of the four output stage FETs have been directly connected together to prevent any odd-mode oscillations. The interstage matching consists of a drain bias stub, followed by a series capacitor and a low-pass splitter with stubs for the gate bias. The input matching starts with a series capacitor, followed by a low-pass splitter with stubs for the gate bias. The design of the driver MMIC has been performed in a similar way.

V. Driver Amplifier

Fig. 4 gives the chip image of the driver amplifier with a chip size of size 2.75 x 2.00 mm^2.

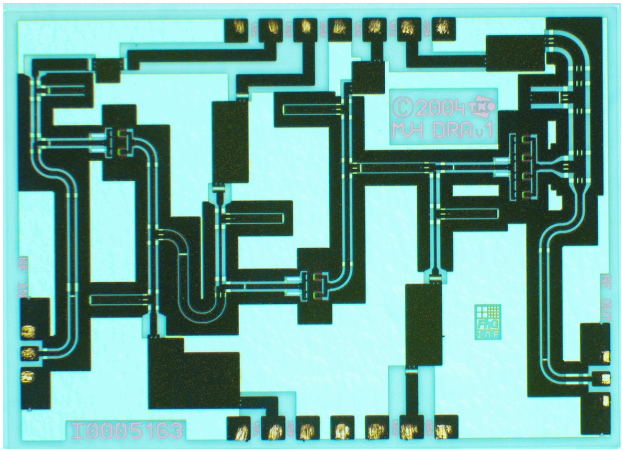

Fig. 4 Chip image of the Driver MMIC, chip size 2.75 x 2.00 mm^2.

Fig. 5 shows the distribution of the measured small signal gain of the driver amplifier over the 2 inch wafer. As can be seen, the distribution is quite uniform and the yield is very good with 20 out of 21 cells or > 95%. Fig. 6 gives the simulated and measured small signal S-parameters between 25 and 35 GHz of the driver. The measurements show a small downward shift in frequency of about 2 GHz. The maximum measured gain is around 14 dB at 28.5 GHz, with respect to 21 dB simulated.

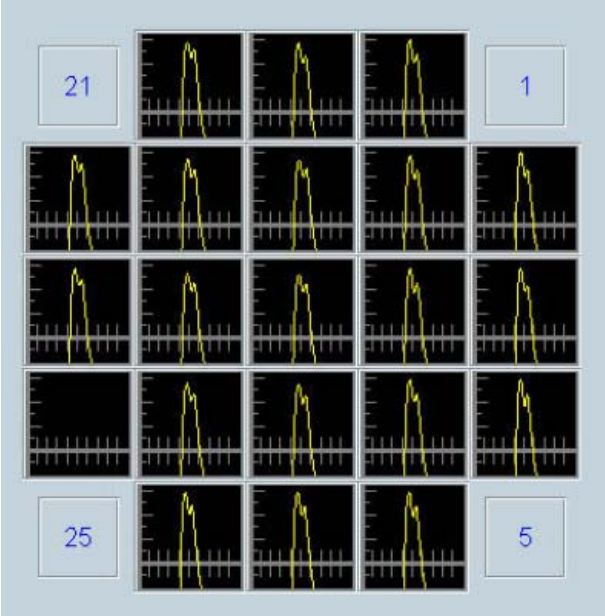

Fig. 5 Distribution of the S-parameter S21 on a 2-inch wafer from 3 to 50 GHz with vertical scale up to 14 dB.

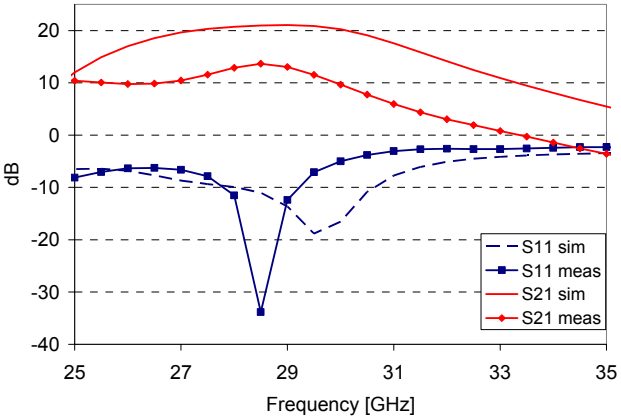

Fig. 6 Simulated and measured small signal S-parameters of the driver amplifier at V_{DS} = 30 V and I_{DStot} = 310 mA.

The CW large signal measurements given in Fig. 7 show an output power of 28.6 dBm at 28 GHz for the driver amplifier.

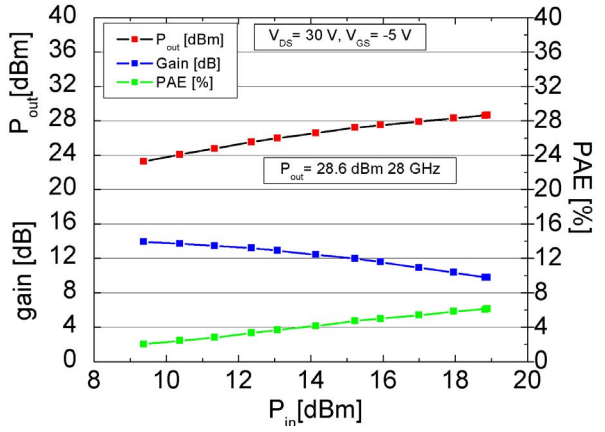

Fig. 7 Measurement CW output power, gain and PAE of the driver amplifier at V_{DS}= 30 V, V_{GS}= -5 V and 28 GHz.

Both gain and output power are lower than expected. This can partly be explained by the fact that the performance of the active devices is lower than simulated and due to mismatch and higher loss of the passive matching circuits. The higher simulated gain can be explained by gm-peaking in the model, which does not correspond with reality. The frequency shift can be attributed to high sensitivity of the passive components, and the circuit design, to process spreading due to the combination of high power transmission lines at small line spacing suitable for the mm-wave range.

VI. High Power Amplifier

Fig. 8 gives the chip image of the HPA MMIC with a chip size of size 2.75 x 3.25 mm^2.

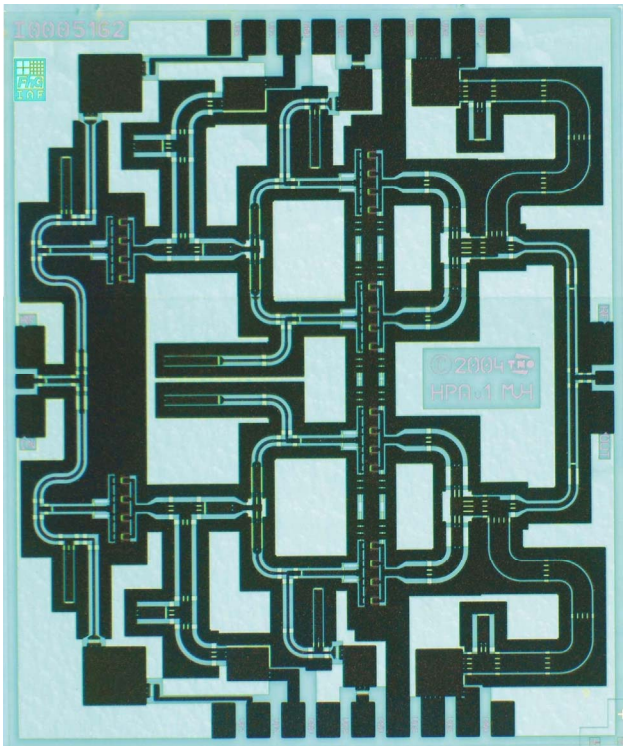

Fig. 8 Chip image of the HPA MMIC, chip size 2.75 x 3.25 mm^2.

Fig. 9 shows the S-parameter measurements in comparison with simulations. Also here a downward shift in frequency and reduction of gain has occurred.

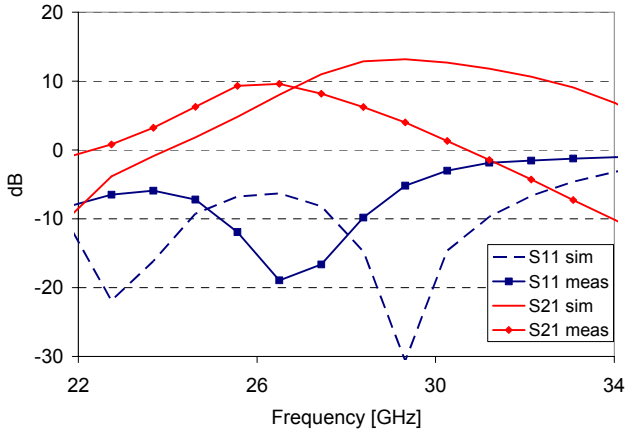

Fig. 9 Simulated and measured small signal S-parameters of the HPA at V_{DS} = 30 V and I_{Dstot} = 636 mA.

The CW output power, gain and PAE measurements are shown in Fig. 10. The maximum measured output power is 34.1 dBm or 2.6 W at 27 GHz, which is lower than simulated, but still a very good performance yielding a power density of 1.35 W/mm for an integrated design at 50 Ω. This exceeds typical GaAs PHEMT values in MMICs by a factor of 3 already at this stage of development in a first shot.

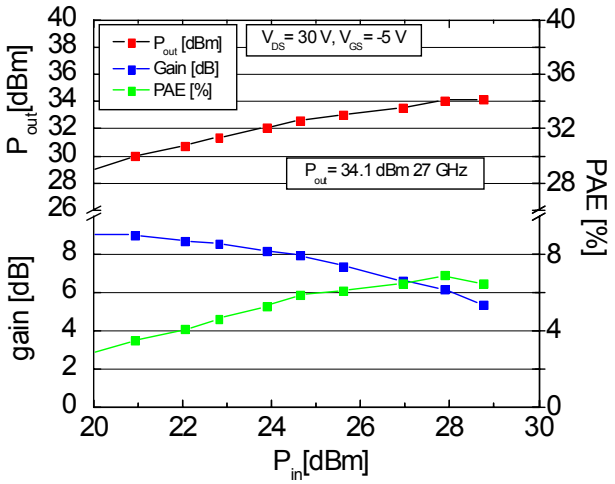

Fig. 10 Measured CW output power, gain and PAE of the power amplifier MMIC at V_{DS}= 30 V, V_{GS}= -5 V and 27 GHz.

To verify the cause of the frequency shift, measurement data of passive test structures has been put back in the simulation. In this case measurements of the stability network have been used. This turns out to be a very sensitive component in the design. Fig. 11 shows the new S-parameter simulation in comparison with the measurement. As can be seen, the frequency shift is also observed in the new simulations.

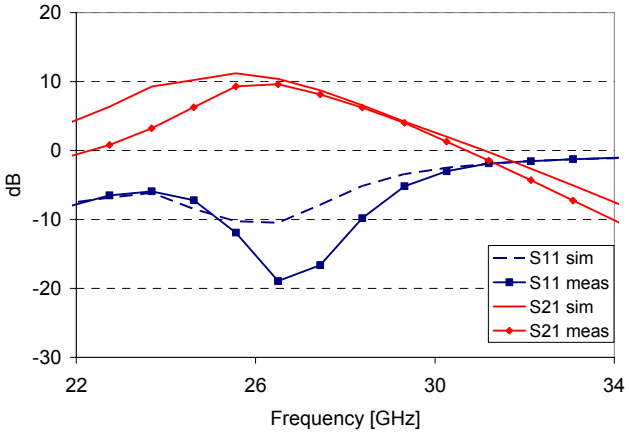

Fig. 11 Simulated and measured small signal S-parameters of the HPA at V_{DS} = 30 V and I_{DStot} = 636 mA, using measured S-parameter data of the stability network.

For both designs, and also for the active devices themselves, the overall efficiency is rather low. This is partly based on the simple planar device concept used, i.e. without a recess, and will be improved in the near future

VII. Conclusion

In this paper the MMIC technology, design and characterization of a high power amplifier and driver amplifier MMIC at Ka-band frequencies in AlGaN/GaN HEMT technology on SiC substrate are presented. The MMICs are designed using CPW technology on a 390 µm thick SiC substrate. The driver shows a measured small-signal gain of 14 dB at 28.5 GHz and an output power of 28.6 dBm at 28 GHz. The HPA has a measured small-signal gain of 10.7 dB at 25.5 GHz and output power of 34.1 dBm, or 1.35 W/mm, at 27 GHz. These are excellent results when considering that this is a first iteration design. With increasing design experience in this technology, improved modeling accuracy and further improved process reproducibility even higher performance figures are near. Overall it has been shown that GaN technology enables the design of integrated high-power amplifiers, which will lower the cost and increase the performance of future microwave systems for a wide range of applications and frequencies.

Acknowledgement

This work has been funded by ESA-ESTEC under contract number 17473/03/NL/CH. The authors further acknowledge the continuous support of the German ministries of education and research (BMBF) and the German ministry of defense (BMVg).

References

[1] J.W. Palmour, J.W. Milligan, J. Henning, S.T. Allen, A. Ward, P. Parikh, R.P. Smith, A. Saxler, M. Moore and Y. Wu, "SiC and GaN Based Transistor and Circuit Advances", Proc. GAAS 2004, Amsterdam, pp. 555–558.

[2] T. Inoue, Y. Ando, H. Miyamoto, Ta Nakayama, Y. Okamoto, K. Hataya and M. Kuzuhara, "30GHz-band 5.8 W High-Power AlGaN/GaN Heterojunction-FET", MTT-S 2004, Fort Worth, pp. 1649-1651.

[3] M. Micovic, Ara Kurdoghlian, H.P. Moyer, P. Hashimoto, A. Schmitz, I. Milosavljevic, P. J. Willadsen, W.-S. Wong, J. Duvall, M. Hu, M. J. Delaney, D. H. Chow, "Ka-band MMIC Power Amplifier in GaN HFET Technology", MTT-S 2004, Fort Worth, pp. 1653-1656.

[4] Y.-F. Wu, M. Moore, A. Saxler, P. Smith, P.M. Chavarkar, P. Parikh, "3.5-Watt AlGaN/GaN HEMTs and Amplifiers at 35 GHz", 2003 IEEE Int. Electron Device Meeting.Dig., pp. 579-581, December 2003.

[5] F. van Raay, R. Quay, R. Kiefer, M. Schlechtweg G. Weimann, "Large signal modeling of AlGaN/GaN HEMTs with Psat > 4 W/mm at 30 GHz suitable for broadband power applications", MTT-S 2003, Philadelphia pp. 451-454.

[6] R. Quay, R. Kiefer, F. van Raay, H. Massler, S. Ramberger, S. Müller, M. Dammann, M. Mikulla, M. Schlechtweg, G. Weimann, "AlGaN/GaN HEMTs on SiC operating at 40 GHz", 2002 IEEE Int. Electron Device Meeting.Dig., pp. 673-676.

[7] A.P. de Hek, "Design, Realisation and Test of GaAs-based Monolithic Integrated X-band High-Power Amplifiers", ISBN 90-386-1920-0, July 2002.