Simplified Validation of Non-Linear Models for Micro- and Millimeter-Wave Electron Devices

A.Raffo [^♣], A.Santarelli [°], P.A.Traverso [°], G.Vannini [^], F.Filicori [°]

[^] Department of Engineering, University of Ferrara, Via Saragat 1, 44100 Ferrara, Italy
[°] Department of Electronics, University of Bologna, Viale Risorgimento 2, 40136 Bologna, Italy
[♣] CoRiTeL, Via Anagnina 203, 00040 Morena (Rome), Italy

***Abstract* — Large-signal modelling of electron devices for nonlinear MMIC design is a fundamental topic for the microwave community. Many different non-linear modelling approaches have been proposed in the last years, and quite often circuit designers suffer from the lack of reliable comparison criteria to identify which model (between those available) could be the most suitable for the desired application. Moreover, similar strategies are needed even from the research groups, whose activity is devoted to the model identification and extraction, in order to quantify the degree of accuracy achievable by the modelling approach adopted. In this paper an approach to verify large-signal model accuracy will be discussed, which is simply based on the comparison between de-embedded measurements and model predictions of Y-parameters versus the bias voltages at the intrinsic device ports.**

I. INTRODUCTION

The problem to quantify the degree of accuracy achievable by the electron device model adopted is a real critical point [1], since many of the models, which are oriented to the design of large-signal circuits, are extracted only on the basis of DC I/V characteristics and small-signal differential parameters measured onto a grid of different bias points. Most of research laboratories do not actually have the capabilities of carrying out the set of large-signal measurements, which should be necessary in order to fully validate their models for each particular application. Large-signal measurement systems can be very expensive (e.g. active load-pull systems) and\or characterized by limited range (e.g. LSNA set-ups are not available above 50 GHz). In addition, simplified procedures, which are based on the comparison between empirical data and model predictions under small-signal operation and can be carried out directly in the software environment exploited for the model extraction (without the need for external CAD tools - e.g. HB simulations), definitely represent an important resource in order to rapidly achieve successful preliminary verification results.

Thus the question is, which small-signal tests are the most suitable to investigate the accuracy achievable by a nonlinear dynamic model?

A first response could be to simply compare the model predictions to the small-signal measurements over the entire frequency and bias sweeping range. Such a "massive" approach could be misleading; in fact, by considering for example a simple class-A power amplifier design, it is evidently not true that all the bias conditions have the same impact on the accuracy of model predictions, which are of interest for this application (e.g. PAE, power at a dB-specified compression point, etc.). Improvements can be certainly achieved by considering only, or weighting mostly, the small-signal parameters that refer to bias conditions "near" the PA loadline. Similar considerations can be made in the framework of the design of a "cold-FET" mixer, where the operation is limited to the linear region of the FET, which is typically biased with VDS= 0 V.

Once the bias sub-grid has been suitably defined, on which model predictions and measurements will be compared, the next problem to be dealt with is what kind of verification has to be used. A natural answer would be that of verifying the accurate fitting between S-parameter simulations and measurements. In practice, the choice of scattering parameters is only related to the fact that measurements with resistive terminations ensure the transistor stability, while the use of short/open loading conditions, which is associated with the direct measurement of admittance or impedance matrix, could easily lead to unstable behaviour. Under many bias conditions Y-parameters could not exist at the extrinsic device ports, but they certainly exist for the intrinsic device i.e. the device obtained after de-embedding from a suitable linear extrinsic parasitic network (see Fig. 1).

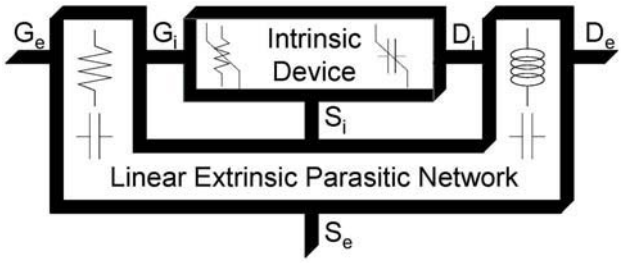

Fig. 1. Representation of a generic electron device in terms of an intrinsic device and extrinsic parasitic elements.

In fact, an ideal Y measurement performed at the intrinsic device implies to short (for the AC components) the input or output intrinsic ports by fixing the charge over the intrinsic device capacitances; since the capacitance charge is a state variable it is clear that under such test conditions the device can not become unstable.

In this paper an approach to verify large-signal model accuracy will be discussed, which is simply based on the comparison between de-embedded measurements and model predictions of small-signal Y parameters versus the bias voltages at the intrinsic device ports. Moreover,

it will be preliminary shown as a suitable metric, based on bias- and frequency-dependent small-signal Y parameters, can be adopted to assess the accuracy of an electron device model under nonlinear operations.

II. The Small-Signal Validation Procedure.

As well-known, at the intrinsic device ports the device can be described (at least until the non-quasi stationary effects can be neglected) by a simple G(V)-C(V) parallel, where V represents the vector of the intrinsic voltages. Under these hypotheses, a more convenient comparison can be made by taking into account Y parameters. In fact, by assuming, for instance, a non-linear polynomial i(v) description for the device, it is well-known that third-order intermodulation (IMD) products are related to third-order derivatives of the currents with respect to the voltages, i.e. the second-order derivatives of the Y-parameters. The quality of the Y-parameters fitting versus the bias conditions is then explicitly related to the performances under large-signal operating condition, but it is important to notice that it would not be sufficient to compare models simply on the basis of the best fitting of Y-parameters, since it would be also fundamental to have a good fitting of second-order derivatives in order to obtain optimum performances. In other words, it would be useful to verify the accuracy shown by the model in reproducing concavities and convexities of the curves, which are obtained by plotting the Y-parameters versus the bias.

It must be observed that the de-embedding of the parasitic networks is always useful because linear parasitic elements tend somehow to hide the non-linear phenomena, which are strictly related to the intrinsic device; therefore a good small-signal, bias-dependent fitting at the extrinsic device ports does not necessary imply good prediction accuracy under large signal operating conditions. In fact, while a good fitting of the bias-dependent G(V)-C(V) intrinsic functions evidently implies accurate predictions under non-linear operation, a good fitting of the extrinsic parameters does not guarantee the same results. In the latter case, it is only possible to state that the model shows a good extrinsic small-signal parameter fitting, but this could be easily obtained by exploiting, for instance, an arbitrary, large number of linear elements in the modelling of the parasitic network. Furthermore, when the analysis of the extrinsic S-parameters manifests an inaccurate fitting with measurements, it is not immediate to understand what kind of non-linearity the model fails to describe: either the quasi-static non-linearity strictly related to the bias-dependent G(V) intrinsic function, or the dynamic non-linearity shown by the bias-dependent C(V) intrinsic function.

A final consideration is that the strong source of device non-linearity is the low-frequency I/V device characteristic with the associated, important dispersive phenomena due to traps and self-heating.

To show the great impact of the low-frequency modelling, two different models for FET devices have been considered here: the "Backgating" model [2] and a recently proposed look-up-table based "Empirical" model [3]; both of the models exploit, besides small-signal measurements, large-signal ones carried out with a recently proposed setup [4].

To test the small-signal prediction capability of the i/v models, measurements of a Triquint 0.25µm GaAs PHEMT low-frequency trans- and output-conductance were carried out for different biases at 2 MHz - i.e. well above the trap cut-off - and compared with the Empirical and Backgating model predictions. Corresponding results are shown in Fig. 2. As can be seen, the Empirical model is more accurate and also capable to perfectly reproduce concavity and convexity of the "measured" intrinsic transconductance. Analogous results have been obtained for the output conductance.

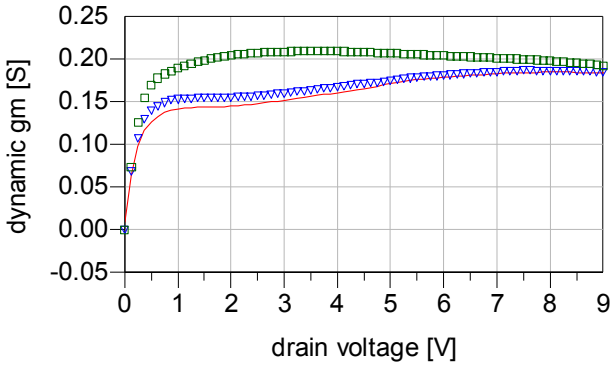

Fig. 2. Intrinsic trans-conductance of a 0.25µm Triquint GaAs PHEMT at different drain biases and Vg0= -0.55V (f = 2 MHz). Measurements (solid line) versus predictions based on Backgating (squares) and Empirical (triangles) models.

The low-frequency drain current models extracted have been embedded in a non-quasi-static large-signal device model for millimeter-wave applications, namely the Nonlinear Discrete Convolution (NDC) model presented in [5]. A conventional bias-dependent S-parameter comparison at the extrinsic device ports does not point out any relevant difference between the two models at microwave frequencies (40 GHz) as shown in Fig. 3 where the second derivatives with respect to the drain voltage of the S21 parameter real part computed with the different models are displayed. On the contrary, the comparison of the intrinsic Y parameters underlines an evidently better prediction capability of the NDC model with embedded the "Empirical" I/V model, especially in the reproduction of the shape of the measured data as can be seen in Fig. 4 where the second derivatives with respect to the drain voltage of the Y21 parameters real part are reported. The higher accuracy of the NDC/Empirical model with respect to the NDC/Backgating one is confirmed also by intermodulation measurements as will be shown in the next Sections.

III. The Proposed Metric

The comparison between intrinsic *Y* parameters can provide useful information, as shown in the previous section. Additionally, a suitable metric can be defined at the intrinsic device ports [6] to estimate the achievable

accuracy of a given model under *virtual* high-frequency nonlinear operation.

We assume here that the accuracy of the DC/low-frequency characteristics of the model has been previously verified, so that the model inaccuracies at high-frequency are mainly due to the purely dynamic nonlinear model response.

The classical bias-dependent small-signal parameters $Y[V_B,\omega]$ are here conveniently expressed as follows:

$$Y[V_B,\omega]=\tilde{Y}[V_B,\omega]+g_{DC}[V_B] \quad (1)$$

where g_{DC} represents the static conductance while $\tilde{Y}[V_B,\omega]$ is the purely-dynamic contribution to the admittance (that is $\tilde{Y}=0$ for ω=0).

By adopting a device description similar to [7], a useful metric can be defined on the basis of the dynamic admittance (1). In particular, according to (1) we may define an associated *predicted* purely-dynamic admittance $\tilde{Y}^P[V_B,\omega_0]$ and a *measured* purely-dynamic admittance $\tilde{Y}^M[V_B,\omega_0]$ of the intrinsic device. Thus, for each bias condition, the deviation between predictions and measurements can be evaluated:

$$\Delta\tilde{Y}[V_B,\omega_0]=\tilde{Y}^P[V_B,\omega_0]-\tilde{Y}^M[V_B,\omega_0]. \quad (2)$$

Deviation (2) can be used to build a suitable metric for the accuracy evaluation of a purely quasi-static or moderately nonquasi-static nonlinear model in a *virtual* large-signal test [6]. In particular, suitable theoretical analysis [6] proves that the following error term:

$$\Delta I_{RMS}^2 \cong \frac{1}{N}\sum_{n=1}^{N}\left(2\,\mathrm{Re}\left[\Delta\tilde{Y}\left[v\left(n\cdot\frac{T}{N}\right),\omega_0\right]V_A e^{j2\pi\frac{n}{N}}\right]\right)^2 \quad (3)$$

represents the deviation between the predicted and measured RMS device current under large signal operation for a strictly quasi-static or moderately nonquasi-static device[1] . On this basis, a final figure of merit can be defined as:

$$\varepsilon=\sqrt{\frac{\Delta I_{RMS}^2}{I_{RMS}^{M\ 2}}}, \quad (4)$$

where the normalization term $I_{RMS}^{M\ 2}$ has been adopted as:

$$I_{RMS}^{M\ 2} \cong \frac{1}{N}\sum_{n=1}^{N}\left(2\,\mathrm{Re}\left[\tilde{Y}^M\left[v\left(n\cdot\frac{T}{N}\right),\omega_0\right]V_A e^{j2\pi\frac{n}{N}}\right]\right)^2 . \quad (5)$$

The error term (4) can be easily extended to the two-port device case considering the four $\Delta\tilde{Y}_{xx}$ terms referring to the four Y-parameters. Two error terms ε_1 and ε_2 are obviously defined in this case, corresponding to the input and output currents.

IV. Example of Use for the Proposed Metric

In order to validate the proposed metric, three different nonlinear models were extracted for a Triquint 0.25μm GaAs PHEMT . The first two models correspond to those considered in section I. In particular, we call "**A**" and "**B**" the NDC/Backgating and the NDC/Empirical models, respectively. Moreover, a conventional, purely quasi-static equivalent circuit model ("**C**") was also considered.

The metric has been here preliminary validated under class-A operating conditions, with special attention paid to device application in high-linearity Power Amplifier design. In this case, the N voltage samples $v(n\cdot T/N)$ in (3) correspond to the sinusoidal voltage excitations at the intrinsic device ports evaluated on the basis of ideal class-A operation of the electron device[2]. In particular: the device was biased at V_{gs0} = -0.6 V, V_{ds0} = 5.5 V; sinusoidal voltages at the frequency of 40-GHz at the intrinsic device ports were considered here, with amplitude equal to 0.6 V at the gate port (in order to avoid forward conduction of the gate diode) and to 4.5V (in order to avoid the knee region during the device operation) at the drain port.

In Table I the evaluated two port error terms are shown for the three modeling approaches considered. It should be noted as the two model **A** and **B**, that differ for the low-frequency description, present the same value for the ε_1 error (the gate current is not affected by dispersion in both models). Instead, the error ε_2 associated to the drain current is lower for the **B** model clearly indicating in what kind of nonlinearities the compared models differ. The metric shows also that the model **C** has the lower level of accuracy.

In order to validate the predictions provided by the metric about the performance of the models considered, the actual accuracy of the approaches **A**, **B** and **C** under nonlinear high-frequency operation has been tested, by comparing simulations and measurements of the third-order intermodulation product to carrier ratio (I/C), carried out at 39.9 GHz (two tone displacement: 10 MHz; class-A operation: I_D=60 mA, V_{DS}=6.5 V). Simulation and measurement results are shown in Fig.5 versus the output power. As shown, the predictions provided by the NDC/Backgating model **A** are in good agreement with measurements, despite the very low level of the intermodulation products required by the specific application.

In the same figure, the simulation results obtained by switching to NDC/Empirical model **B**, which allows for the highest level of accuracy, are also shown. Finally, the worse prediction capabilities obtained by making use of the equivalent circuit model **C** are reported. Similar results have been obtained under different load and source termination conditions, confirming the validity of the new metric presented.

V. Conclusion

In this paper a methodology to verify the prediction accuracy of a non-linear model under large-signal operating conditions has been proposed, which is based

[1] Theoretical, experimental results show that the accuracy is still acceptable under the typical, mild non quasi-static regime of microwave electron devices.

[2] Different classes of operation (e.g., AB or B) could also easily be considered.

	ΔI^2_{1RMS}	ΔI^2_{2RMS}	$I^{M}_{1RMS}{}^2$	$I^{M}_{2RMS}{}^2$	ε_1	ε_2
"A"	0.000061	0.001002	0.023875	0.062562	0.050320	0.126510
"B"	0.000061	0.000055	0.023875	0.062562	0.050320	0.029450
"C"	0.000901	0.015722	0.023875	0.062562	0.194260	0.501310

TABLE I

Evaluation of the three device modelling approaches considered by means of the new metric proposed.

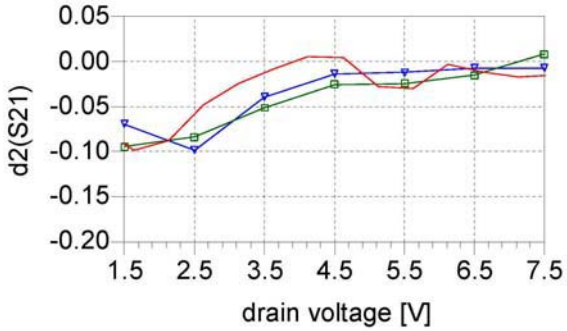

Fig. 3. 2nd-order derivative of the extrinsic real part of the S21 parameter (40 GHz) for the Triquint GaAs PHEMT at different drain biases and Vg0= -0.55V. Measurements (solid line) versus predictions of the NDC/Backgating (squares) and NDC/Empirical (triangles) models.

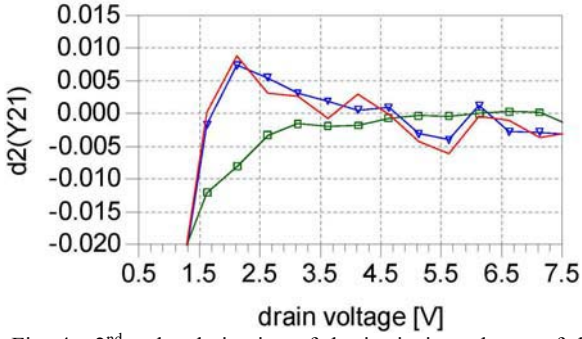

Fig. 4. 2nd-order derivative of the intrinsic real part of the Y21 parameter (40 GHz) for the Triquint GaAs PHEMT at different drain biases and Vg0= -0.55V. Measurements (solid line) versus predictions of the NDC/Backgating (squares) and NDC/Empirical (triangles) models.

on simple comparison of small-signal Y parameters at the intrinsic device ports.

In particular, it has been preliminary outlined, by exploiting a new metric formulation [6], as the evaluation of the accuracy of Y parameters can be linked to the grade of non-linear model accuracy and also to what kind of non-linearity the model fails to describe.

ACKNOWLEDGEMENT

This work was partly funded by the Italian Ministry of Instruction, University and Research within the project "Modelli di dispositivi elettronici per il progetto di circuiti integrati monolitici a microonde ed onde millimetriche per collegamenti radio di nuova generazione ad elevate prestazioni" and also performed in the context of the network TARGET – "Top Amplifier Research Groups in a European Team" supported by the Information Society Technologies Programme of the EU under contract IST-1-507893-NOE, www.target-net.org.

REFERENCES

[1] M.Miller; M.Golio; B.Beckwith; E.Arnold; D.Halchin; S.Ageno; S.Dorn, "Choosing an optimum large signal model for GaAs MESFETs and HEMTs," in *1990 IEEE MTT-S Int. Microwave Symp. Dig.*, vol. 3, pp. 1275-1282.

[2] A.Santarelli, et al. "Backgating model including self-heating for low-frequency dispersive effects in III-V FETs," Electron. Lett. , vol.34 no. 20, pp. 1974 - 1976, Oct. 1998.

[3] A.Raffo, et al. "Improvement of PHEMT Intermodulation Prediction Through the Accurate Modelling of Low-Frequency Dispersion Effects," in *IEEE MTT-S Int. Microwave Symp. Dig.*, Jun *2005*

[4] A.Raffo, A.Santarelli, P.A.Traverso, G.Vannini, F.Filicori, "On-wafer I/V measurement setup for the characterization of low-frequency dispersion in electron devices," in *IEEE 63rd ARFTG Dig.*, Jun. 2004, pp. 21 – 28.

[5] F.Filicori, A.Santarelli, P.A.Traverso, G.Vannini, "Electron device model based on Nonlinear Discrete Convolution for large-signal circuit analysis using commercial CAD packages," in *Proc GAAS99*, 1999, pp.225-230.

[6] A.Raffo, A.Santarelli, P.A.Traverso, G.Vannini, F.Filicori, "A Small-Signal Parameter Based Metric for Nonlinear Models of Micro- and Millimeter-Wave Electron Devices," to be published.

[7] F. Filicori, G. Vannini, and V. Monaco, "A nonlinear integral model of electron devices for HB circuit analysis", *IEEE Trans. Microwave Theory Tech.*, Vol. 40, pp. 1456-1465, Jul 1992.

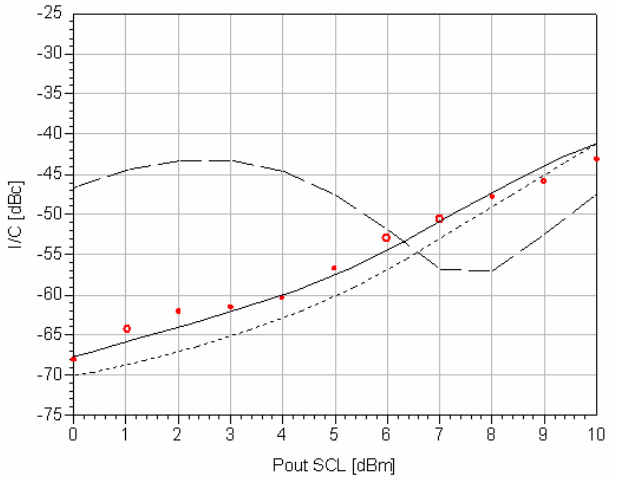

Fig. 5. Third-order intermodulation product to carrier ratio versus output power (Single Carrier Level) for the 0.25µm Triquint GaAs PHEMT at 39.9 GHz [Bias: Id0 = 60 mA, Vd0 = 6.5 V, Load Γ_L = (0.7∠168°), Source Γ_S = (0.871∠-177°)]. Measurements (circles) are compared to predictions based on **A** (dot line) **B** (solid line) and **C** (dashed line) models.