

A High Purity 60 GHz-Band Single Chip X8 Multiplier with Low Phase Noise

Camilla Kärnfelt, Rumen Kozhuharov, and Herbert Zirath

Chalmers University of Technology, Department of Microtechnology and Nanoscience,
Microwave Electronics Laboratory, Kemivägen 9, SE-412 96 Göteborg, Sweden
phone +46-31-772 1738, fax +46-31-16 45 13, e-mail Camilla.Karnfelt@mc2.chalmers.se

Abstract — A single chip multiplier by eight (x8) MMIC for 52-62 GHz output frequency is presented. The multiplier consists of quadrupler stage followed by a high pass filter, an inter-stage amplifier and a doubler stage. The required output power is achieved by a two stage buffer amplifier on the output.

An output power exceeding 7 dBm is achieved from 52 to 61 GHz. The rejection of the unwanted harmonics is better than 28 dB and the detected degradation of phase noise due to the circuit is less than 1dB at 100 kHz offset from the carrier, compared to a theoretical value of 18.06 dB for a multiplier by eight. The bias configuration is optimized to reduce the number of the required bias voltages to three. The total power dissipation is 450 mW.

The MMIC is designed and manufactured in a commercial 0.15 μm pHEMT process from WIN foundry.

To our knowledge this is the first reported MMIC multiplier by eight based on PHEMT technology.

Index Terms — doubler, LO-chain, MMIC, quadrupler, x8.

I. INTRODUCTION

In future wireless communication systems the 60 GHz band is considered to be used in several cases such as multimedia communication, inter-vehicle communication and roadside communication [1]. To enable such systems, signal generation with stabilized frequency and low phase noise is needed.

The signal can be generated either directly by a fundamental-frequency oscillator or by the combination of a low frequency integrated oscillator and a few frequency-multiplier stages. The use of frequency multipliers to create millimeter-wave signals is an attractive alternative to direct generation of the signal if phase locking is required since, in this case, frequency dividers are required. Frequency dividers are not available commercially for mm-waves, and in addition, they consume significantly more dc-power. Another advantage of signal generation using multipliers is lower phase noise since the lowest phase noise VCOs are realized at lower frequencies [2]. Most active multipliers have generally been configured as frequency doublers [3]-[5], or quadruplers [6]-[8].

The purpose of this work is to develop a 60 GHz local oscillator (LO)-chain based on pHEMT technology for further integration in a single chip transmitter/receiver circuit [9]. A multiplier by eight is designed and

implemented on single chip using 0.15 μm GaAs pHEMT technology¹.

II. CIRCUIT DESIGN AND MEASUREMENTS

The objective for this design was to make a broadband multiplier to cover the VCO frequency range from 7.0 to 7.7 GHz with an output power of the 8th harmonic of 10 dBm. The input power is specified to be 0 dBm. The signal suppression of other harmonics (fundamental, 2nd, 3rd, ..., 7th) was specified to be more than 20 dB below the 8th harmonic.

The multiplier by eight (x8) has a circuit topology according to the diagram in Fig. 1. It includes a quadrupler followed by a doubler and a 2-stage buffer amplifier at the output.

This topology is chosen to enable the high level of integration. It is accomplished with only two multiplier stages, x4 and x2. The input matching and interstage amplification are designed also to occupy a minimum of the chip area.

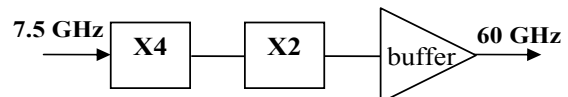


Fig. 1. Multiplier block diagram

Each part of the LO-chain has been made as a break out circuit. This has enabled the investigation of the break outs circuits separately preceding the evaluation of the complete x8. The photograph of complete single-chip x8 is shown in Fig. 2.

The measurement equipment used in this work is a PNA network analyzer E8361A for S-parameter measurements. A synthesizer HP83650B was used as input signal source and the output power was evaluated by a HP8565EC spectrum analyzer with pre-selector HP11974. A power meter HP4419B was used with a V8486A power sensor to verify the power sensed by the spectrum analyzer.

¹ WIN PP15-20 0.15 μm power pHEMT process

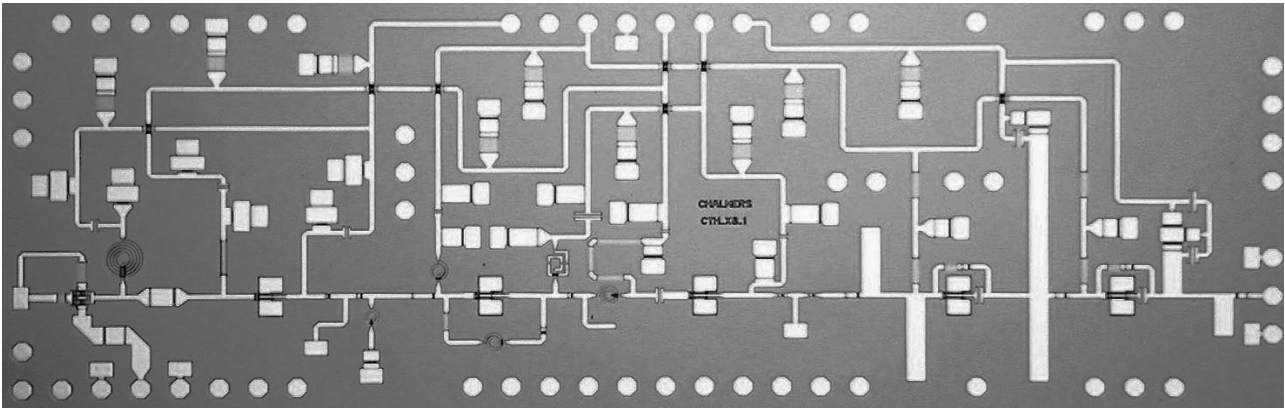


Fig. 2. Photograph of the x8 MMIC. The chip size is 5.0 x 1.6 mm.

A. The Quadrupler

The input stage of the x8 is a two stage quadrupler. The first stage is a grounded gate transistor which has the advantages to achieve large frequency range matching and improved stability while it requires only a small chip area.

The nonlinearity used to generate harmonic frequencies is clipping of the I_{ds} waveform induced by biasing the second stage at pinch-off. The matched load for the fourth harmonic and effective rejection of unwanted harmonics is accomplished by a two pole high pass filter at the output.

In Fig. 3, the measured output power of all harmonics versus input frequency is shown.

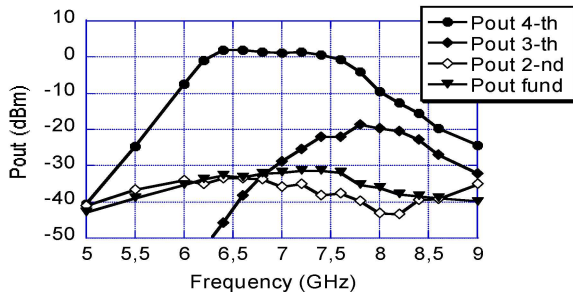


Fig. 3. Measured output power of the 4th, 3rd, 2nd harmonic and fundamental frequency versus frequency at 0 dBm input power.

The rejection of the 3rd harmonic is more than 20 dB. A maximum output power of more than 2.0 dBm over a 1.8 GHz bandwidth is obtained.

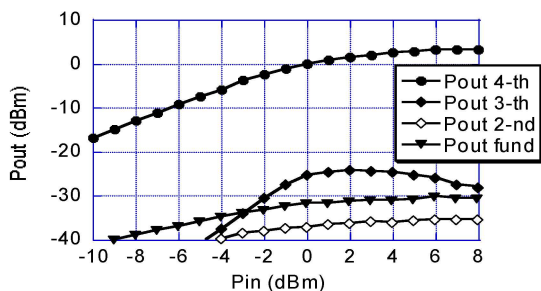


Fig. 4. Measured output power of different harmonics versus input power at 7 GHz.

The measured power dependence of the 4th, 3rd, 2nd harmonic and the fundamental frequency on the input power at 7 GHz are shown in Fig. 4.

B. The Doubler with Feedback Amplifier

The frequency doubler consists of a feedback amplifier (FBA) and a doubler stage. The FBA is realized with negative feedback technique to achieve a wide bandwidth with small gain variation and improved stability. As a result of the feedback arrangement this amplifier has a flat response and a 3 dB bandwidth ranging from 16.5 GHz to 40 GHz.

The doubler stage (x2) is biased at the pinch-off voltage for optimal multiplication conditions. This bias is also beneficial for minimum power dissipation. An effective rejection of the fundamental frequency, i.e. the 4th harmonics from the quadrupler, of more than 20 dB is achieved by an output high-pass filter.

In Fig. 5 measurements of the complete doubler with feedback amplifier is shown. The 1-dB compression point is at -4 dBm input power. At 2 dBm input power (i.e. the amount of power delivered from the quadrupler), the output power is 4 dBm.

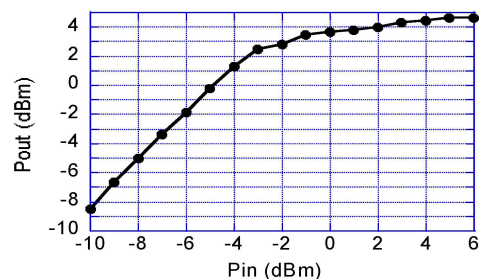


Fig. 5. Measured output power of 2nd harmonic of the two stage doubler versus input power at input frequency of 29 GHz.

The output power dependence on input frequency is shown in Fig. 6. Both the second harmonic and the fundamental frequency are presented.

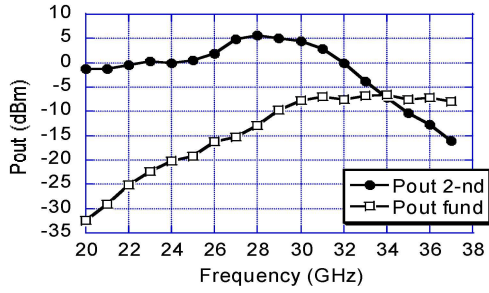


Fig. 6. Measured output power versus frequency of 2nd harmonic and fundamental frequency for the doubler stage. The input power is 0 dBm.

In the input frequency range from 26 to 32 GHz, the doubler's output power is more than 0 dBm at 0 dBm input power. The maximum output power of 5 dBm is reached at 28 GHz input frequency. The rejection of the fundamental signal varies from 18 dB at the lower edge to 10 dB at the upper edge of the frequency band.

C. The Buffer Amplifier

A two stage buffer amplifier is used for further amplification of the output signal from the doubler. This amplifier consists of two feedback stabilized amplifier stages designed to have a flat frequency response from 50 to 65 GHz with input and output matching better than -10 dB. The measured small signal gain is 11 dB with an -1 dB bandwidth of 45-64 GHz, the input and output reflection coefficient is less than -8 dB from 36 to 67 GHz and 48 to 67 GHz respectively. Both the input and the output are matched by two stubs; the input was matched by two open stubs and the output by a shorted and an open stub. The measured amplifier gain versus input power is shown in Fig. 7. Due to the compression, the output gain is 8.5 dB at 0 dBm input power.

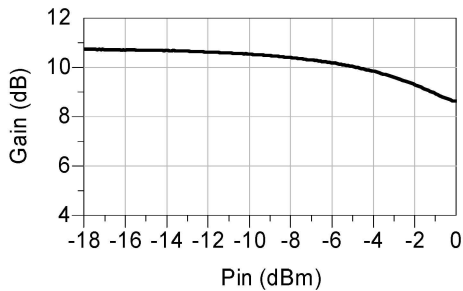


Fig. 7 Measured gain versus input power at 60 GHz.

III. MEASUREMENTS OF THE X8

The complete multiplier was designed utilizing ADS from Agilent. The input matching, simulated and measured, is presented in Fig. 8.

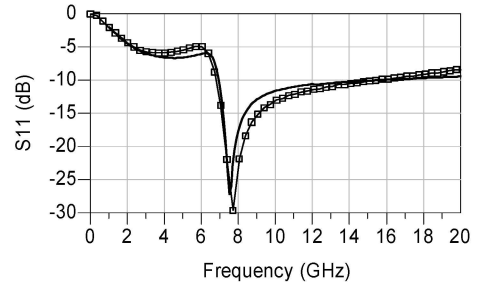


Fig. 8. Input matching of the X8 circuit. Simulated (-) and measured (□) data.

The correspondence between simulated and measured input matching confirms the efficiency of the grounded gate-stage at the quadrupler input.

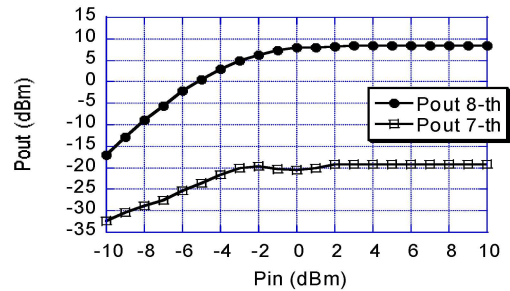


Fig. 9. Measured output power of the 8th and the 7th harmonic versus input power at 7.35 GHz input frequency.

The measured output power is 8.4 dBm with the 1-dB compression point at -7 dBm input power, Fig. 9. The rejection of the nearest harmonics (i.e. the 7th) is 28 dB. At 0 dBm input power the output power at the 8th harmonic is fully saturated.

The second experimental test shows the output power and efficiency versus output frequency, Fig. 10. The efficiency is defined as the ratio of the output power at the 8th harmonic over the sum of the dissipated DC power and the input power at the fundamental frequency. The maximum output power of 11.7 dBm and efficiency of 3.26% are reached at 54.4 GHz. An output power of more than 7 dBm is obtained from 52 to 61 GHz.

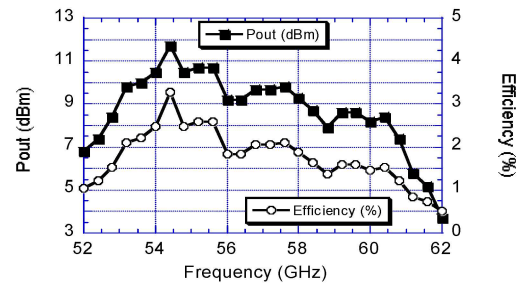


Fig. 10. Measured output power and efficiency versus output frequency. The input power is 0 dBm.

Phase noise is an important characteristic in frequency generation systems, and for that reason evaluation of output phase noise is executed. A frequency multiplier is, in fact, a phase multiplier which multiplies the phase deviation as well as the frequency of the input signal. This causes the phase noise degradation given by $20 \cdot \log(N)$, where N is the multiplication order. In the case of an x8 the theoretical value is 18.06 dB.

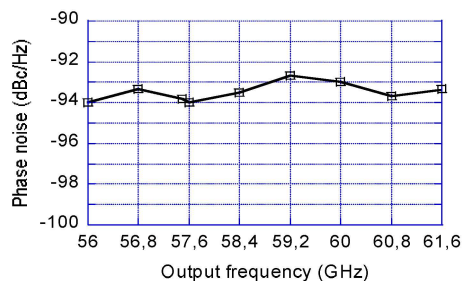


Fig. 11. Measured phase noise at 100 kHz offset from the carrier versus carrier frequency. The input signal phase noise is -111.2 dBc/Hz.

Both the input and output signals phase noise are measured using HP 8565EC with the module HP 85620A. A phase noise of -111.2 dBc/Hz at 100 kHz offset from the carrier is measured at the input of the x8 (i.e. the 7-GHz signal generated in HP 83650B). The measured values at the output show that the degradation is 18.5 ± 0.5 dB; hence the extra phase noise degradation due to the circuit is less than 1dB, Fig.11.

According to the requirement for a low phase noise of LO signal (less than -90 dBc/Hz at 100 kHz offset) to obtain a transmission with low bit error rate ($BER < 10^{-3}$), a recommendation concerning 7 GHz VCO can be made. An HBT VCO with -110 dBc/Hz phase noise will be a reliable decision.

IV. CONCLUSION

A single chip MMIC x8 frequency multiplier is designed and characterized. An output power of more than 7 dBm is obtained from 52 to 61 GHz. The rejection of unwanted harmonics is better than 28 dB. The measured phase noise degradation of 18.5 ± 0.5 dB indicates that this circuit is a good alternative in reaching

low phase noise requirements for a millimeter wave LO-chain.

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