UP-converter for high performance cellular radio test equipment

Alberto Caliumi* Member *IEEE*, ***Leonardo Masini*** * Member *IEEE* , ***Steen Bak Christensen*** **, ***Marcello Aglietti*****
**Laboratori Fondazione Guglielmo Marconi*,Via Porrettana 123 - I-40044 Pontecchio Marconi - ITALY
***GIGA*, Mileparken 22 DK-2740 Skovlunde - DENMARK.
****ITALTEL*, SS 17 Località Boschetto L'Aquila - ITALY

Abstract
Design and realisation of two complex L-Band UP-converters in GaAs technology is presented. This paper describes the architectures chosen for both devices and will focus on the design techniques that should be adopted when RF signals, with different power levels and/or at different frequencies, must meet on the same chip without mutual interferences. The paper will also focus on the electrical modelling of large IC packages for digital VLSI IC's to be used at L-band frequencies. In the cases herein described, low cost and high volume production are not mandatory, while high performance, very high yields, multifunctions on chip, no needs of external interfaces and tuning components, freehold property of the devices and fast and reliable circuit design are the requirements.

Introduction
Since the invention of superheterodyne concept (Armstrong 1918), mixers have assumed an important role in the new age radio-systems. Actually, mixers do not mix in the sense of combining inputs linearly but they multiply frequencies generating complex output products. In this work the multiplying signal concept is adopted to design two UP-converters. The two UP-converters are respectively DC and AC internally coupled. Together with the DC coupled solution, the AC has been implemented particularly to introduce a further degree of freedom for the reduction of in-band spurious. The block diagram of such devices are shown in Fig.1 and Fig.2. As it can be seen from previous figures, the Up-converters includes an input RF switch that enables the selection of LO inputs, an IF preamplifier, also needed to obtain a moderate Noise Figure of the whole device, a mixer, and a RF amplifier. Ancillary devices are a RF output detector and a TTL interface for the switch driver. The requirement for TTL to GaAs FET Logic interfaces [1] on both RFIC's makes them truly mixed analog-digital IC's, thereby calling for both analog and digital design know how.
The main requirements for the frequency converters are: 1) IF input Frequency 220-250 MHz , LO Frequency 1070 - 1250 MHz, RF output Frequency 820-1000 MHz; 2) Output spurious response below 70 dBc in the band 820-1000 MHz; 3) Noise Figure better than 10 dB; 4) Isolation between the two LO's input better than 38 dB; 5) LO-RF Isolation and IF-RF Isolation better than 25 dB; 6) conversion gain up to 13 dB +/-1 dB with LO at 0 dBm; 7) broadband IF input and RF output 50 Ohm matched ports; 8) variation gain Vs. temperature should be +/- 1 dB in the range -40 °C to +85 °C.

Circuit design
The design techniques for such devices are both analog and digital IC's approaches. During the phase design, particular care took the suppression of in-band spurious. This shortcoming should be overcome by means of linearisation of the mixer and differential amplifiers together with the use of a suitable external component. To obtain a good linear behaviour of the whole Up-conversion chain, the gain of the different blocks and their intercept points can be defined using the following formula:

$$IP = \left[\left(\frac{1}{IP_1} \right)^q + \left(\frac{G_1}{IP_2} \right)^q + \left(\frac{G_1 G_2}{IP_3} \right) + \cdots + \left(\frac{G_1 G_2 \cdots G_{n-1}}{IP_n} \right) \right]^{1/q}$$

$q = (m-1)/2; \quad m = order \quad of \quad intercept; \quad G_k = gain \quad of \quad k^{th} - block$

$IP_k = m^{th} - order \quad intercept \quad of \quad k^{th} - block$

$IP = \quad m^{th} - order \quad cascaded \quad intercept \; point$

Even if the DC coupling solution leads to broadband performances and easier RF test set-up, the adoption of the AC approach allows to compensate the current flowing on the balanced mixer cell by means of an external suitable Positive Temperature Compensated (PTC) termistor without affecting the voltage DC levels of the output amplifier. In fact in the AC coupled solution the mixer stage is connected to the following by means of metal-insulator-metal Silicon Nitride (SiN) capacitors. The AC solution, differently to DC, includes a pre-driver RF output stage to recover a conversion gain degradation. Furthermore, a high impedance inter-stage matching has been adopted mainly to reduce the power consumption and the die area. The needs of high isolation between ports in the Up-converters can be achieved by means of balanced structures. The IF amplifier (Fig.3) is a gate coupled differential input amplifier driven by suitable current generator. The 50-ohm input matching is achieved setting the trasconductance g_m of the GaAsFET's J1 and J2 equal to 20 mS. An external balun transformer might be used to convert the single-ended IF signal into a differential mode. The IF amplifier gain shows the best trade off between Up-converter noise figure and intermodulation products. A doubly-balanced active mixer topology (Fig.4) has been implemented in these Up-converters for achieving enough linearity and carrier suppressions [2], critical parameters in this application. The g_m of transistors J6 and J7 sets the noise of the active mixer and their dimensions, together with the upper FET's and load and source resistors have been optimised to improve the overall performances. The source degeneration resistors in some differential pairs improve the spur suppression, even adding further noise sources. The use of an external PTC termistor is particularly suited to control better the current and gain Vs. temperature in the mixer. A broadband RF differential amplifier follows the analog multiplier. The

use of two stages (Fig.5 and Fig.6) in AC version improves the linearity and the CMRR (which is not ideal at these frequencies) of the amplifier [3]. In order to avoid intermodulation problems this amplifier should be extremely linear. In this context particular care has been taken of its voltage DC levels and currents. The amplifier also comprises the output buffer stages driving external 50-ohm impedance. The 1dB compression point was simulated at 8 dBm on 50 Ohm output impedance. Single ended or balanced RF output are available. Electrical simulations shows that even with single-ended LO injection, the isolation specs could be achieved. In order to limit the clamping effect both in AC and DC solutions, the level shifter stages contain parallel RC networks instead of diodes. Special care was taken in the design of temperature and foundry processes compensated current generators for the amplifier and multiplier stages [4]. The RF switches were designed as combination of assorbitive Single Pole Double Throw (SPDT) switch cells driven by proper TTL to Source-coupled FET logic (SFCL) converters [1]. During the computer simulation phase the TOM model has been used to predict the behaviour of active devices.

Package modelling

The need of several I/O analog and digital signals in both devices leads to the use of large packages that are not well suited at UHF frequencies. Large parasitic effects are associated with such packages and they could affect the performances of the devices in terms of port isolation, spurious and stability. A modelling of the chosen package has been achieved first, by means of a Microwave tool simulator and the available measurements, in order to be introduced later in the circuit design. A big effort was necessary to model the adopted 44 pins ceramic package and to obtain the equivalent circuit in terms of lumped elements (Fig.7) well suited for the PSPICE platforms.

Layout Considerations

The circuits have been manufactured using 1-um E and D-type MESFET process, precise Nichrome (NiCr) resistors, SiN capacitors, two metal layers, no via-holes. The layouts were carried out with special care for the parasitic couplings between I/O ports. The GNDs of IF amplifier, mixer and RF out amplifier are kept separate on die, in order to have no intersections between input and output ground currents. Further GND lines were drawn to reduce line-line interactions. The on die parasitics were extracted and included in the original electric diagrams. Before the definitive layouts were delivered to the foundry, postlayout simulations were accurately carried on to minimise the effect of the parasitics. The photograph of the internally AC coupled UP-converter housed in its 44-pin package is shown in Fig.8.

Performance

10 prototypes for each device have been tested and all the performance have been found in specs for the UP-converter internally AC coupled. The DC internally coupled UP-converter produces higher in-band spurs (figures 9, 10 and 11) compared with the AC solution. The spurious simulation results are not presented because the numerical noise, together with the available non-linear models implemented on PSPICE, do not allow to achieve the needed accuracy for the comparison between simulated and measured in-band spurious. The figure 12 shows the conversion gain variation as a function of the termistor (ADJ resistance) connected to the Curr-Adj node (Fig.4) of the mixer. The output power of the converted signal is shown in Fig.13. As far as the scattering parameters are concerned, the DC and AC coupled solutions show the same results. Simulated and measured reflection coefficients are plotted respectively in Fig.14 and Fig.15

Conclusions

The development of two L-Band UPC's has been described. The performance of both devices has been found very close to the simulations, proving a high degree of reliability of the foundry libraries and of the package modelling. The AC internally coupled UP-converter is to be preferred to DC coupled solution in terms of spurious, when an external PTC termistor is used as current controller for the doubly-balanced GaAsFET mixer.

References

[1] Stephen I.Long, Steven E.Butner *Gallium Arsenide Digital Integrated Circuit Design* Mc Graw Hill ,1990.

[2] Barrie Gilbert "*A high-performance monolithic multiplier using active feeback*" IEEE J. Solid-State Circuit Vol. Sc-9, pp 364-373, Dec. 1974

[3] A.Boveda, F.Ortigoso, J.I.Alonso "*A 0.7-3GHz GaAs QPSK/QAM direct modulator*" IEEE J. Solid-State Circuit Vol. 28, pp 1340-1349, Dec. 1993

[4] C.Toumazou, F.J.Lidgey & D.G.Haigh *Analogue IC design : the current mode approach* Peter Peregrinus Ltd on behalf of the IEE ,1990.

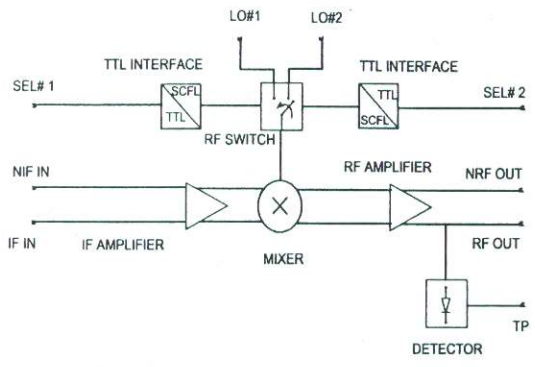

Figure 1- Block diagram of the DC internally coupled Up-converter

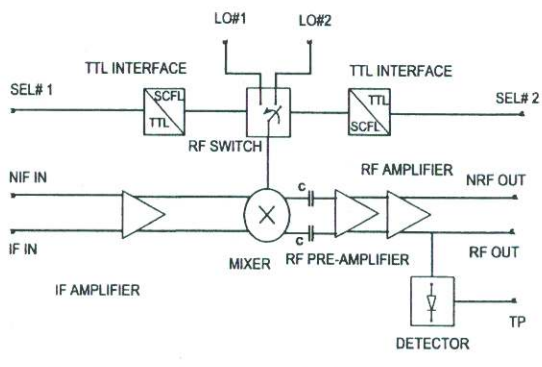

Figure 2- Block diagram of the AC internally coupled Up-converter

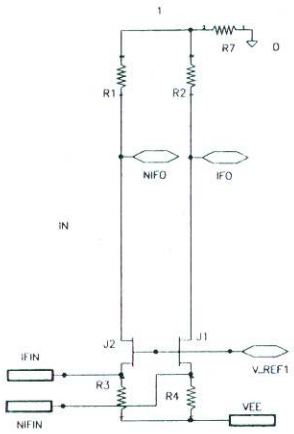

Fig. 3 – IF input amplifier

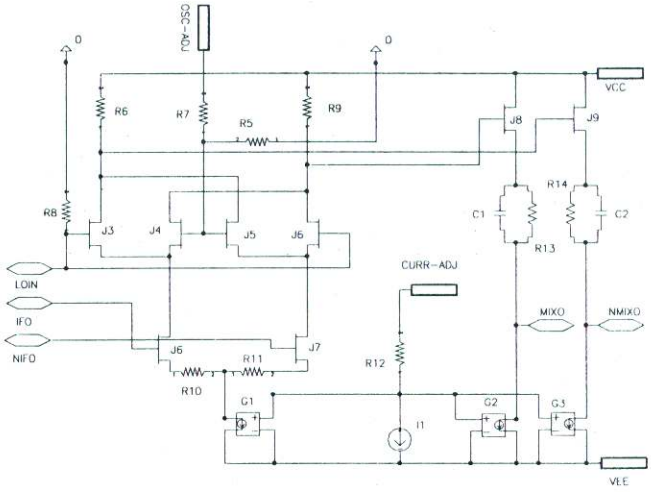

Fig. 4 – Doubly-balanced GaAsFET Mixer

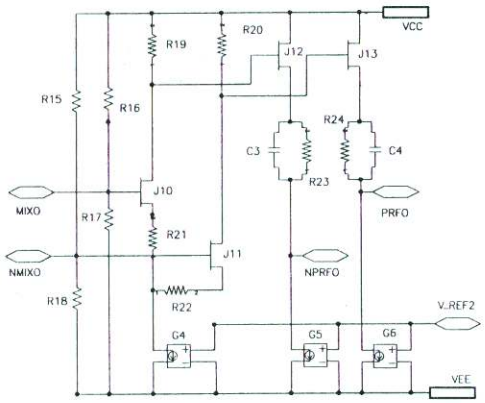

Fig. 5 – RF pre-amplifier

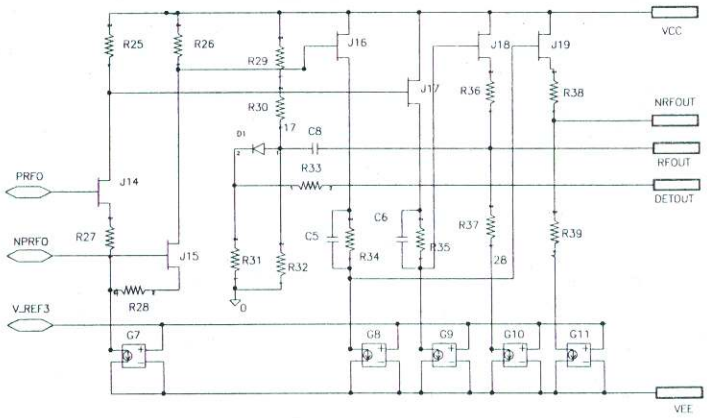

Fig. 6 – RF output amplifier and detector

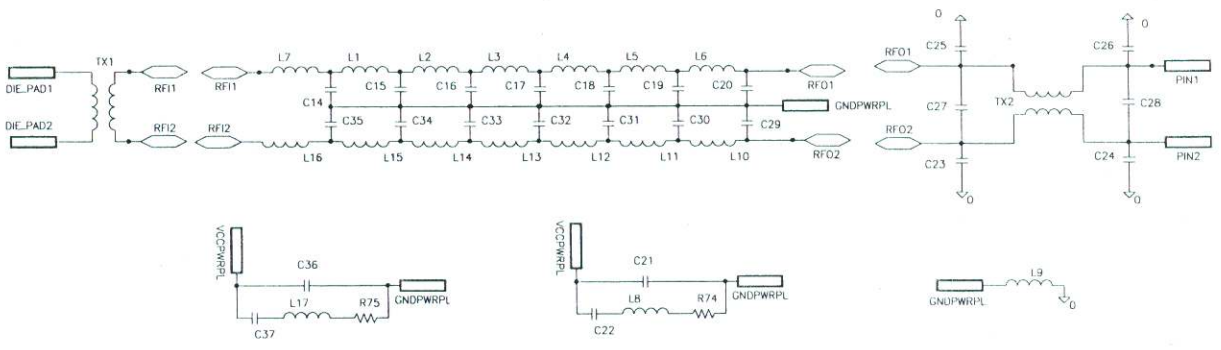

Fig. 7 – Lumped equivalent model of package adjacent pins and power planes

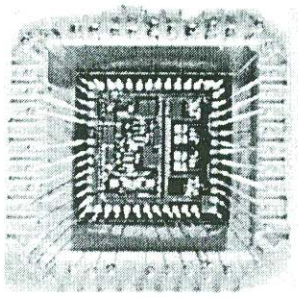

Figure 8- Photograph of the 3x3 mm^2 GaAsFET Up-converter housed in the 44-pin package

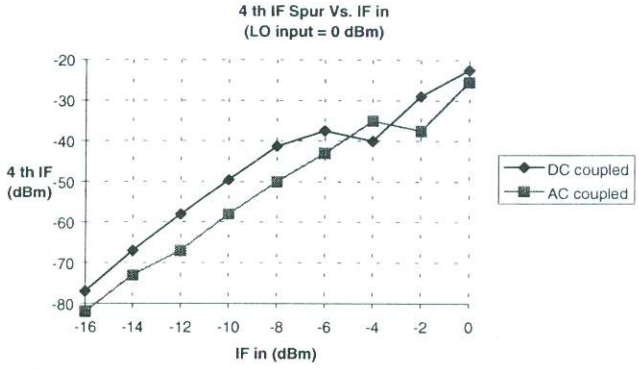

Figure 9- 4th-harmonic output spurs for the AC and DC internally coupled Up-converters

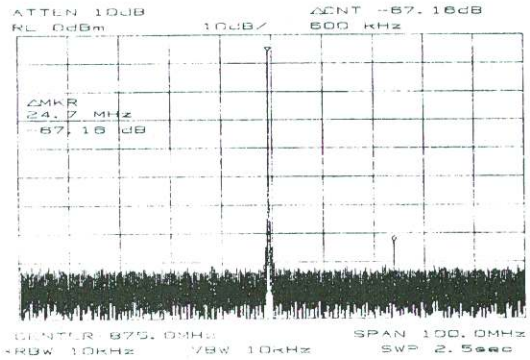

Figure 30- Converted signal and 4th-harmonic spur for the DC internally coupled solution

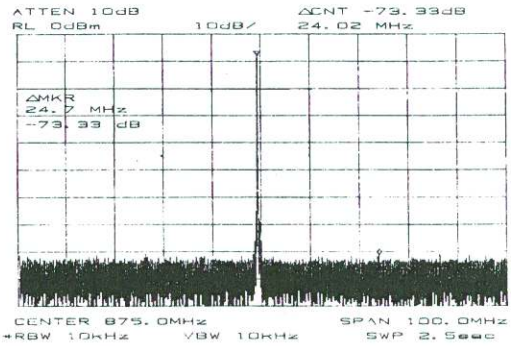

Figure 11- Converted signal and 4th-harmonic spur for the AC internally coupled solution

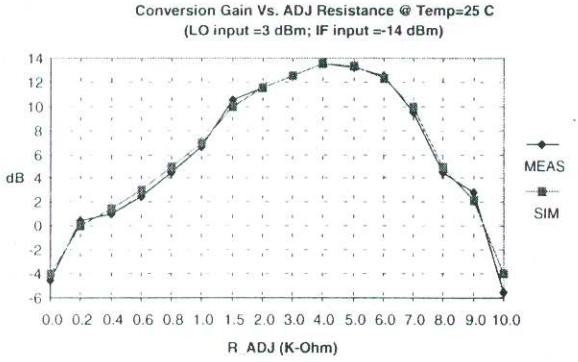

Figure 12- Measured and simulated conversion gain for the AC internally coupled Up-converter

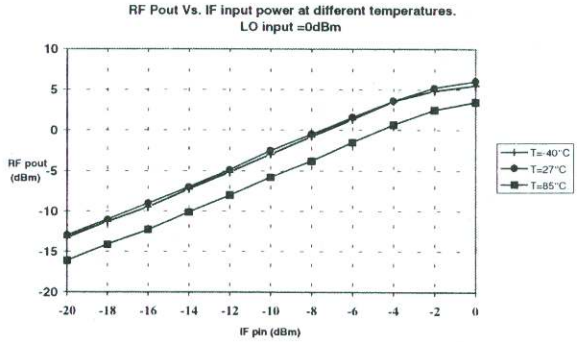

Figure-13 Output power of the upconverted signal at different temperatures (-40 C, 27 C, 85 C)

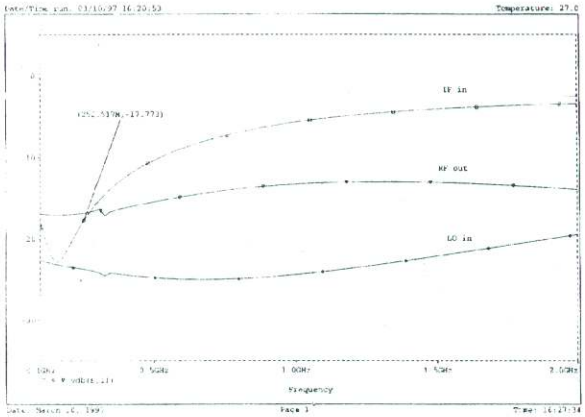

Figure 14- Magnitude of simulated reflection coefficients at IF in, LO in and RF out ports

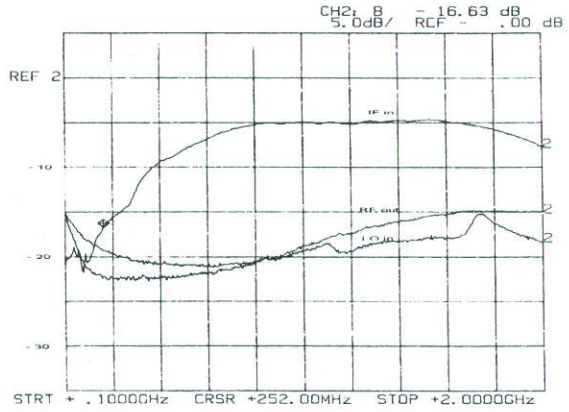

Figure 15- Magnitude of measured reflection coefficients at IF in, LO in and RF out ports