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GaAs MESFET SRAM using a New High Speed Memory Cell

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Abstract

This paper presents an experimental 1kb GaAs MESFET static RAM using a novel high speed memory cell. The array overcomes the subthreshold leakage currents drawbacks inherent to conventional cell using a particular word/bit lines biasing. Power consumption is reduced by powering down the parts of the array not selected. An address access time of 1ns with 20 µA/cell power consumption has been obtained. The RAM can be operated at the single supply voltage of 1V up to 2V.

1. Introduction

Low power GaAs LSI technology is becoming an important and growing area of electronics. In particular, low power SRAM is an area of this technology in which considerable attention has been focused. Much effort has been dedicated to the development of GaAs SRAMs and some important progress in power reduction, performance and temperature tolerance have been obtained [1][2]. Currently, several high-speed on-line GaAs memories are being designed to be applied to high-speed GaAs microprocessors [3][4], which use small amount of memory on-chip in order to exploit the hierarchical high-speed memory benefits.

Commonly, six transistors conventional memory cell has been used to implement static RAM, but this cell presents important limitations to implement GaAs SRAM structures. As can be seen from figure 1, there are some problems in using conventional cell. First one, when the word line level is "high", the low and high nodes of the cell become capacitevely coupled to the bit lines (i). Secondly, current is also injected into the cell through the gate-source diode of the access transistor (ii), causing one of the more important mechanism that can generate destructive readout which is itself an strong yield limiting factor for GaAs SRAMs.

MESFET leakage current flows at only the "low" node, from the bit line in non selected cells, then the number of memory cells and the combination of the stored data in each column define the sum of the leakage currents per bit line and not only the leakage currents in the individual access transistor (iii). Additionaly, a reduction of the "high" internal node level can be caused by the increase both of the drain to source leakage current in the driver enhancement FET and of the Schottky current from the gate to the source in the driver enhancement FET in the succeding stage (iv). If exist a temperature variation, the bit-line potential, a stability of the memory cell and in consequence the circuit operation of GaAs SRAM are strongly affected by the leakage current increment in the access transistors of memory cells.

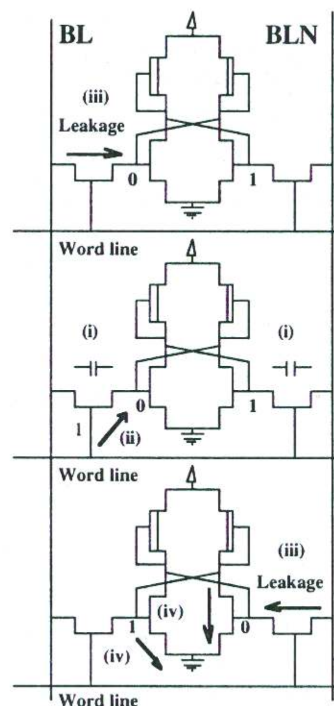

Figure 1. Conventional memory cell limitations.

Several solutions have proposed as diode or ground shifting techniques [1][5][6][7], in order to limit the leakage currents. Other have applied built-in redundancy [8] or current mirror [9][10] techniques to GaAs SRAM [3], but additional control logic or several voltage levels are required increasing the complexity and the access time.

In this paper the circuit design of 1 Kb SRAM based on a novel high-speed cell is presented. A good performance and operational margin over a wide temperature range are its principal features. The cell structure and its operation are briefly discussed. The final layout of 1 KB SRAM and simulation results are presented. The 1 Kb SRAM can be used in high speed systems with sub 2 ns on-line memories requirements. The circuit is currently in fabrication.

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2. Memory cell design

The schematic of the high-speed new cell is shown in Figure 2. Source-gate back biasing in the depletion transistors *M1* and *M2* are used as sub threshold current reduction circuit in order to reduce the power dissipation of the cell. The back biasing is obtained using *D1* and *D2* diodes. The depletion transistor and diode combination acts as a weak pullup current supply and must be designed considering the pullup time requirements, power reduction and the necessary current to compensate both the sub-threshold leakage and Schottky currents through the enhancement devices in order to keep the high level in the respective node [11]. The latch formed by the cross-coupled transistors *M3* and *M4*, provides a robust storage element with reduced static power dissipation. Transistor *M5* acts as one write-only port, while transistor *M6* acts as read-only port.

The operation of the cell is straightforward. The read and write cycles occur on oposite phases of a system clock. The write cycle begin on the rising edge of the clock and the read cycle on the falling edge. The cell is read by pulling down the read word line which is maintained at 1V before the read cycle. The word line for selected row is lowered to 0v, while the word lines of the remaining non selected rows are held at 1v.

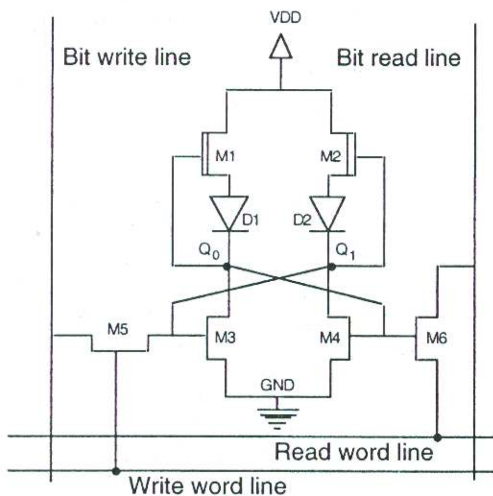


Figure 2. New cell diagram

In this configuration the gate-drain and gate-source diodes of the access transistors of non selected cells are reversed biased an appear as additional capacitances to the storage node overcoming the mentioned conventional cell problem. Additionaly, the access transistor of the selected cell cannot inject current into the storage nodes causing a nondestructive read operation.

If the cell stores a high value at the internal node Q_0 and the read word line is lowered to 0v, a saturation current flows through *M6* transistor pulling down the bit read line which must be precharged at 1v before each read operation. If the cell stores a low value at Q_0 , not significant currents appear through access transistor and the precharged bit line value is held.

The write operation is similar to that in a conventional six-transistor cell , data is placed on the bit write line and the write word line is raised, the cross-coupled transistors force the internal nodes to change to appropriated voltage levels maintaning the state of the cell. In order to obtain a high speed write operation, the access transistor *M5* must be dimensioned respect to *M3* pull down transistor. Usually, a ratio of *M3* = *3M5* is required.

To write a low level, the low voltage bit line is connected through the *M5* pass transistors to a cell storage node pulling it low and causing the opposite cell storage node to be driven high. To write a high level it must be guarantee that ,$V_G \geq Vi + V_{TH}$ if $V_{BL} > Vi$, where V_G is a gate voltage of access tarnsistor, V_{BL} is a bitline voltage level and V_{TH} is the threshold voltage, Vi would be the internal storage node. Using the mentioned voltage levels the write operation is reliable.

Unlike the reported full mirror cell, no multiple diodes are present in writing process, the cell ground does not have be driven causing that less control circuitery would be required. In this new cell, only a single voltage of 1v up to 2v is required. The memory cell designed presents good stability and access speed. A noise margins of 200 mv were obtained.

3. Basic circuit

To analyse the stability of the memory cell HSPICE simulations were carried out . The circuit includes a memory array, the bit line precharge scheme, I/O circuitery and the sense amplifier. Figure 3 shows the 1kb RAM block diagram.

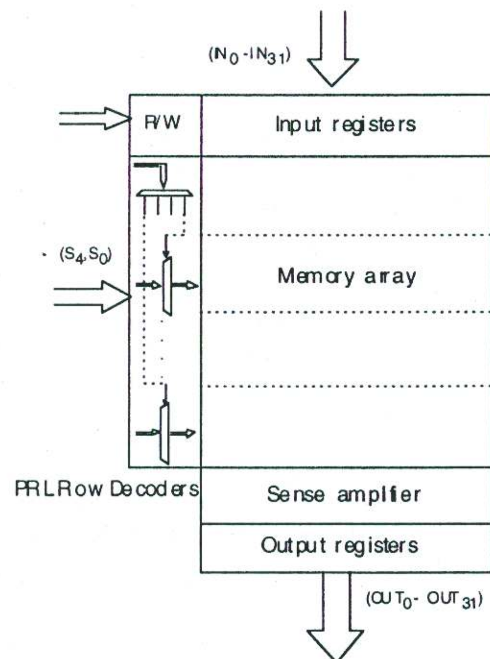


Figure 3. Block Diagram

The delay time from the address input to the word line is called word-line selection time and is reponsible for a large part of the access time. In order to reduce this

selection time the following method was applied for the row selection circuit. A 1KB memory array is divided in four 8x32 blocks and the address signals are categorized into two groups. The firts group (S_4, S_3), is used for block selection while the second group (S_2, S_1, S_0) is used for row selection.

A hierarchical block decoding method uses PRL decoders in order to reduce their power dissipation, when one block has been selected, the remaining three row decoders are disactivated because of their power rail control lines are brought down to ground, forcing their outputs low.

Because is a technological requirement to reduce the word line RC delay and the array current for prevening the lowering of the high level, using this method a significant reduction in both delay time and power consumption are achieved.

As the temperature increases, the high level rapidly lowers by the parasitic Schottky diodes in the decoder circuit. So, the operational margin for the temperature is also improved by this power rail decoding method. To reduce the transient time of the data line signal in *read* operation, column sense amplifiers were used in each column.

The output stage consists of a register that regenerates and stores the output sense amplifier voltage levels, providing a good fanout and noise margin characteristics. The register limit the output high voltage at 0.7V to satisfy the input voltage requirements of the next circuitery.

4. Sense amplifier

A PRL [12] sense amplifier to achieve lower consumption during no reading operation is proposed. The sense amplifier shown in Fig. 4, consists of a SBFL inverter and two cross-coupled PRL NOR gates. When a read operation is started, the read signal is buffered through the SBFL inverter supplying the power rail of NOR SR latch.

The two cross-coupled transistors *M4* and *M5* avoid charge leakage on the uncharged internal node. This scheme provide a positive feedback which allow to switch fastly when a small voltage differences are sensed between the output nodes.

Direct and complementary bit read line signals are connected to *M6* and *M3* MESFETs respectively. Since only a single read bit line is required for each memory cell, an inverter is used with the PRL NOR cross-coupled amplifier to generate the complementary signal for the sense operation.

The internal voltage levels are after buffered by the push-pull output driver of the sense amplifier offering a suitable fanout capacity, permiting operate at the maximum gain point and furnishing the appropriated voltage levels.

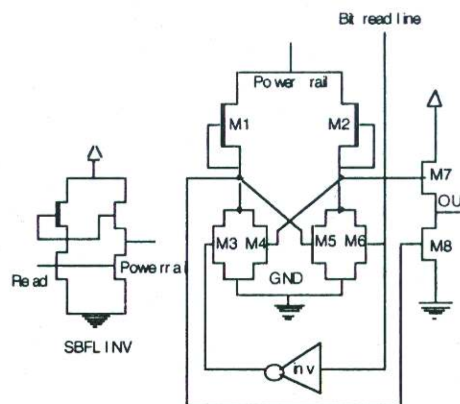


Figure 4. PRL sense amplifier

5. Simulation results

From simulation results the total cell read/write access times were found to be 760 ps and 150 ps respectively. An active current of 20 µA (at 1Ghz) was obtained. The memory array accommodates 32 cells in a single column. The column circuitry of this SRAM include input/output registers and sense amplifiers.

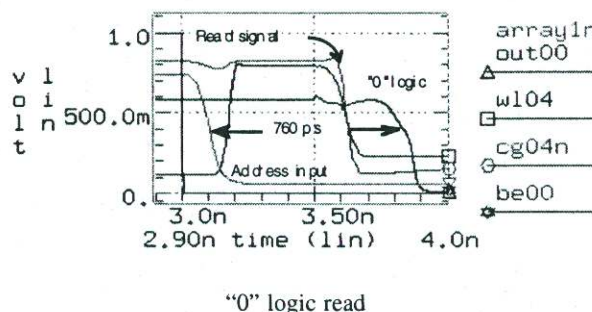
The total power dissipation of the 1 Kb core memory array operated at 1v is 20.5 mW. A global access time of 1 ns was measured from the input to the output buffers. The read access time is longer than the write access time because of the regeneration process necessary to magnify the small bit line voltage difference to full voltage swing.

In table I, a comparison between the new cell and some of the reported cells is presented.

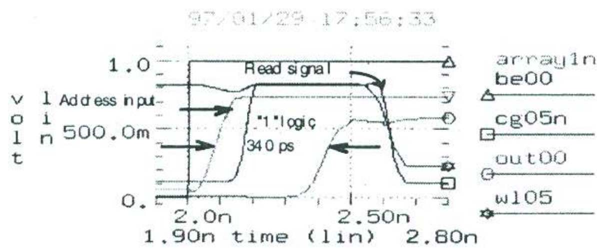
Table I. Memory Cells Comparison

Cell	SRAM	Access	Tech.	Power	Size
Mak [1]	4 KB	7 ns	1.0 µm	0.85 W	35x29
Cha [3]	1 KB	2.3 ns	0.6 µm	0.8 W	18x20
Fie [4]	4 KB	3.6ns	1.0 µm	1.9 W	------
Mat [5]	16 KB	5 ns	0.7 µm	2 W	36x23
Mat [6]	16 KB	7 ns	0.7 µm	2.1 W	36x23
Law [7]	1 KB	2.5 ns	1.0 µm	0.5 W	26x31
Tse [8]	16 KB	7.5 ns	------	1 W	33x34
Ber [11]	1 KB	1ns	0.6 µm	0.15 W	36x37

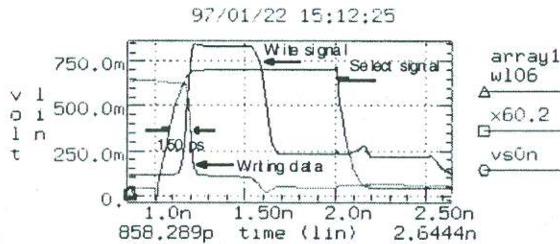
In figure 5, the address input and data output wave form for a read and write cycle of the memory cell are shown. In figure 6, 1 Kb chip layout is presented.



"0" logic read



"1" logic read



Write operation

Figure 5 Read/Write operations - Wave forms

6. Conclusion

A novel memory cell structure has been developed to implement static RAM in GaAs technology. The new cell present low power dissipation and high operating speed. The RAM was designed and currently fabricated using Vitesse III - GaAs technology.

By the improvement of the structure an address access time of 1ns with a core power dissipation of 20mW has been obtained. The RAM operates at only supply voltage of 1v up to 2V. This RAM can be easily used in implementing high-speed cache memory.

7. Acknowledgement

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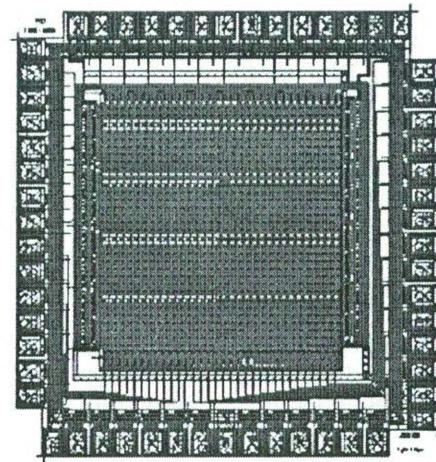

Figure 6. Chip layout

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