

Decoding and Decision Circuits for High Speed Multi-Level Transmission

Ph. André*, M. Meghelli, P. Desrousseaux, A. Konczykowska, J. Godin
 France Telecom-CNET, DTD - BAG/CBO, 196 av. Henri-Ravera - BP 107 - 92 225 BAGNEUX Cedex,
 fax : + 33 1 01 47 46 04 17, *e-mail : philippe.andre@bagneux.cnet.fr

Abstract: High speed decoding and decision ICs for 4-level ETDM fibre optic transmission systems are presented. The circuits were fabricated in a InP/InGaAs HBT technology with $F_t = 53$ GHz and $F_{max} = 40$ GHz. A 4-level decoding circuit using a mux core architecture and a binary decision circuit were designed and measured. The potential performance of the decoder were experimentally assessed up to 16 GBaud (32 Gbit/s) (input data). The decision circuit is a D MSFF which was tested up to 22 Gbit/s.

Introduction

Multi-level versus binary modulation format

Telecommunication research laboratories are working intensively to demonstrate the feasibility of ETDM fibre-optics systems up to 40 Gbit/s. For achieving this ambitious objective, it is necessary to improve frequency performance of devices; this has a cost and implies important technological effort. This difficulty can be overcome by the use of a higher level modulation format than the usual binary one. The 4-level modulation format appears to be one of the most interesting in terms of reliability, effort and benefit [1]. The major advantage is that, for an equivalent bit rate, the clock frequency of the

4-level decoding and decision

The figure 1 and the truth table of the figure 2 give the principle of 4-level coding and decoding. At the emission end the two 20 Gbit/s binary data streams D1 and D2 are combined to generate a 20 GBaud (40 Gbit/s) 4-level data stream. The decoding operation consists, in a first step, in detecting A, B and C using threshold detectors. As D1 equals B (fig. 2), one can get directly D1 with B. To obtain D2 it is necessary to combine A, B and C. Several architectures have been studied. We have selected one of the sturdiest solutions able to deal with high bit rates and proposed in [1, 2]. To decode D2 we use a mux core, we multiplex A and C using B as a clock. When B equals 1 the output is A; when B equals 0, the output is C. To keep an equivalent delay between the 2 paths it is possible to regenerate D1 by the same way, just inverting the connection of B to the mux clock input (figure 3). The decision operation consists in synchronising data and is carried out, after decoding, using an MSDFF circuit on each data stream.

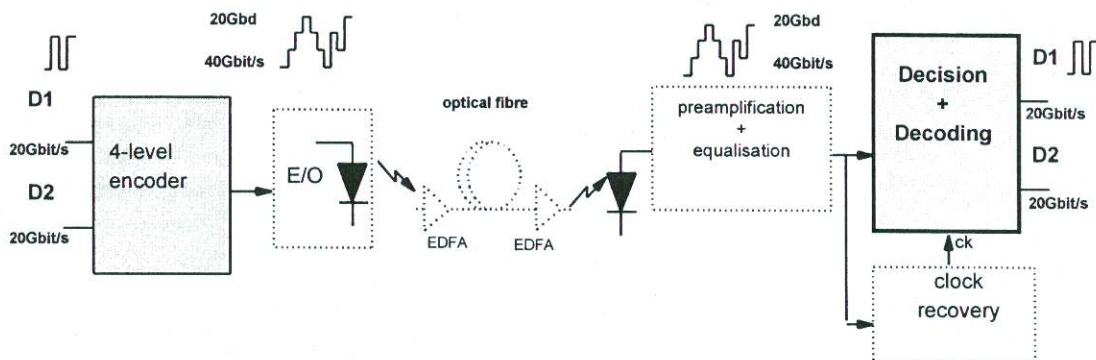


Figure 1 : block diagram of the 4-level fibre-optic transmission system

4-level transmission system can be reduced by two compared with the binary case. As a consequence, the technological requirements and the circuit layout design are somehow relaxed.

Figure 1 shows the block diagram of the 4-level ETDM fibre-optic communication system with the following specific circuits: at the transmitting end, an encoder circuit carries out data multilevel coding and multiplexing and at the receiving end, decoding and reshaping circuits restore the two binary data streams. We have focused our work essentially on the decoding and decision aspect of the system.

D1	D2	D	A	B	C
0	0	0	0	0	0
0	1	1	1	0	0
1	0	2	1	1	0
1	1	3	1	1	1

Figure 2 : truth table of the 4-level coding and decoding

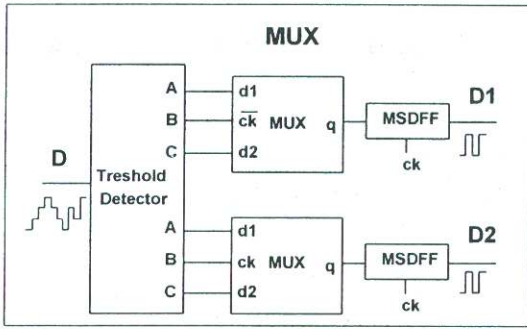


Figure 3 : block diagram of the decoding and decision circuit using the mux architecture.

Technology

The technology implemented and developed at Bagneux-CNET laboratory is based on InP / InGaAs HBT devices [3]. It is a non-self-aligned triple mesa technology. It includes two level Ti/Au interconnects, thin film resistors and MIM capacitors. The Emitter-Base area of the transistors used is $3 \times 8 \mu\text{m}^2$. The DC current gain is typically about 90 at a current density of 40 kA/cm^2 with $F_t = 53 \text{ GHz}$ and $F_{\text{max}} = 40 \text{ GHz}$ for a collector-emitter voltage $V_{\text{ce}} = 2\text{V}$. The breakdown voltage BV_{ce0} is about 15 V.

Design

The objective was to design decoding and decision circuits able to operate up to 20 GBaud. Emitter Emitter Coupled Logic (E²CL) was used and special care was taken in the circuit implementation to minimise parasitic effects and to exploit, in an optimal way, the potentialities of our technology in terms of bit rate. Then, as illustrated by the figure 7 and 11, the layouts were designed in a symmetrical and compact way [4] in order to keep a synchronous propagation between the data and their complementary on each path and to reduce crosstalk and common mode. 50Ω coplanar acces associated with on-chip 50Ω resistors are used on the input to reduce

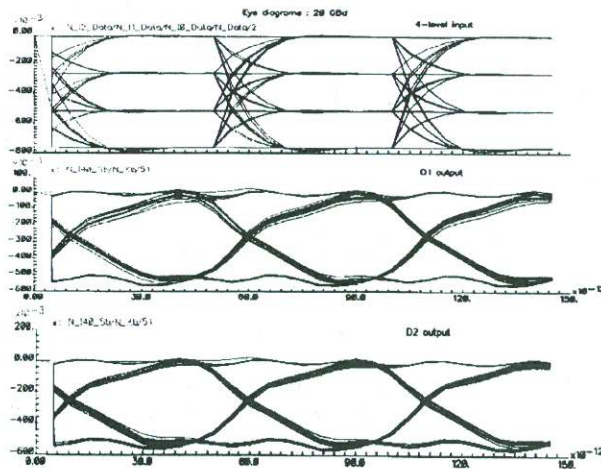


Figure 4 : D1 and D2 decoding : simulated eye diagram at 20 GBd

distortions introduced by multiple reflections and achieve a good matching.

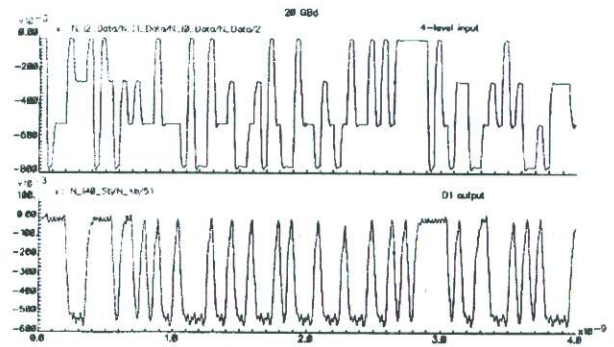


Figure 5 : D1 decoding : simulated waveform at 20 GBd

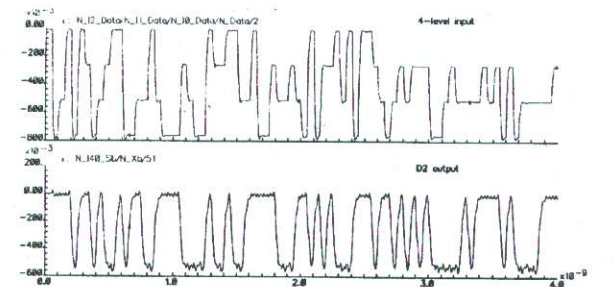


Figure 6 : D2 decoding : simulated waveform at 20 GBd

The two decoding circuits (D1 and D2) have been simulated with the decision circuit at a bit rate of 20 GBaud (figures 4-6) with perfectly opened eye diagrams. The MSDFF reduces time jitter and removes efficiently the glitches which can be introduced by the selector (MUX).

Experimental Results

On-wafer high speed measurements of the integrated circuits were done on-wafer using Cascade Microtech DC probes and Picoprobe microwave probes. A 12.5 Gbit/s Anritsu pattern generator was used with an external 20 Gbit/s multiplexer to obtain measurements up to 20 GBaud.

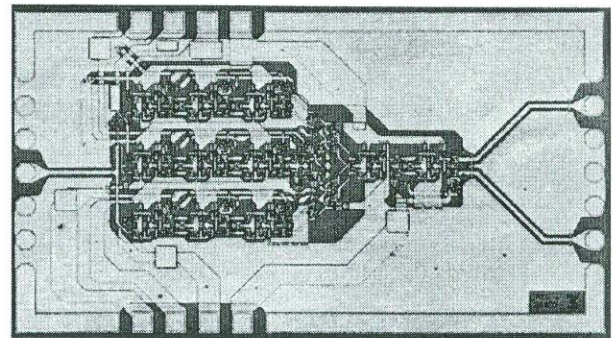


Figure 7 : photograph of the D2 decoding circuit ($1450 \times 2650 \mu\text{m}^2$)

Figure 7 shows the photograph of the D2 decoding circuit. Having no 4-level pattern source available at this

time, the performance assessment of the 4-level decoder was done with the help of a binary test procedure. The principle of this procedure is illustrated by the figure 8. Using a classical binary source (Anritsu generator) coupled with an external multiplexer, we have measured the response of our circuit for each one of the multilevel input signal transitions. An output signal at 20 Gbit/s was measured for each transition on the D1 decoder (Figure 9). On the D2 decoder the 3-1 and 2-0 transitions have shown important perturbations (glitches) limiting the output bit rate at 16 Gbit/s. Already at this bit rate, glitches appear, in particular on the 2-0 transition (Figure 10). This bit rate was obtained with an output voltage swing of about 300 mV and using respectively, to detect A, B and C (figure 2 and 3), the reference voltages Vr1 = -200mV, Vr2 = -400 mV and Vr3 = -600 mV.

According to these results one can think that the mux core decoder can potentially operate up to 16 GBaud (32Gbit/s) (4-level input data). These results must be confirmed by multilevel measurements in order to show if binary test is significant to assess the performance of such a kind of circuit. Indeed, in the binary test case, the measurement done for one transition is decorrelated from the others. In the 4-level test case each transition depend on the previous ones. That can increase the time jitter and the glitch phenomenon and deteriorate bit rate performance. On the other hand A, B and C detected data must be perfectly timed when apply to the mux core in order to reduce that kind of deterioration.

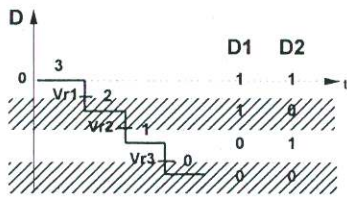


Figure 8 : binary test procedure illustration

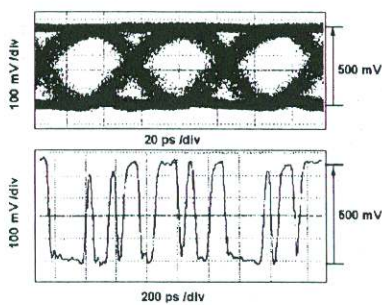


Figure 9 : D1 decoder output measured at 20 Gbit/s (transition 2-1)

Then, it is particularly important to use flip flop in order to retime decoded data, decrease jitter and remove residual glitches. Figure 11 shows the photograph of the decision circuit (D MSFF) which will be used after decoding. This circuit, packaged, was tested at a bit rate of 22 Gbit/s (2^{15} -1 PRBS) and with a single-ended output voltage swing of about 600 mV across 50 Ω . The figure 12 displays the eye diagram and the waveform obtained

at this bit rate. The measured clock phase margin is 180°. The performance of this circuit is adequate to retime the D1 or D2 data extracted from the decoder.

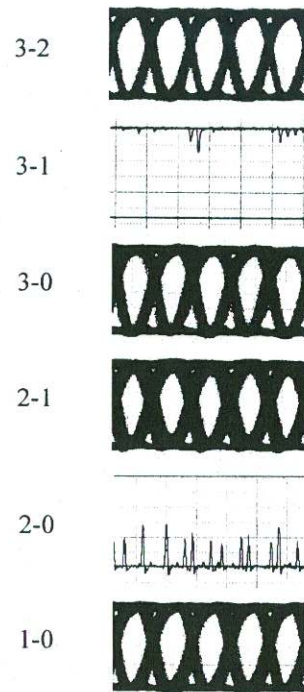


Figure 10 : measurement results obtained on the D2 decoder output at 16 Gbit/s corresponding to a 16 Gbaud (32 Gbit/s) decoder potential working (single ended voltage swing : 300 mV)

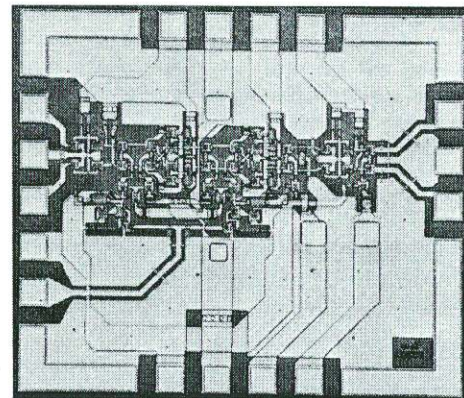


Figure 11 : photograph of the décision circuit (1450x1450 μm^2)

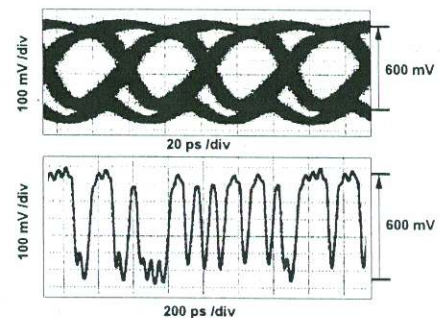


Figure 12 : D-MSFF circuit eye diagram and waveform at 22 Gbit/s

Conclusion

Multi-level modulation appears to be a promising alternative to the classical binary transmission for reaching high bit rate. The realisation of a 4-level ETDM transmission demonstrator is one of the purposes of the European project ACTS SPEED to demonstrate the interest of the multi-level approach. In this contribution, we present the first results obtained with 4-level decoding circuits and a binary decision circuit realised in InGaAs/InP HBT technology. Decoding circuits using a mux core architecture and a decision circuit were designed and measured. The potential performance of the 4-level decoder were experimentally assessed up to 16 GBaud (32 Gbit/s) (input data) using binary test procedure. The binary decision circuit was tested up to 22 Gbit/s. We hope than 4-level measurements will allow to confirm these results.

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