A 3.2 W Coplanar Single-Device X-Band Amplifier with GaAs HBT

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***Abstract*— High-power GaInP/GaAs HBTs with high breakdown voltage for X-Band applications are presented. To demonstrate the capabilities of these devices, a simple monolithic amplifier is realized. For a single 12-finger device with 2x70 μm^2 emitter finger size, an output power of 3.2 W at 9 GHz with 47% PAE is achieved.**

***Index Terms*— Heterojunction bipolar transistors, MMIC power amplifiers.**

High-power X-band amplifiers have been a topic of great interest over the last years, most of them based on GaAs HEMT MMICs. More recently, two further transistor technologies have entered this application field: the GaAs HBT and the GaN HFET. For GaN HFETs, mostly realized on SiC substrates, the large band-gap in conjunction with high electron mobility and good thermal properties are the key features for high power. However, costs of this technology are still high and reliability is not yet clarified. The second new contender for high power in this frequency range is the GaInP/GaAs high-voltage HBT. This device benefits from the mature material and processing technologies as well as the proven performance for related HBT devices. Increasing the collector thickness allows operating GaInP/GaAs power HBTs at higher bias voltage, which brings output impedance closer to 50 ohms. This technology has been established for S-band applications such as base-station amplifiers recently [1], [2].

However, gain of these devices is still too low to reach X-band frequencies. But situation can be improved by trading breakdown voltage against transit frequency. The results are presented in this paper. A careful epi-layer structure design yields a compromise between power and gain performance of the device in X band. A second important aspect is thermal management. In contrast to SiC-based GaN, the GaAs substrate itself has a low thermal conductivity. Hence, for the GaInP/GaAs HBT, a flip-chip assembly is employed.

In this paper, we report on optimization of such HBT power cells and their application in an X-band power amplifier. Two layout variants with different emitter geometries are studied in order to identify the transistor version most suitable. Based on this, a single-device one-stage amplifier is designed, fabricated, and measured. It achieves a maximum output power of 3.2 W at 9 GHz at 9 dB of linear gain. This proves the capabilities of our devices for high power applications at X-band frequencies.

I. Device Technology

Device technology is based on our established high-voltage HBT (HV-HBTs) process, which allows operation at bias voltages up to 28 V [3]. These HBT power cells achieve high output power (10+ W for 4000μm devices) with efficiencies of up to 70% at near-class-B operation at 2 GHz. In order to extend the frequency range of these power HBTs to X band, the HBT layer structure and processing details had to be optimized accordingly.

The HBT structures are grown in-house on 100 mm GaAs substrates in an Aixtron AIX2400 PlanetaryTM MOVPE reactor. The epitaxial layer structures mainly consist of a 700 nm GaAs subcollector layer (n=5x10^{18}cm^{-3}), an up to 1000 nm thick GaAs collector layer (n-doped in a region of 2x10^{16}cm^{-3}), a 100 nm GaAs base layer (p=4x10^{19}cm^{-3}), a 30 nm $Ga_{0.51}In_{0.49}P$ emitter layer (n=5x10^{17}cm^{-3}), and GaAs and InGaAs contact layers. Si and C are used for the n-type and p-type doping, respectively. Special high-resistance layers are included in the emitter layer as a ballasting resistor. This prevents thermal runaway and improves electrical and thermal stability of the device. Epitaxial design and processing is chosen such that breakdown voltage BV_{CB0} reaches 24 V, which provides enough margin for safe operation in the 9...10 V bias range.

The HBT process is based on a two-mesa approach in order to access the base and the collector layers. Double implantation is used for device isolation as well as for reduction of the external base-collector capacitance, thus improving the high frequency performance of the device. Using this technology record values of transit frequencies were achieved [4]: f_T of 45 GHz and f_{max} of 200 GHz. Interconnections are made by Ti/Pt/Au metal and emitter thermal shunts are formed by a 20 μm thick electroplated Au layer which is well visible in Fig. 1 and 2. HBT power cells with up to 16 emitter fingers and a total emitter area of up to 3600 μm^2 have been fabricated.

As for the S-band HV-HBTs, we use our proprietary flip-chip soldering process on patterned AlN or diamond submounts for low thermal resistance mounting of these power devices [1]. This large-area flip-chip soldering proved to be suitable not only for discrete devices but also for MMICs. Thus, work is in progress for flip-chip mounting of monolithic PAs such as the one presented in Sec. III.

II. Device Optimization and Measurements

To select the optimum device for the amplifier, small and large signal measurements were performed on devices of different size and layout. Two layout configurations were compared, a fishbone type (see Fig. 1) and a MESFET-like parallel-in-line layout (see Fig. 2), which is referred to as the parallel type in the following. We investigated devices with 4, 8, and 12 emitter fingers and single-finger emitter areas of 2x70 μm^2, 2x100 μm^2, and 2x150 μm^2. For L-band applications, the fishbone-layout is popular due to its good thermal behavior. For X-band applications, however, the parallel-in-line layout turned out to be superior. It has a smaller periphery as well as smaller parasitics, which yields a higher maximum frequency of oscillation (f_{max}) and consequently higher gain (MAG) at X-band.

Fig. 3 presents the behavior of f_{max} as a function of total emitter area for the different configurations under investigation. Clearly, f_{max} for the parallel layout is always higher than for the corresponding fishbone type transistor. As can be expected, the maximum available gain MAG shows the same characteristics. With increasing emitter area, it decreases from about 15 dB to 8 dB for the largest devices (at 10 GHz). Also, the input reflection coefficient $|S_{11}|$ of the parallel layout transistors is slightly lower in magnitude than for the fishbone type (see Fig. 4). This is in favor of the parallel type as well because input impedance is very low and a reduction in $|S_{11}|$ makes matching easier.

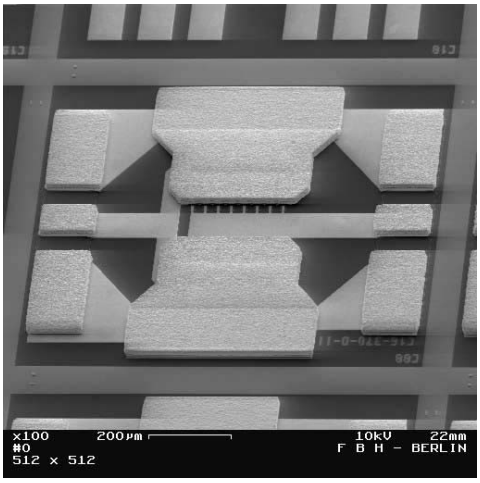

Fig. 1. SEM image of a typical HBT power cell (fishbone configuration).

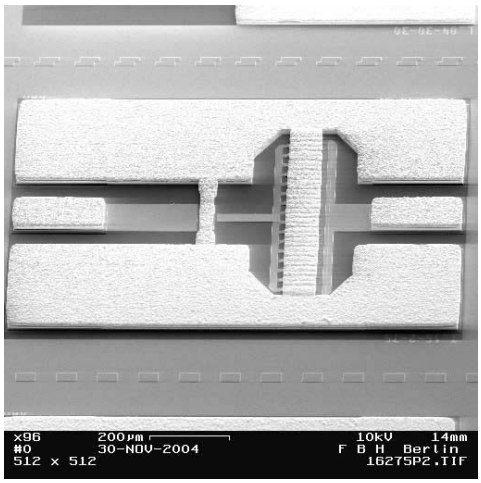

Fig. 2. SEM image of a typical HBT power cell (parallel-inline configuration with prematching).

Output power measurements indicated the same preference for the parallel layout. Also, the load-pull measurements revealed that a total emitter area of about 1600 μm^2 is sufficient to achieve an output power of at least 2 W at $U_{CE} = 9$ V bias voltage. Based on these results, a 12 finger transistor with 2x70 μm^2 emitter area in parallel-layout was chosen for the amplifier.

III. Amplifier Design

In order to focus on the transistor properties, a relatively simple amplifier topology was used. The amplifier is realized as a coplanar MMIC. Fig. 5 presents the chip photo.

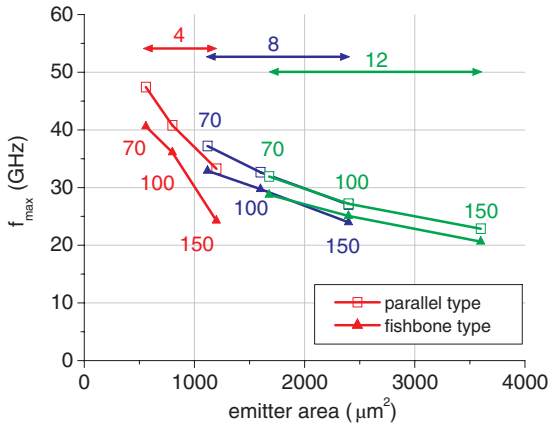

Fig. 3. Maximum frequency of oscillation (f_{max}) of X-band HBT power cells with different emitter geometries: fishbone type (triangles) and parallel type (rectangles) with 4, 8, 12 emitter fingers and 70, 100, 150 μm finger length.

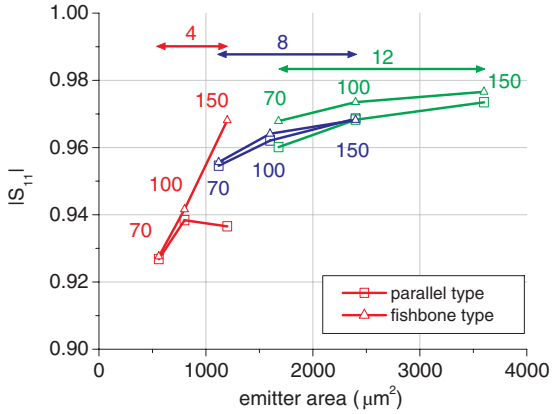

Fig. 4. Input reflection coefficient as a function of emitter area for the different HBT geometries: fishbone type (triangles) and parallel type (rectangles) with 4, 8, 12 emitter fingers and 70, 100, 150 μm finger length.

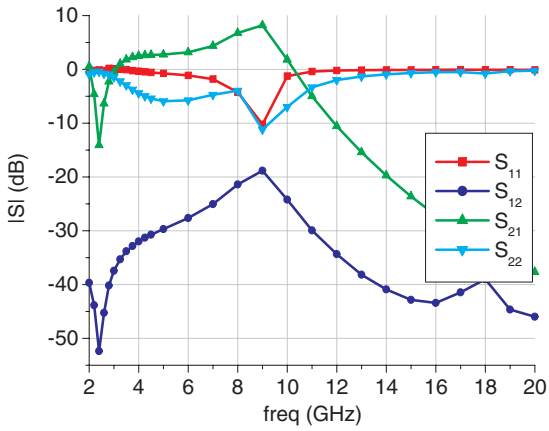

Fig. 6. Small signal S-parameter measurements of the 9 GHz amplifier.

Coplanar lines with a ground-to-ground spacing of 175 μm and a line width of 70 μm were used. This allows for a low-loss transformation to 50 Ω as well as provides sufficient cross-sectional area to accommodate the maximum current flow.

The matching networks of the amplifier are designed based on the small-signal input and output impedances extracted from on-wafer measurements of the single HBT. Since output impedance is expected to deviate from the small-signal value under large-signal conditions, matching to the large-signal load-pull output impedance should improve output power. The matching networks consist of coplanar lines at the base and the collector port of the HBT, shunted with capacitors to ground. At the base side, this configuration is the same as it was used for prematched HBT designs (see fig. 2), which yields a compact network. At the collector side, a longer line in the range of 1 mm and a smaller capacitor are required.

Spiral inductors are used as chokes for DC current feeding. The design of the inductors has to take into account not only inductance and parasitic elements, but also the maximum current flow, which is particularly critical at the underpath of the spiral. This must be considered for the the inductor layout.

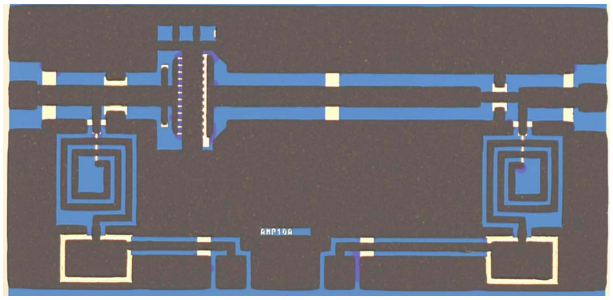

Fig. 5. Chip photo of the 9 GHz amplifier. The chip size is 2.175 x 1.028 mm^2.

IV. Amplifier Measurements

The measured S parameters of the amplifier are plotted in Fig. 6. They behave as designed: at 9 GHz, we find low input and output reflection coefficients of about -10 dB and a gain of about 9 dB, which is close to the MAG value.

The large-signal measured data is shown in Fig. 7. The MMIC was measured on-wafer in a 50 Ohm system. At the designated bias voltage of 9 V, the maximum PAE is larger than 57%, with an associated output power of 2.3 W. Saturated output power at 9 V is 2.7 W. With a higher bias voltage of 11 V the output power of the amplifier can be increased up to 3.2 W with the PAE still exceeding 47%.

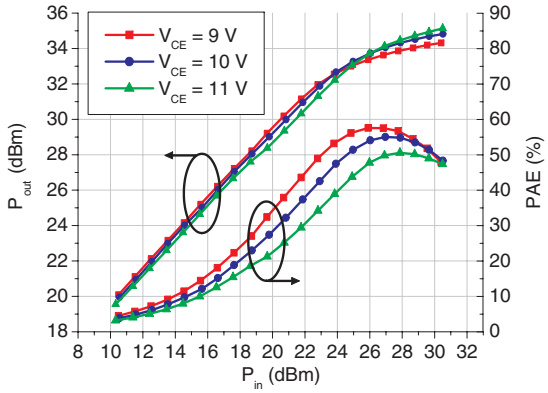

Fig. 7. Power measurements of the 9 GHz amplifier: Output power P_{out} and PAE against input power P_{in} with collector bias voltage as parameter.

V. Conclusions

A GaInP/GaAs power HBT with 24 V breakdown voltage for X-band applications is presented. A monolithic coplanar amplifier was fabricated to demonstrate device and MMIC performance. At 9 GHz, 3.2 W maximum output power with almost 10 dB linear gain was achieved. To our knowledge, this is the highest published output power for a single GaAs-HBT power cell in this frequency range. The results proov potential of this technology for high-power applications. Work is in progress to build more complex MMIC amplifiers with optimized designs and several power cells combined in one circuit.

Acknowledgment

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