An Active Balun for High-CMRR IC Design

Francesco Centurelli[1], Raimondo Luzzi[2], Piero Marietti[1], Giuseppe Scotti[1],
Pasquale Tommasino[1], Alessandro Trifiletti[1]

[1]University of Rome "La Sapienza", Department of Electronic Engineering,
Via Eudossiana 18, I-00184 Roma, Italy, +39 06 44585679
[2] Infineon technologies Austria AG, Development Center Graz,
Babenberger Str. 10, A-8020 Graz, Austria, +43 05 1777 5394

***Abstract* — A circuit topology that provides large bandwidth single-ended to differential conversion is presented. The proposed cell is based on a differential pair where feedback on common mode signal provides about 6 dB conversion gain increase, together with attenuation of common mode signal. Small-signal characterisation is presented, based on a block decomposition of the cell. Measurements on a SiGe test IC show more than 5 dB of gain improvement with respect to a simple differential pair.**

I. INTRODUCTION

The active balun (BALunced – UNbalanced convertor) is a basic cell required to provide single-ended to differential conversion for applications in a wide frequency range, e.g. the operational amplifiers for low-frequency analog signal processing, and circuits for wireless communication and optical digital telecommunication systems [1]-[7]. For instance, in the receiver chain of a digital optical communication system, a single-ended to differential converter is used to transform the unbalanced signal from the photodetector to a differential signal. Conversion to differential-mode is performed in the first blocks of the receiver, in order to take benefit of the common mode noise rejection provided by differential topologies. Simple differential pairs with single-ended input have been used as active baluns in both wireless [4]-[5] and optical [6] systems: their common-mode rejection capability makes them preferable in receiver chain design. The second input is usually grounded or is biased by low-pass filtering of the input signal [8]. In [4] the second input is used to provide L-C-R series feedback in order to adjust gain and phase unbalance of the differential pair used as active balun in a phase splitter. Some techniques have been introduced in order to increase the differential-mode gain, by applying a proper signal also at the second input of the differential pair. In [7] active feedback is used to drive the second input of the differential pair: a larger input differential-mode signal is obtained so that the effective differential-mode gain is increased.

In [9] some of the authors proposed a new topology of active balun, based on the differential pair. Such topology allows about 6 dB of extra gain, and attenuation of the common mode signal with respect to a simple differential pair with a grounded input, due to a common mode feedback loop that is able to provide an out-of-phase signal at the second input of the cell. This topology is conceptually similar to the former in [7], but design constraints are more flexible. In fact, in [9] the loop used to provide the signal at the second input of the differential pair is completely independent of the main differential pair itself, thus allowing independent optimization of the two gains. However, the two topologies share problems in obtaining proper stable bias for the feedback transistor.

Here, the novel topology is presented in detail, together with a solution to provide proper biasing and therefore to design robust circuits in bipolar, and field-effect integrated technologies. A complete model for small-signal behaviour has been developed, that allows both circuit behaviour understanding by means of block decomposition and feedback theory, and the design of active balun's in integrated technologies.

II. THE PROPOSED BALUN TOPOLOGY

In [9] a new topology for active balun was proposed based on a differential pair and a feedback inverting amplifier. The basic idea is to use a negative feedback configuration, that allows to sense and amplify the common mode at the common source (or emitter) node of a differential pair. If the differential pair is driven by a single-ended input signal, the amplified and inverted common mode can be used to feed the second input of the differential pair. In the limit of infinite feedback loop-gain, a signal with the same module and opposite phase with respect to the input signal is generated: the cell allows 6 dB of extra conversion gain and vanishing input common mode, so that output common mode is suppressed too. In this topology, circuit biasing is strongly sensitive to process parameter dispersion as for a simple differential pair balun, and external trimming is needed to ensure proper operation. A modification to the basic topology is here proposed to overcome this problem: a second differential pair can be used as feedback stage instead of the inverter (see Fig. 1). The differential output of the balun is filtered and its DC component is amplified and used to drive the second input of the feedback differential pair (node 4): the DC feedback loop reduces output offset and provides correct operation of the balun. The proposed topology shows improved overall performance with respect to the simple differential pair used as a balun, in a wide frequency range under the hypothesis that the poles introduced by the feedback amplifier do not affect frequency performance of the main differential pair. The proposed topology is therefore useful to design blocks for signal

processing in very diverse application fields. In particular, it has been used in recent years to design a transimpedance amplifier as the first block of a 10 Gb/s optical receiver [10] in GaAs HEMT technology; it has been proposed as a block in the CMOS IF section of a wireless receiver [11], and to design the output stage of a COA in CMOS technology [12].

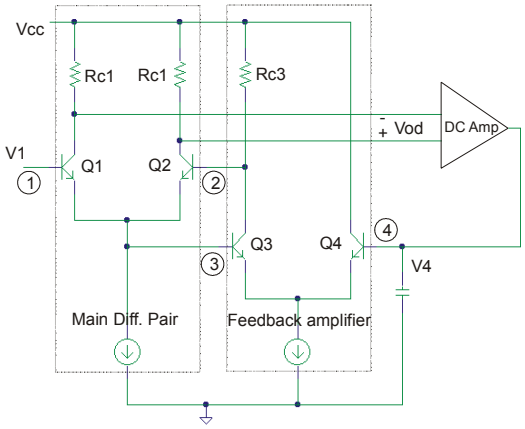

Fig. 1. Schematic circuit of the active balun.

The wide range of applications of the topology may involve different design constraints according to the given design goals. An accurate signal model is required that is able to allow performance comparison with respect to a simple differential pair and to provide straightforward design guidelines. If the classical feedback theory is used to determine the closed-loop performance, a sufficiently accurate model is found at low-frequency: each block can be considered as unilateral, and the mutual loading effects are easily evaluated. At frequencies higher than the cut-off of the loop gain the hypotheses above are not fulfilled, and only an approximate evaluation can be obtained. An alternative approach that does not consider unilateral approximation of the feedback block and does not make use of a linear two-port representation is the return-ratio analysis. However, the representation obtained for the network is not fully compatible with the feedback-based scheme.

In this work, block decomposition of the circuit has been used to evaluate circuit response. Three-port admittance matrices Y^A and Y^B, shown in Fig. 2, have been used to represent the gain stage (ports 1 and 2 refer to the gate nodes and port 3 to the coupled source node), and the feedback differential pair (ports 1 and 2 refer to the gate nodes and port 3 to the drain node), respectively. The block decomposition used to evaluate the closed-loop transfer function, by taking the mutual loading effects into account, is shown in the right side of Fig. 2. The connection between the networks is broken, and proper equivalent admittances y_a and y_b that accounts for the closed-loop loading effect of each of the blocks on the other one are introduced:

$$y_a = \frac{I_1^B}{V_3} = y_{11}^B - y_{13}^B \cdot \frac{y_{23}^A + y_{31}^B}{y_{22}^A + y_{33}^B} \qquad (1)$$

$$y_b = \frac{I_2^A}{V_2} = y_{22}^A - y_{23}^A \cdot \frac{y_{22}^A + y_{33}^B}{y_{23}^A + y_{31}^B} \qquad (2)$$

where I_1^B and I_2^A are the currents flowing in closed-loop connection into port 1 of block B, and port 2 of block A, respectively, under the hypotheses that a signal is applied at node 1, node 4 is shorted. Then, the transfer function of each block is evaluated by means of an equivalent open-loop configuration. In particular, the transfer function A_{f1} is evaluated by using the closed-loop admittance y_b:

$$A_{f1} = \frac{V_2}{V_3} = -\frac{y_{31}^B}{y_b + y_{33}^B} \qquad (3)$$

The common mode at node 3, as a function of the input signal V_1 and feedback signal V_2, with node 4 shorted, is evaluated as transfer function A_c by using the closed-loop admittance y_a:

$$A_c = \frac{V_3}{[(V_1 + V_2)/2)]} = -\frac{2\,y_{31}^A}{y_a + y_{33}^A} \qquad (4)$$

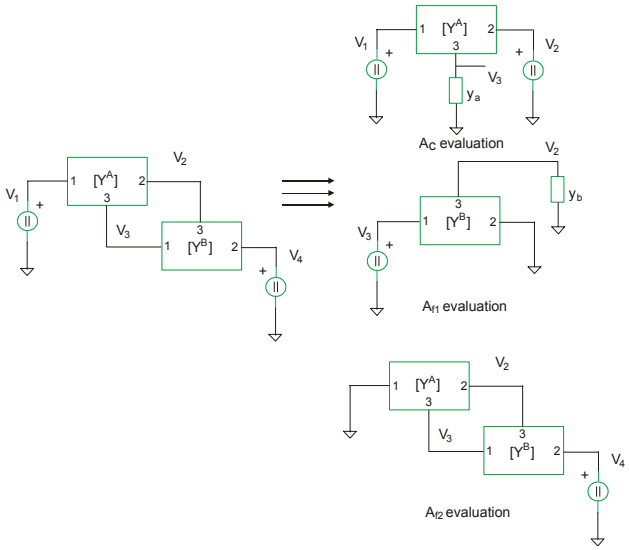

Fig. 2. Equivalent representation of the active balun.

The block decomposition presented above has been used to determine the input common mode voltage v_{ic} and the differential mode voltage v_{id} of the gain stage as a function of input signal at nodes 1 and 4:

$$v_{ic} = \frac{V_1 + V_2}{2} = \frac{V_1}{2\cdot(1+T)} + \frac{A_{f2}}{2} V_4 \qquad (5)$$

$$v_{id} = V_1 - V_2 = \frac{1+2T}{1+T} V_1 - A_{f2} V_4 \qquad (6)$$

where the gain T of the feedback loop has been defined as:

$$T \equiv \left(-\frac{V_2}{V_1 + V_2} \right)_{V_4=0} = -\frac{A_c A_{f1}}{2} \qquad (7)$$

and A_{f2} is the transfer function from node 4 to node 2 with node 1 shorted:

$$A_{f2} = \frac{V_2}{V_4} = -\frac{T}{y_{31}^{A} \cdot (1+T)} \cdot \left[y_{12}^{B} - y_{32}^{B} \frac{y_{11}^{B} + y_{33}^{A}}{y_{31}^{B} + y_{13}^{A}} \right] \quad (8)$$

It can be seen that the input common mode generated by a signal contribution at node 1 is attenuated by the loop-gain, and the input differential mode is doubled if an infinite loop-gain is considered.

A complete characterisation of the cell is obtained by evaluating the input admittance y_{in1} at node 1, expressed as:

$$y_{in1} = y_{11}^{A} - y_{13}^{A} \cdot \frac{A_c}{2 \cdot (1+T)} \quad (9)$$

Finally, the overall transfer functions of the balun are straightforwardly evaluated using Eqs. (5) and (6) and the transfer functions of the main differential pair for both the common mode (A_{cm}) and the differential mode (A_{dm}). Based on the considerations above and using Eq. (6), the overall differential mode gain A_{vdm} of the balun can be evaluated as:

$$v_{od} = A_{dm} \cdot v_{id} = A_{dm} \cdot \frac{1+2T}{1+T} \cdot V_1 = A_v \cdot V_1 \quad (10)$$

where V_4 is considered as grounded.

The output common mode can be also evaluated by means of Eq. (5), under the hypothesis of node 4 grounded:

$$v_{oc} = A_{cm} \cdot v_{ic} = \frac{A_{cm}}{2} \cdot \frac{V_1}{1+T} = A_{vcm} \cdot V_1 \quad (11)$$

where A_{vcm} is the overall common mode gain of the balun.

III. Circuit Implementation

A MMIC has been designed by using the STMicroelectronics BiCMOS7 technology that features SiGe HBT's with a maximum f_T in excess of 65 GHz, to compare performance of the proposed balun converter topology to a simple differential pair. The designed MMIC contains three distinct test circuits. The first two circuits present the topology in Fig. 3, composed of a 50 Ω single-ended voltage buffer, the core active BALUN, and a 50 Ω differential voltage buffer.

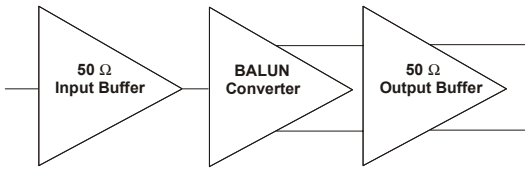

Fig. 3. Block scheme of the designed baluns.

As the core active balun, a simple differential pair has been designed in the first case. A second differential pair has been added in the second circuit, in order to sense and amplify the common mode at the emitter node of the main differential pair. The second input of the feedback differential pair has been made available as an output pin in order to provide proper biasing by means of an off-chip DC feedback loop. Finally, a third circuit containing the input and the output buffer has been added for reference. On-chip preliminary measurements have been performed by means of a probe station and a Network Analyser (see Fig. 4), and manually providing the proper bias at the second input of the feedback differential pair. In Fig. 5 the conversion gain of the proposed balun is compared to the one of the balun based on the simple differential pair: more than 5 dB of gain improvement has been found for the proposed topology, and a -3 dB cut-off frequency of 7.2 GHz has been measured, resulting 0.4 GHz lower with respect to the simulated value. Moreover, as the reference circuit composed of both the input and output buffers shows a measured conversion gain of -14.5 dB, the gain of the core balun is 22.7 dB. In Fig. 6, the S_{11} and the S_{22} parameters of the proposed balun are also shown.

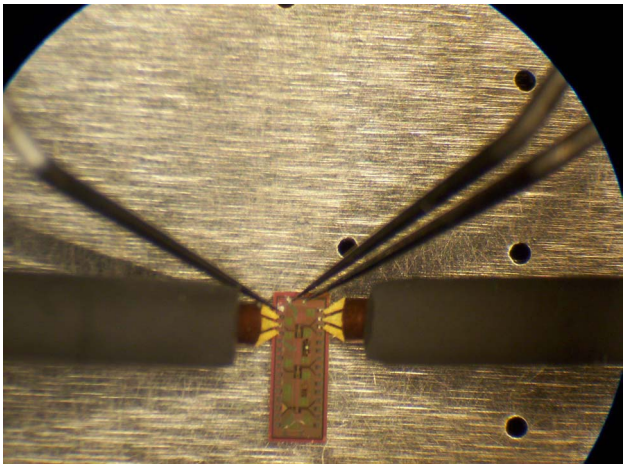

Fig. 4. On-chip measurements of the designed circuits.

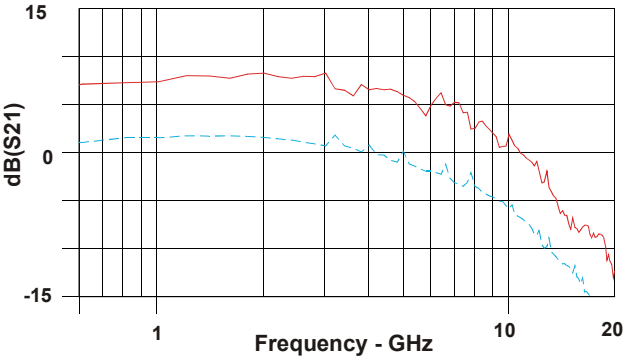

Fig. 5. Measured conversion gain of the designed baluns.

IV. Conclusion

An active balun topology suitable to be used for the design of integrated circuits in a wide range of applications has been proposed. A technology independent small signal model has been provided to highlight design constraints. Finally, a MMIC in SiGe technology has been fabricated and measured in order to compare performance to the ones of a simple differential pair. As a result, an improvement of more than 5 dB in the conversion gain has been found.

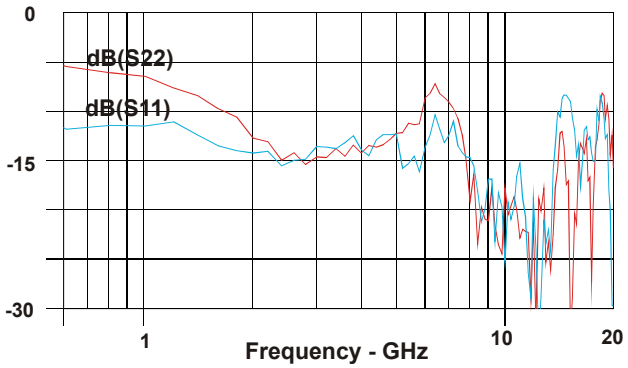

Fig. 6. Measured S_{11} and S_{22} of the proposed balun.

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