A Novel Technique for Obtaining LO and RF (LSB) Rejection in 25-40 GHz Microwave Up Conversion Mixers Based on the Concepts of Distributed and Double Balanced Mixing

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***Abstract* — In this paper a new configuration of up converter is presented. In this circuit, the LO and RF (LSB) frequencies are rejected thanks to a distributed and balanced circuit. Eight GaAs PHEMTs with a gate-length of 0.25 µm are used. A conversion gain of -6 dB and a rejection over 6 dB on LO and RF (LSB) are obtained.**

I. Introduction

During last years most of communication systems use mixers circuit in transmit or receive branches. When IF is very low or directly in base band, it is no more possible to use filtering techniques to reject LO or one of the modulation side bands. Even with the use of hybrid filters.

In case of up-converters or modulators, the rejection of unwanted frequencies can be obtained by using distributed phase shifters. It is hence possible to reject LO, RF (LSB) and possibly IF. An example of one of these mixers is described. The mixing is operated via four mixing cells, each of them containing two single-gate PHEMTs in a cascode mounting. The operation frequencies are F_{LO} = 29 GHz and F_{IF} = 2 GHz at the input and F_{RF} = 31 GHz at the output. The applied input powers are P_{OL} = 14 dBm and P_{IF} = 10 dBm.

II. Mixer Design Procedure

The design procedure for this circuit is based on the balanced and distributed mixers theories [1]. The heart of the mixer uses two PHEMTs in cascode mounting. Usually, the distributed mixers are using transmission lines to work at a wide band. The originality of this circuit relates on the use of these lines to introduce phase shifts between the cascode cells. The design is based on a PH25 (pseudomorphic heterojunction PHEMTs) technology from UMS.

A. Modeling of Cascode Mounting

A cascode mounting is constituted of two single-gate PHEMTs as shown on Fig. 1. In our circuit, these transistors are single-gate PHEMT having a gate length of 0.25 µm and a width of 75 µm. The first transistor is used as a mixer while the second one amplifies the modulated signal. The I/V characteristics of the cascode mounting PHEMT can be extracted from those of the single gate devices by observing rather obvious constraints: the channel current in both devices must be equal, and $V_{gs2} = V_{g2s} - V_{ds1}$. The applied voltages are V_{ds}, V_{g2s} and V_{gs1}.

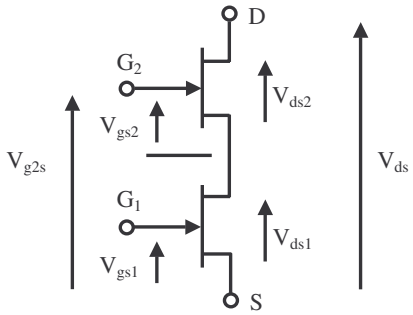

Fig. 1. Two single-gate PHEMTs connected in series (cascode mounting).

To determine the drain current for any set of applied voltages, V_{ds1} is treated as an independent variable and is varied between zero and V_{ds} until a value giving the same drain current for both single-gate PHEMTs is found.

The current in the upper PHEMT is controlled by its gate-to-source voltage, as is the current in the lower PHEMT. The gate-to-source voltage, in the lower PHEMT, V_{gs1}, is the applied gate voltage. In the upper PHEMT, however, the applied voltage V_{g2s}, is described by the relation given above.

The curves of Fig. 2 show how the I/V characteristics of the cascode PHEMT can be derived from those of the individual single-gate PHEMTs.

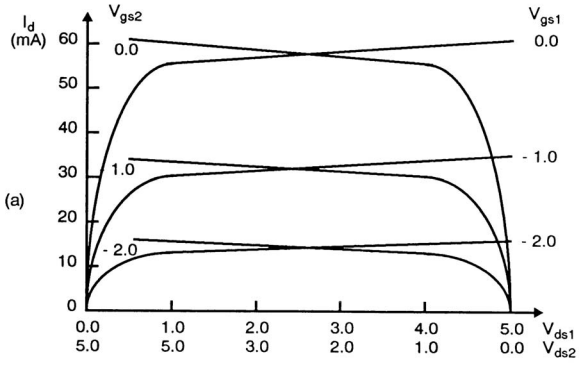

Fig. 2. I/V characteristic of the cascode FET in terms of V_{gs2}.

The points of intersection correspond to the different identical drain currents into each single-gate PHEMT.

The curves of Fig. 3 show the I/V characteristics of the cascode PHEMT for different values of V_{g2s}.

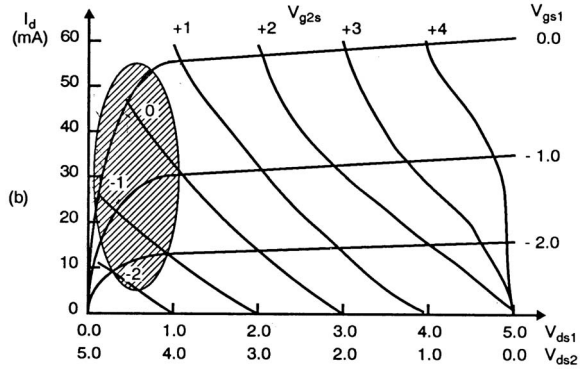

Fig. 3. I/V characteristic of the cascode PHEMT in terms of V_{g2s}.

The shaded area shows one of the regions where the operating points of the two devices must be located to get successful mixing and a good conversion gain. The biasing of the PHEMTs will be done in this region.

B. Modeling of the mixer

The circuit is shown in Fig. 4. Two series of phase shifting cells can be seen on this figure. One of the series introduces a phase delay while the other introduces a phase advance. These cells have a 50 Ω characteristic impedance and represent the LO and IF input accesses.
The phase difference between two successive cells of the IF line is + 90° and for the LO line it is - 90°.

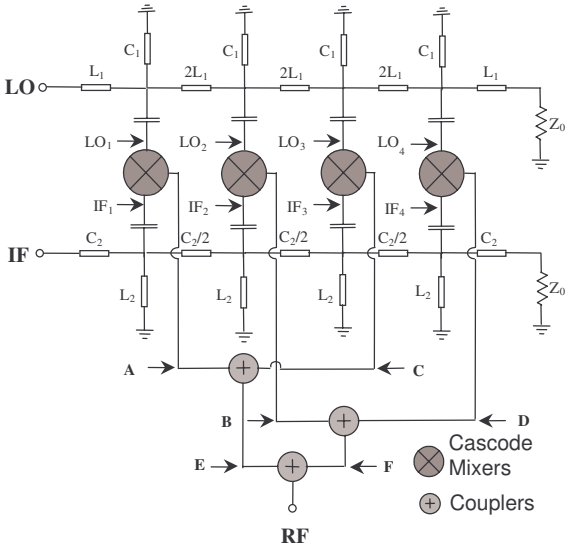

Fig. 4. Electrical diagram of the LO and low RF rejection mixer.

Connecting the PHEMTs to the lines induces some power loss, this loss is due to the gate resistances of PHEMTs. These losses will be compensated by the gain of the transistors but have to be controlled. When a small series resistance R is added to the shunt capacitance C_1 as on Fig. 5. The frequency-dependent loss per section is given by $e^{-\alpha}$ [2][3], where $\alpha \approx 4\pi^2 f^2 C_1^2 RZ / 2$, in which Z is the characteristic impedance of the line.

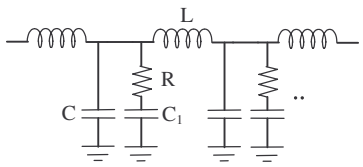

Fig. 5. Periodic synthetic transmission line with frequency-dependent loss.

Table I hereafter shows the phase distribution of the circuit of Fig. 4. And Table II indicates which frequencies will be rejected.

A	**B**	**C**	**D**
IF ∠ 0°	IF ∠+90°	IF ∠+180°	IF ∠ +270°
LO ∠ 0°	LO ∠-90°	LO ∠-180°	LO ∠-270°
RF ∠ 0°	RF ∠ 0°	RF ∠ 0°	RF ∠ 0°
RFL ∠ 0°	RFL ∠180°	RFL ∠ 0°	RFL ∠180°

TABLE I
DISTRIBUTION OF PHASE SHIFTS IN THE CIRCUIT

The outputs **A** & **C**, **B** & **D** and **E** & **F** are added using three Wilkinson couplers with two accesses, or a new single four accesses Wilkinson coupler.
The results of that addition are shown on the Table II.

E = A + C	**F = B + D**	**RF = E + F**
IF Rejection	IF Rejection	IF Rejection
LO Rejection	LO Rejection	LO Rejection
RF ∠ 0°	RF ∠ 0°	RF ∠ 0°
RFL ∠ 0°	RFL ∠-180°	RFL Rejection

TABLE II
DESCRIPTION OF THE FREQUENCIES, WHICH ARE REJECTED

The Fig. 6 shows the chip photograph of the rejection modulator using the MMIC technological rules of PH25 PHEMT process technology of United Monolithic Semiconductors.

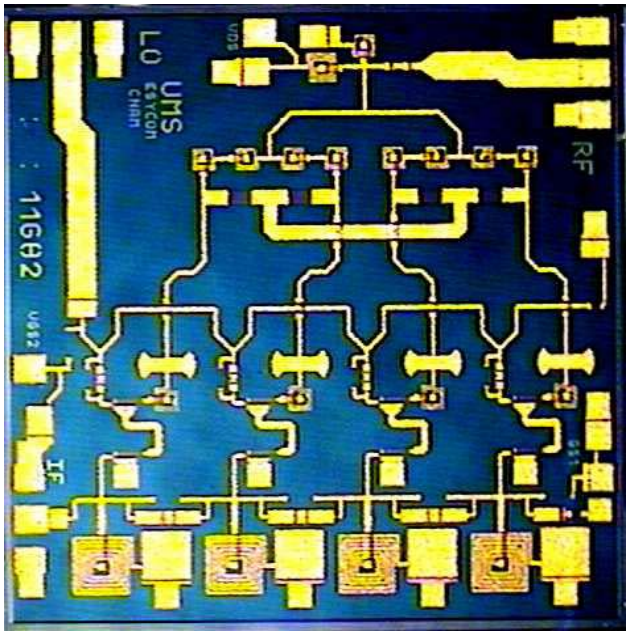

Fig. 6. Photograph of the MMIC Layout: 2.1 x 2.2 mm^2.

This layout contains several transistors assembled in cascode two by two and several passive elements (capacitors, spiral inductors, air-bridges, microstrip T lines, …).

We can observe that the LO way is made with a synthetic line which allows a phase shift of -90° from each gate to the other. The IF way is constituted by a series of discrete components (capacitors and spiral inductors), introducing a +90° phase shift between each PHEMT gate.

This choice of design is due to the opposite phase shifting sign between the two accesses LO and IF. The large difference of frequency between IF and LO introduces a large difference in size between the two series of cells. We can also observe that the four cascode drains are combined with a four ports Wilkinson coupler after a matching circuit.

This circuit is deposited on a GaAs substrate with a wafer thickness of 100 µm. The monolithic wafer contains several passive components; a microstrip Tline, eight PH25 PHEMT transistors and its dimensions are 2.1 x 2.2 mm².

III. Simulated Results

Fig. 7 shows the conversion gain and rejection which can be obtained by simulation as a function of LO frequency for a LO power of 11 dBm, an IF power of -9 dBm and a biasing of V_{ds} = 2.5 V, V_{gs1} = -0.4 V and V_{g2s} = 0.7 V.

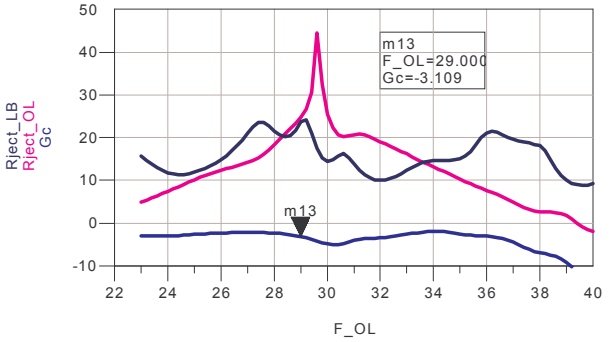

Fig. 7. Simulated output powers (RF_{LSB}, LO & RF) in term of injected LO frequency in GHz.

The optimal conversion gain was obtained for the bias points above. It value is -3 dB ± 1 dB over the [24-36] GHz F_{OL} sweep value. The rejections are higher than 10 dB over this frequency band.

IV. Measured Results and Comparison with Simulations

The circuit was realised in GaAs technology but because of a defect in this realization, it was not possible to bias the gates of the transistors.

So, the circuit has been tested on-wafer for V_{gs1} and V_{g2s} = 0 V (Fig. 8) using a measurement setup based on an Agilent E8257D synthesizer for the LO input power, an R&S SMT03 synthesizer for the IF input power and an Agilent E4448A spectrum analyzer.

For the full characterization of the device, different measurements and simulations have been performed versus drain bias, input powers level (IF & LO) and frequencies. The most revelants are listed below.

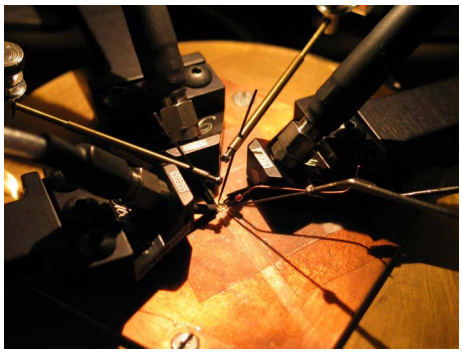

Fig. 8. Photograph of the tested wafer by using RF and DC probes.

Fig. 9 presents the first analysis of the mixer. It shows the simulated and measured output RF power versus the bias drain voltage Vds.

The injected powers were fixed at 14 dBm for LO and 10 dBm for IF.

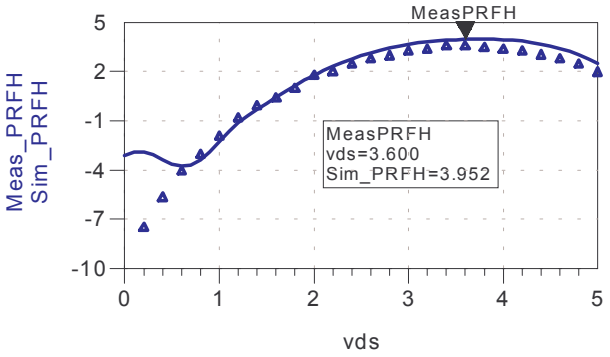

Fig. 9. Measured and simulated RF output powers in term of bias drain voltage Vds (V).

A maximum RF power of 4 dBm was extracted with good correction between simulation and experiments at a Vds drain voltage of 3,6 V.

Taking into account the circuit's defect, the results here after will be only presented for gates voltages (V_{gs1} and V_{g2s}) of 0 V. The total drain voltage is fixed at 3,6 V.

The simulated and measured output powers are presented in Fig. 10.

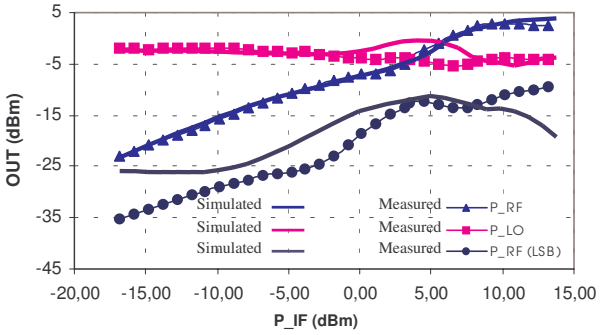

Fig. 10. Measured and simulated (RF_{LSB}, LO & RF) output powers for a LO frequency of 29 GHz.

A maximum RF power of 4 dBm was measured with IF input power greater than 9 dBm and for a fixed 14 dBm LO input power. The LO and RF_{LSB} output powers are respectively -5 and -10 dBm.

The mixer's performances can be shown in term of conversion gain and sub-harmonically rejections (Fig. 11).

The maximum conversion gain value is -6 dB at 9 dBm input IF power and higher than -10 dB over the entire P_{IF} sweep.

Such a conversion gain is sufficient at these high frequencies as given in [4], taking into account the losses in complex structures.

The LO signal becomes lower than the RF signal, i.e. the LO rejection is positive, for an IF input power above 4 dBm, its maximum value is 7 dB at 11 dBm.

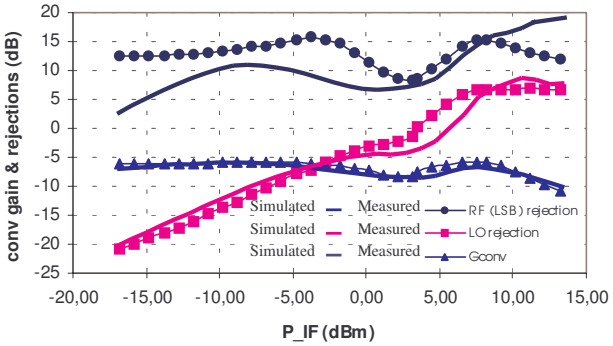

Fig. 11. Measured and simulated output conversion gain and (LO, low RF) rejections for LO frequency of 29 GHz.

The low RF rejection is above 8 dB over the entire IF input power sweep.

The simulated and measured curves of Fig. 12 present the performances of the circuit in term of LO frequency band.

The input powers were fixed at 12 dBm for LO and 8 dBm for IF. These power values make the simulation converge at the 25-40 GHz LO frequency band.

We observe that the RF output power is comprised between -4 and +2 dBm over all the LO frequency sweep.

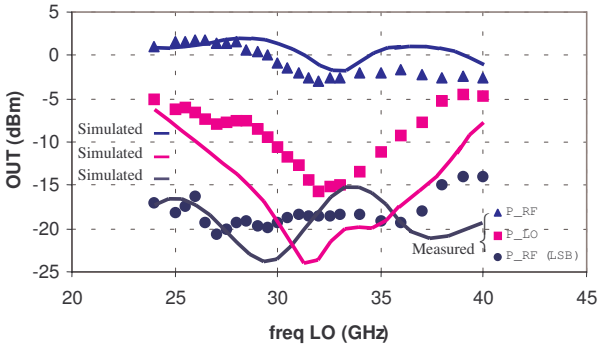

Fig. 12. Measured and simulated output powers (RF_{LSB}, LO & RF) in term of injected LO frequency.

The minimums LO and RF (LSB) output powers are respectively -15 and -20 dBm.

Fig. 13 presents the output mixer's spectrum. It shows the rejection between the RF and all the other rays.

The measured RF power level is about 1 dBm after subtracting the output cable losses (2 dB at 31 GHz).

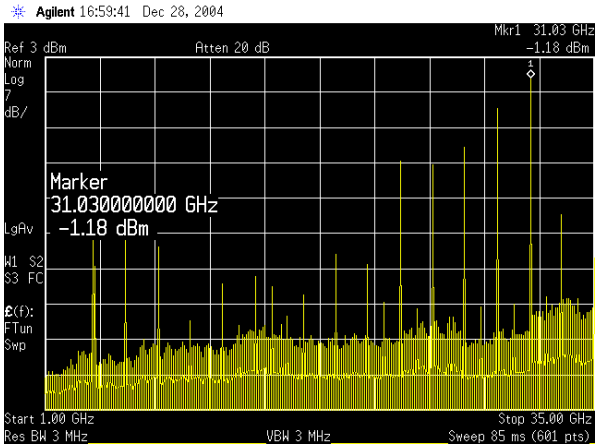

Figure 13. Output mixer spectrum obtained for injected 12 dBm and 8 dBm LO and IF powers levels.

V. Conclusion

The original topology of our up-converter mixer structure [5], constitutes a new approach of the low RF and local oscillator rejection modulators. Compared to a conventional modulator with rejection, the lumped components count was decreased. It means that the circuit size was decreased too. These modulator works at relatively high frequencies, and the phase shifting technique replace the active filtering, which cannot be used in MMIC technology.

The simulated performances of our circuit are -3 dB for the conversion gain and more than 10 dB of sub-harmonically rejections. Due to a defect in the process of the DC feed resistance layer, the measurement are presented only for gate voltages of 0 V.

In this case, the main performances of our circuit are a conversion gain of -6 dB for an IF power of 9 dBm and a good power rejection (over 5 dB) for the LO, and the low RF frequencies. And these results are in good agreement between simulation and measurements.

A new circuit is launched to confirm the results of simulations for an optimum biasing of the gates. This circuit is under run and will be tested very soon.

References

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