High Efficiency 10Gb/s Optical Modulator Driver Amplifier using a Power pHEMT Technology

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Abstract — **This paper presents the design and performance of a high efficiency GaAs MMIC distributed amplifier for 10Gb/s optical driver applications. The power consumption is only 550mW, approximately 40% lower than typical reported results for this application. It is shown that while the commonly-used cascode topology gives higher gain-BW performance, the ordinary common-source design gives better efficiency and stability performance. This makes it a better choice for 10Gb/s applications when a suitable high power pHEMT process is used.**

I. Introduction

Multi-decade amplifier design and technology for optical driver applications has progressed continuously to meet wider BW demands, including 40Gb/s systems and above. The transistors' frequency of operation and gain has increased by developing advanced process technology. Firstly, a short gate length with the same width reduces the capacitance while keeping the gain high. Secondly, channel modulation structures such as in the HEMT increase the mobility by reducing the scattering effects and further increase the gain/BW product. Heterojunction engineering leads to flexibility in the junction doping. Finally, optimising the device layout can significantly reduce the parasitics added to the intrinsic transistor.

The two amplifier topologies that are used for this ultra-wide bandwidth requirement are the distributed amplifier and the feedback amplifier [1-7]. Only the distributed amplifier topology provides a real improvement in the gain/BW product. Therefore, it is widely used for LiNbO3 modulator drivers for higher and higher bit rates. MMIC technology has improved constantly but many optical systems remain at 10Gb/s – with WDM techniques used to achieve extremely high aggregate data rates. It is valuable then to focus on design for 10Gb/s application and consider different DA structures that improve the efficiency of the amplifier, to ease cooling problems and facilitate optical-microwave system-in-package (SiP) integration.

A design for 10Gb/s is able to trade-off the ultimate gain and BW performance for improved efficiency. In this paper, we investigate the causes of low efficiency in the distributed amplifier and compare the common-source and cascode topologies. It is shown that when a suitably optimised high power device technology is available, using only common-source devices gives a small degradation of the gain and BW but yields a very significant improvement in the efficiency.

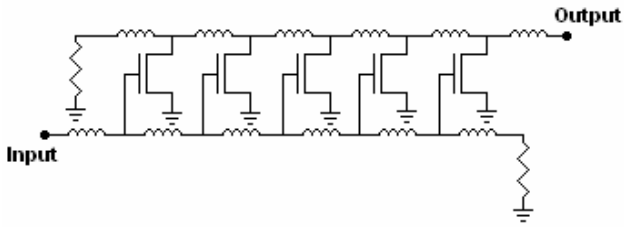

Fig. 1. Basic structure of the standard distributed amplifier with common-source stages.

II. Sources of DA Inefficiency

In the distributed amplifier (DA), the capacitors of each transistor are isolated while the drain currents from each transistor are added. The DA structure has gate and drain artificial transmission lines with a constant-K ladder structure. For the currents to add constructively, the delay of the two artificial transmission lines must be equal at all the pass-band frequencies. The amplifier BW is dictated by the relatively large transistor input capacitance.

Significant research has been carried out in order to study distributed amplifiers and improve their efficiency [8-11]. The inefficiency stems from the transistor itself and from the complicated DA structure. The transistor intrinsic Rds and Ri lead to losses in the drain and the gate line respectively [1, 12]. However, the losses at high frequency can be partially compensated by the high image impedance of the pi-network near cut-off to give flat gain up to a frequency close to the f_{max} of the transistor. For large-signal operation, regions in the transistor IV characteristic where the transistor does not function usefully, such as the triode region, of the transistor cause poor efficiency.

The standard DA structure is uniform; i.e., all constant-K sections are identical. It is difficult to match these sections over the whole frequency range since the Pi and T-section impedances are real but frequency dependent [3]. The unmatched ladder reflects some of the power and produces reflection along the gate and drain lines. This gives lower gain and produces signal distortion in the optical system. M-derived sections can be used as buffers between the constant-K ladder and the termination

resistor. This improves the matching over a wide range but does not solve the problem completely [3].

In the drain line the greatest source of loss is the reverse drain termination which absorbs half the power over much of the frequency range and reduces efficiency significantly. The other main source of inefficiency comes from having the transistors not all working at optimum power due to the gate-line loss and due to the non-optimum source and load presented to the devices by the artificial transmission lines. Only the last transistor's output terminal has all the currents synchronized, producing high voltage level.

III. Cascode Versus Common Source DA

Most early DA designs used the common-source structure shown in Fig. 1, but now the cascode stage DA shown in Fig. 2 is widely used. The cascode structure is built from a common-source followed by a common-gate FET.

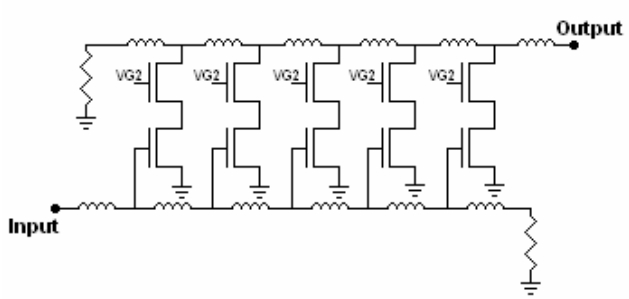

Fig. 2. High gain-BW performance distributed amplifier with cascode topology.

For achieving wide bandwidth and high gain the cascode DA structure has significant advantages over the common-source DA case; in particular, the cascode has higher output impedance, higher breakdown voltage and lower input capacitance.

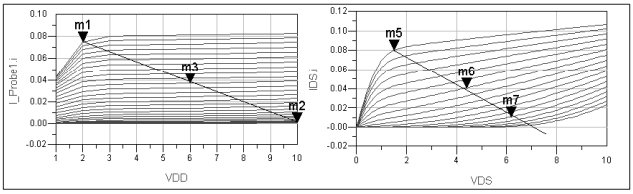

Fig. 3. Comparison of IV curves for the cascode structure (Left) and single common-source device (Right) for a generic pHEMT with ~ 8 V breakdown voltage.

The higher output resistance and higher breakdown voltage of the cascode are illustrated in Fig. 3. The higher output resistance reduces drain line loss and means that more sections can be used in the DA, giving higher gain-BW product. The cascode breakdown voltage is increased considerably and together with the high output impedance this allows a higher output swing voltage for high power operation. The lower input capacitance is a result of (a) the reduction of the voltage gain of the common-source device (reducing the Miller effect feedback current) because of the common-gate device's low input impedance, and (b) the common-source device's isolation from the voltage summation effect caused by the additive gain on the drain line.

Unfortunately, the cascode arrangement has increased circuit complexity and size, increased power consumption, and severe stability problems which the designer must combat. The efficiency is degraded since the cascode requires higher VDD supply voltage because the overall knee voltage is the sum of the two transistors individual knee voltages. In many circuits, the linearity is improved by increasing VG2 and VDD and this reduces the efficiency further.

Stability problems arise with the common-gate device which is particularly sensitive in its output feedback. For stability and high performance the common-gate device in DA application requires low delay, low Cds capacitance and low gate grounding inductance. When these parameters are not suitable, the DA cascode design would need to be stabilized using a combination of various circuit techniques. The overall performance would have lower gain and BW in most DAs as a consequence of the stabilizing circuitry.

Practical cascode DA designs cannot use simple shunt feedback [13] and instead will other indirect techniques that do not affect the artificial transmission line structure. In a practical design, resistors on the drain are often still needed at the output to stabilize the device. One such indirect technique is to use a resistor as a series negative feedback element at the gate terminal of the common-gate devices. Another is to use an inductance between the common-source and common-gate devices to reduce the negative output resistance [2,14]. A series feedback capacitor with minimised gate grounding inductance is another alternative [15]. A DA implemented in CPW instead of a microstrip reduces the common-gate grounding inductance.

For a 10Gb/s design, the performance advantages of the cascode are not essential to meet the target specifications, providing the technology used has low Cdg (reducing the feedback effect for more bandwidth), high Rds and high breakdown voltage. So, a significantly more efficient design can be realized with the common-source topology as long as the chosen device technology has suitable performance. For 10Gb/s, a smaller number of sections and larger periphery devices can be used, so the high output impedance (low drain line loss) of the cascode is not essential.

IV. DA design and Simulation

The amplifier specification was for the output stage of an optical modulator driver. Filtronic's 0.5µm pHEMT technology was selected for its high power and high volume manufacturing capability. The MMIC design used the simple form of the common-source DA. The first step was to evaluate the device and its gate capacitance as the BW-limiting factor. This showed very low Cgd, high Rds and a moderate gain with BW > 15 GHz, implying that the distributed amplifier was the only suitable solution – a feedback design needs a device with

f_T much higher than the design bandwidth. Finally, the breakdown voltage measured in a DC simulation was sufficient and the knee voltage was about 1V. That meant that the DC supply could be dropped significantly to 5.5V, reducing the power consumption.

The gate capacitance evaluated by S-parameter simulation was used to design a 6 transistor DA with simple lumped elements such as ideal inductors, capacitors and resistors. Later, all components were changed to Filtronic component models with the associated parasitic components. The amplifier uses capacitively-coupled stages with different coupling factors as suggested in [16] that compensate for the loss in the gate line. The amplifier layout is shown in Fig. 4: the first three transistor stages on the left have small coupling capacitance for low gate loss, while the last 3 transistor stages on the right have larger coupling capacitors, giving a more equal gate terminal voltage distribution.

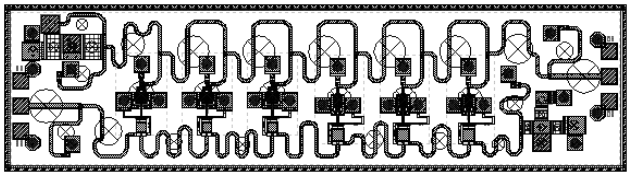

Fig. 4. Optical modulator Driver high power stage layout (3.75x1mm^2).

For lower power consumption, the MMIC DA used a decoupling capacitor to isolate the gate and drain terminations from the DC supply. The DA was intended to work down to 30 kHz, so the decoupling was split into on-chip and off-chip sections.

The MMIC amplifier simulation in Fig. 5 showed an 8 dB gain with BW > 15 GHz. The S11 and S22 show the input and output to be matched below -10dB for good power transfer and minimizing reflections and distortion. Finally the low S12 verified the circuit stability condition.

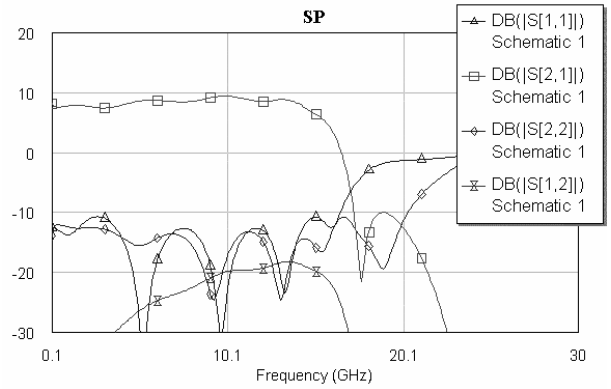

Fig. 5. Optical Modulator Driver SP simulation.

V. MEASUREMENTS

A microphotograph of the chip is shown in Fig. 6. The chip size is 1x3.75mm^2. The chip was fed with a DC gate voltage of -1.0V and a drain voltage of 5.5V. The circuit current consumption was 100mA, which gives an overall power consumption 550mW.

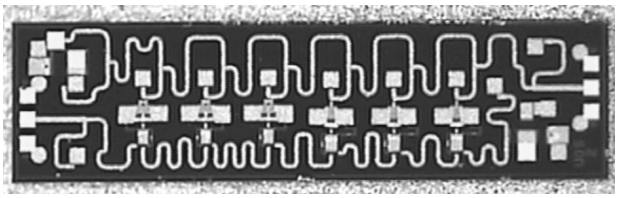

Fig. 6. Optical Modulator Driver high power stage microphotograph (3.75x1mm^2).

Figs. 7-10 show the frequency response of the DA, measured with bias tees but not with the external low frequency bias circuitry. The gain measured was 6-7dB which is enough in order to make the power consumption of the pre-amplification stage non-critical. A return loss below 10dB is achieved from 4GHz (where the on-chip part of the bias network becomes effective) to the stop-band. With the external bias circuitry, the low frequency matching will improve. The circuit is shown to be stable without the need for specialized CG device, stabilizing resistors or a stabilizing circuitry.

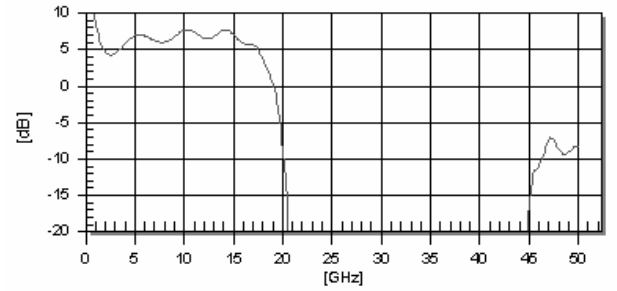

Fig. 7. Optical Modulator Driver S21 measurement.

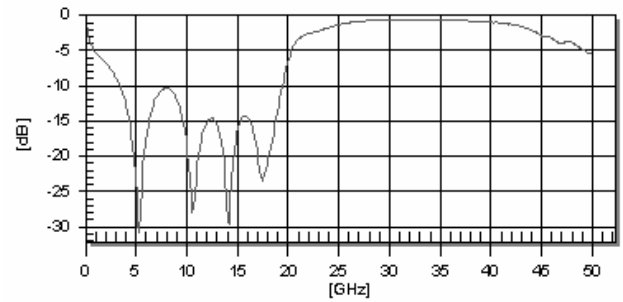

Fig. 8. Optical Modulator Driver S11 measurement.

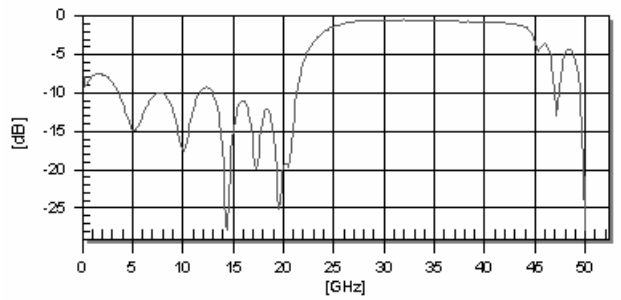

Fig. 9. Optical Modulator Driver S22 measurement.

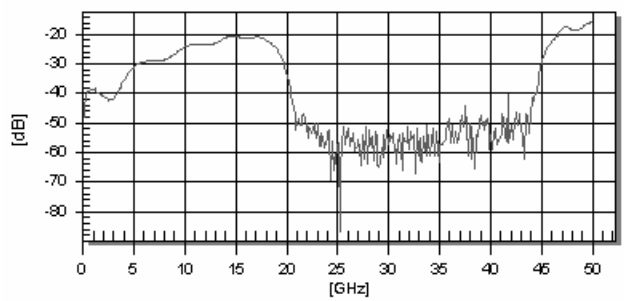

Fig. 10 .Optical Modulator Driver S12 measurement.

VI. CONCLUSION

A high efficiency DA for 10Gb/s optical driver application has been demonstrated by reducing the relatively high VDD needed in the cascode topology. This was accomplished through the use of a simpler common-source by using a high performance transistor with high breakdown voltage. The change has taken away some of the high gain and BW advantages of the cascode structure but now the amplifier may be integrated close to the heat sensitive optical modulator and reduce system cost. We have successfully designed and implemented the high power DA stage using 0.5um pHEMT technology as the last stage in the 10Gb/s optical driver applications.

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