Low Power Single-Ended Active Frequency Doubler for a 60 GHz-Band Application

Toru Masuda, Lars Landén*, Herbert Zirath*^

Hitachi, Central Research Laboratory, Tokyo, 185-8601, Japan.
Toru-crl.Masuda@c-net3.crl.hitachi.co.jp
*Chalmers University of Technology, Department of Microelectronics, Göteborg, SE-412 96, Sweden
landen@ep.chalmers.se and zirath@ep.chalmers.se
^Ericsson Microwave Systems, Mölndal, SE-431 84, Sweden,

Abstract

The design and characterization of a 28-56 GHz frequency doubler based on a commercial foundry GaAs pHEMT process is described. To realize low power consumption and high conversion gain with small input power at the same time, we employed a simple circuit topology composed of a single-ended active frequency doubler and a frequency selective buffer amplifier. The doubler chip occupies 2 mm^2 chip area and delivers 4 dBm with an input power of 0 dBm. The excellent unwanted harmonics suppression of 29 dB and low power operation of 40 mW were obtained.

INTRODUCTION

The millimeter-wave wireless communication systems are promising candidates to realize future multimedia communication. Especially, 60-GHz band radio system is watched with keen interest for the application areas of Wireless Local Area Networks, Wireless Broadband Access Systems, and Intelligent Transport Systems [1]. The 60 GHz-band has some advantages such as large spectral capacity, compact and light equipments, and small co-channel interference due to the property of large oxygen absorption. Consequently, the development of 60 GHz wireless transceiver is strongly required. For battery-operated systems, the power consumption of the transceiver is also an important parameter. Moreover, the transceiver must be realized with a highly integrated chipset at a low cost for the widespread commercial use.

Frequency multiplier is a key component to construct a low–cost LO-chain in the transceiver. Because of the lack of integrated fundamental-frequency oscillators with sufficiently good phase noise at the millimeter wave frequencies, the combination of a low frequency integrated oscillator and a few frequency-multiplier stages is a practical solution [2].

FREQUENCY DOUBLERS

Figure 1 categorizes previous works reported on frequency doublers' conversion efficiency and input power [3-8]. The dashed line shows an output power of –10, 0, and +10 dBm, respectively. The performances are listed in table 1. Figure 1 indicates that balanced doublers were mainly used to realize an output power of more than +5 dBm and conversion efficiency of less than 0 dB even though large input power of more than +8dBm was provided. Accordingly, an oscillator that is used with these frequency multipliers must generate and dissipate a large power. Moreover, the balanced doublers require large chip area to implement hybrids such as a Lange coupler or a balun. Therefore, we have designed a low power single-ended 28-56 GHz frequency-doubler for a LO-chain. In the design, we focused on obtaining an output power of more than +5 dBm with an input power at around 0 dBm, i.e. high conversion gain at low input power. Additionally, several approaches were used to meet the demands such as low power dissipation, small chip area, and good suppression of unwanted harmonics at the same time. The frequency doubler was fabricated by using OMMIC's D01PH-process. The process involves double delta-doped pHEMT with gate-length of 0.14 μm, 95-GHz f_T and 180-GHz f_{max}.

CIRCUIT DESIGNS

Figure 2 shows a circuit schematic of the single-ended frequency doubler and figure 3 shows the chip layout. This frequency doubler is composed of two active cascaded pHEMT-stages, the first pHEMT (T1) is used as a doubler with the gate-source bias voltage close to pinch-off, and the second pHEMT (T2) is used as a buffer amplifier for the second harmonic component of the input signal. The gate-width of both T1 and T2 were

100 μm in this design. The drain of T1 is biased through a transmission line TL3, which is RF-shorted at its end by a capacitor (Cp1) connected to a via-ground. In order to reject fundamental frequency component at the drain of T1 and deliver the second harmonic component to the buffer amplifier stage, the length of TL3 was optimised to provide a low drain load-impedance for fundamental frequency and a high impedance for the second harmonic frequency. The drain of T1 is connected to a buffer amplifier stage via an inter digital capacitor (IDC). The IDC works as both a dc-block capacitor and a band-pass filter to reject unwanted harmonics. At the drain, voltage supplies VD1 and VD2, a bias network, composed of resistor Rd and capacitors Cp, is introduced to suppress the resonance at the voltage supply when the chip is mounted on a module substrate via bonding-wires. The buffer amplifier consists of an open-stub (OS2), a common-source transistor (T2), and transmission lines (TL4-TL7). The minimization of the drain DC current of T2 is the most effective way to reduce the total power consumption. Therefore, we optimised the bias voltages of VG2 and VD2 in consideration for sufficient power gain and low DC power. By using a harmonic balance simulator, we determined the bias voltages VG1, VD2, VG2, VD2 to be –0.7, 2, -0.2, 2 V, respectively. The estimated power consumption was 57 mW with an input power of 0 dBm. The chip size is 2 x 1.5 mm. The design was performed by Herbert Zirath.

MEASUREMENT RESULTS

The experimental verification has been performed using on-chip power measurements utilizing coplanar RF wafer probes. The output power was measured by using a HP 3650A signal generator, a HP 8565E spectrum analyser, and HP 11974 pre-mixer. Power attenuation in cables, connectors, and probes were measured and used to correct the measured results.

We evaluated output power and power consumption dependence on bias conditions at an output frequency of 56 GHz. Figure 4(a) and (b) show the measured 2nd harmonic component of the output power and power consumption within a gate bias-voltage range of VG1 and VG2 from –1 to 0 V. The drain bias voltages of VD1 and VD2 were 2V. The frequency doubler delivered a maximum output power of 4 dBm with an input power of 0 dBm when the VG1 and VG2 were –0.7 V and –0.2 V. The power consumption was 70 mW. In the case when VG2 was –0.4V, the output power was still close to the maximum value, 2 dBm with a lower power consumption, 48 mW. Figure 5 shows the input power dependence of output power harmonics and conversion efficiency with a bias condition of VG1 = -0.7 V, VG2 = -0.2 V, VD1 and VD2 = 2 V. The output power saturates at 6 dBm when the input power was 5.5 dBm. The suppression ratio of fundamental frequency component is more than 26 dB within an input power range from –5 to +5 dBm. This result is caused by the circuit configuration with an IDC as a band pass filter. The simulated result of the 2nd harmonic component achieved good agreement with the measured result. The conversion efficiency has a maximum value of 4 dB with the input power –0.5 dBm. The measured frequency dependence of the output power can be shown in figure 6. The suppression of unwanted harmonics at the output frequencies 50 GHz and 56 GHz were 40 dB and 29dB, respectively. With an input power of 0 dBm, the maximum output power 6 dBm was obtained when the output frequency was 50 GHz. The 3dB bandwidth was 10 GHz from 47.5 GHz to 57.5 GHz; i.e. 19 %. These results were plotted as two star marks in figure 1. We confirmed that the frequency doubler we have presented has the highest conversion gain with such a small input power of 0 dBm and low power consumption. The measurements were performed by Toru Masuda and Lars Landen.

CONCLUSIONS

A low power single-ended 28-56 GHz active frequency doubler was designed and characterized. The frequency doubler achieved high conversion gain of 4 dB with small input power of 0 dBm, 40dB suppression of unwanted harmonics, and low power operation of 70 mW. These results indicate that this simple circuit topology with a buffer amplifier can be a good alternative in achieving all requirements for millimeter wave frequency multipliers.

ACKNOWLEDGEMENT

The Swedish Foundation for Strategic Research (SSF), Chalmers Center for High-Speed Technology (CHACH), The Swedish Agency for Innovation Systems (VINNOVA) are acknowledged to financial support. The authors also would like to thank Mr. Christian Fager for valuable discussions, and Dr. Katsuyoshi Washio, Hitachi Central Research Laboratory for this research collaboration.

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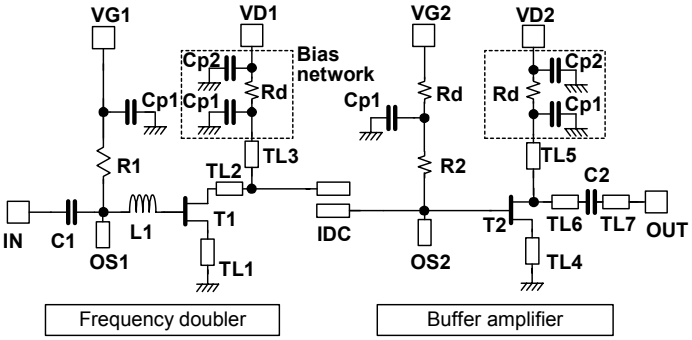


Figure 2. Schematic of the low power single-ended frequency doubler.

TABLES AND FIGURES

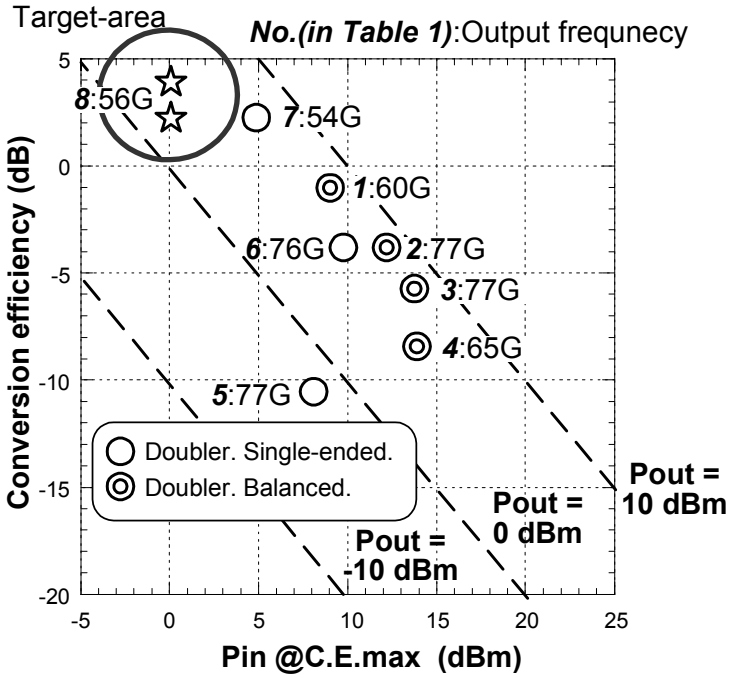


Figure 1. Relation between Input power and conversion efficiency

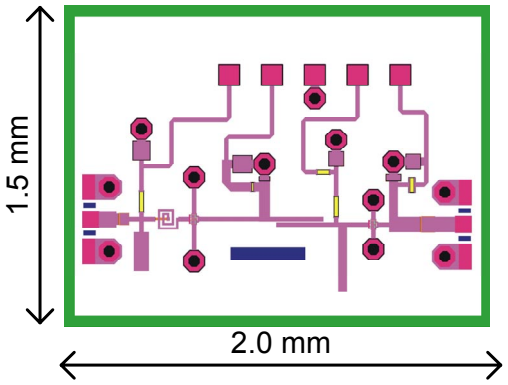


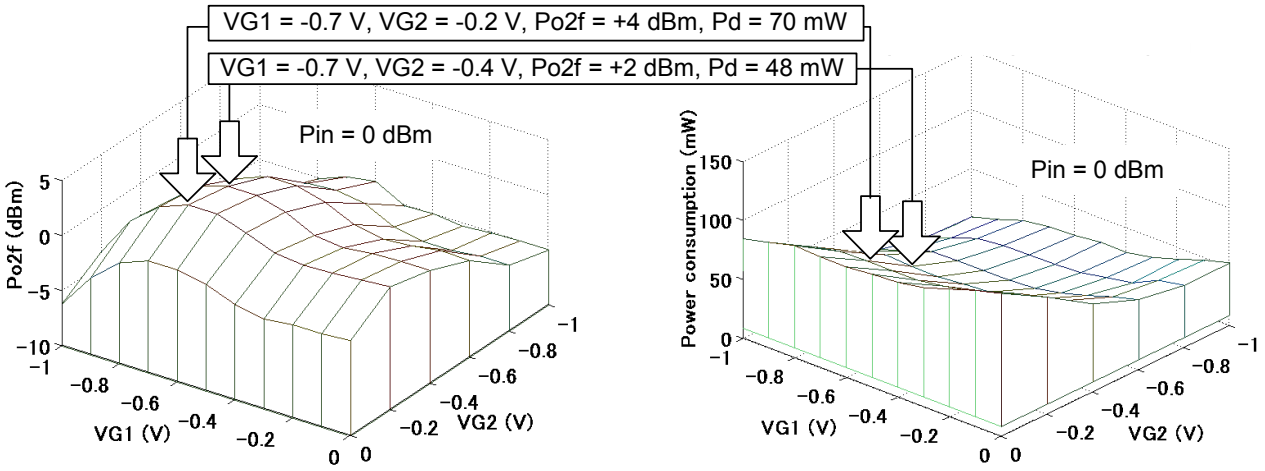
Figure 3. Chip layout of the low power single-ended frequency doubler.

Table 1. Frequency multiplier performances.

No.	Author	Device	Type	C.E. (dB)	Pin @ C.E.max (dBm)	Pout (dBm)	Fout (GHz)	BW (%)	Pdc (mW)	η* (%)	Ref.
1	Kangslahti	GaAs pHEMT	Balance	-1	9	8	60				3
2	Campos-Roca	GaAs pHEMT	Balance	-4	12	8	77	12	110	5,0	4
3	Campos-Roca	GaAs pHEMT	Balance	-6	14	8	77	17	86	5,7	
4	Piernas	GaAs pHEMT	Balance	-8,5	14	5,5	65	23	50	4,7	5
5	Caruth	GaAs MESFET	Single	-11	8	-3	77		27	1,5	6
6	Campos-Roca	GaAs pHEMT	Single	-4	10	6	76	20			7
7	Chalmers Univ.	GaAs pHEMT	Single	2	5	7	54	22	275	1,8	8
8	This work	GaAs pHEMT	Single	4	0	4	56	19	70	3,5	
				2	0	2	56		48	3,2	

C.E.: Conversion Efficiency

η* = Pout / (Pdc + Pin)



(a) Output power of 2nd harmonic component.

(b) Power consumption

Figure 4. Measured ouput power and power consumption as a function of bias voltages at the output frequency 56 GHz and the input power 0 dBm.

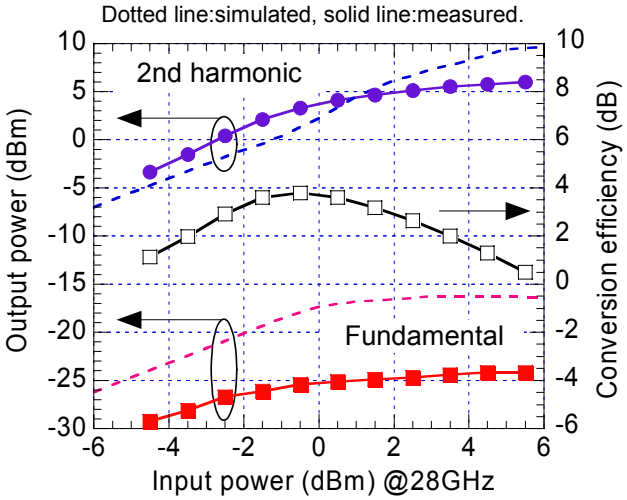


Figure 5. Measured ouput power dependence on input power at the output frequency 56 GHz with a bias condition of VG1=-0.7V, VG2=-0.2 V, VD1 and VD2=2 V.

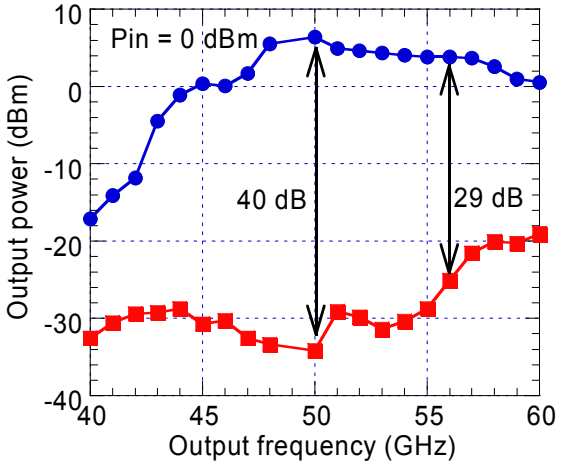


Figure 6. Frequency dependence of measured ouput power at the input power 0 dBm with a bias condition of VG1=-0.7V, VG2=-0.2 V, VD1 and VD2=2 V.