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Defective States in Semi-Insulating Gallium Arsenide Substrates

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Abstract

Semi-insulating gallium arsenide substrates are widely used for microwave discrete devices and integrated circuits. However, the performance of the above devices may be significantly affected by the substrate quality, i.e. crystal defects and related deep levels. Consequently, a careful characterization of substrates is mandatory to improve both device performance and production yields.

In this work we have investigated gallium arsenide substrates from different suppliers and/or differently processed. To these substrates we have applied, discussed and compared different methodologies (current-voltage and capacitance-voltage characteristics as well as spectroscopic methods) to characterize the many deep levels which are either present in as-received semi-insulating substrates or induced by device processing such as ion implantation and the subsequent thermal annealing.

Introduction

Semi-insulating (SI) Liquid Encapsulated Czochralski (LEC) gallium arsenide is extensively utilized as a substrate for microwave discrete devices and integrated circuits. In this kind of application, however, substrate quality plays a remarkable role on device characteristics and an accurate characterization of the substrates is compulsory to optimize the final circuit performance. Hence, the knowledge of the levels deep in the forbidden gap and of their compensation ratio is of major importance.

As late as a few years ago, it was commonly assumed that the electrical properties of SI GaAs were only determined by the dominant donor center EL2 with a midgap level at 0.75 eV from the conduction band. At that time the compensation was modelled with only three levels: the deep level EL2 and two shallow levels due to acceptor carbon and donor silicon. Shortly thereafter, it was realized that the actual electrical behavior of SI GaAs cannot be explained according to this simple model and that a realistic compensation model must account also for defects shallower than EL2 with significant concentration (on the order of 10^{15}cm^{-3}). Consequently, methods have been developed in order to sweep in high resistivity substrates the forbidden energy gap and to find energy position in the gap, capture cross section and concentration of deep centers other than EL2.

This paper will be concerned with characterization of defects occurring in substrates from different manufacturers or induced by ion implantation, typically employed in integrated circuits to create the device active region.

Experimental

Semi-insulating GaAs wafers grown by Liquid Encapsulated Czochralski (LEC) method received from Nippon, Hitachi and Freiberger have been analyzed. All these wafers were undoped <100> oriented, with n-type resistivity $\rho = 1 \div 3 \times 10^7$ Ωcm. Nippon and Hitachi wafers were 100 μm thick, while the Freiberger ones were 250 μm thick. Samples of 5×5 mm^2 were cut. To achieve the rectifying contact necessary for the electrical characterization, circular (diameter $\phi = 3$ mm) Schottky contacts were obtained by Au metallization (~ 150 Å thick) on sample front side. The ohmic contacts were realized with an Au/Ge/Ni metallization (1250Å/500Å/500Å) followed by a thermal cycle 430°C (20 s) in N_2+H_2 (10%) atmosphere.

To analyze the defects induced by ion implantation a few Hitachi samples were implanted with Si^+ ions at two different doses and energies, 7×10^{12} cm^{-2} at 300 keV and 1×10^{13} cm^{-2} at 40 keV. The wafers, with a reactively sputtered silicon nitride cap, were then fast annealed at 850°C for 30s. Finally, the ohmic contact was achieved by alloying an e-beam deposited AuGeNi multilayer at 420°C for 30 s. From now on the set of implanted samples will be referred to as Hitachi A and the as-received Hitachi B.

Current-voltage (I-V) and capacitance-voltage (C-V) characteristics at different temperatures were performed to electrically characterize the aforementioned materials and process.

To detect and possibly identify defects other than EL2, spectroscopic methods were applied. To this purpose Photo-Induced Current Transient Spectroscopy (PICTS) and Photo-Deep Level Transient Spectroscopy (P-DLTS) were utilized, the former of which provides information on the all existing deep levels without distinguishing between majority and minority charge carrier traps while the latter reveals only the majority carrier ones. They are, thus, powerful tools when complementarily used.

Results and discussion

Figure 1 shows I-V curves at different temperatures relevant to the Hitachi material and, in the inset, the Arrhenius plot obtained from these curves at a reverse biasing V_a = - 5 V. Activation energy E_a , calculated from the plot slope, indicates that the transport properties in this temperature range are controlled by the dominant donor defect EL2 with level energy (E_c - 0.78) eV.

From capacitance-voltage characteristics performed at T = 420 K (where the all EL2 defects were calculated to be ionized [1]) the total concentration N_{EL2} was obtained. This concentration is 1.4 $\times$ 10^{16} cm^{-3} in Freiberger material and doubles to 2.9 $\times$ 10^{16} cm^{-3} in Nippon, going through 2.2 $\times$ 10^{16} cm^{-3} in Hitachi with only a small increase (0.3 $\times$ 10^{16} cm^{-3}) after implantation. It is to remind that similar doubling in N_{EL2} was calculated by Look [2] to change the equilibrium Fermi level E_F very little. From the thermionic leakage current density through the Schottky contact, measured from the I-V curves, the

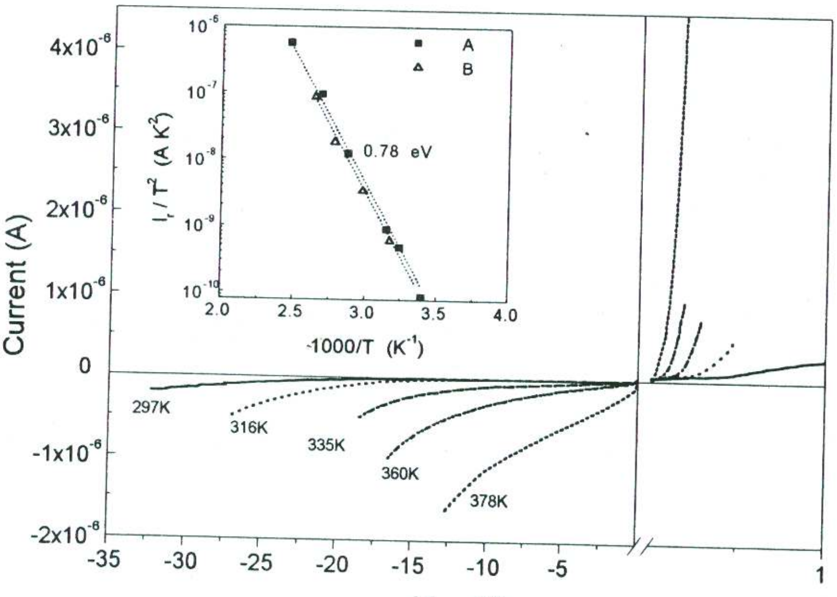

Fig. 1 Current-voltage characteristics at different temperatures of the Hitachi B substrate. In the inset the Arrhenius plot (deduced at V_a = -5V) shows that the transport properties are controlled by the midgap level EL2 at (E_c- 0.78) eV.

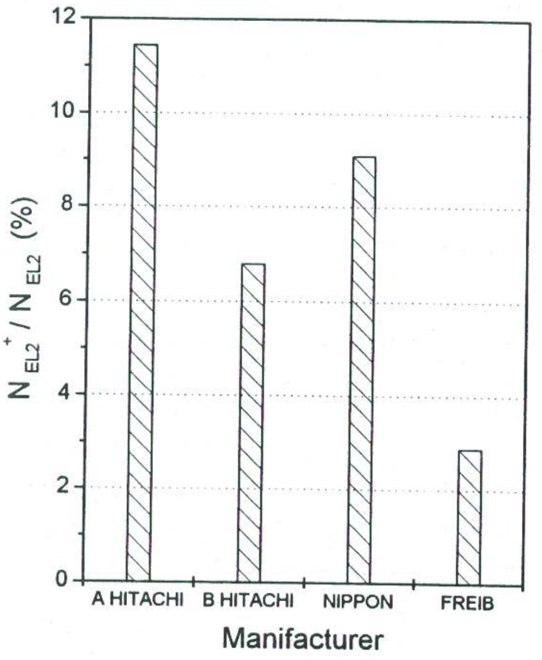

Fig. 2 Histogram of the ratio between the density of the ionized EL2⁺ and EL2 defects in the different materials investigated.

concentration N_{EL2}^+ of ionized $EL2^+$ at room temperature was determined [3] and the ratio between the ionized and the total deep donor concentration was calculated. The histogram of this ratio for all the investigated materials is reported in Fig. 2. It is evident that the changes of the ratio N_{EL2}^+/ N_{EL2} from a substrate to another are much larger than the corresponding changes of EL2 above reported. Even though it is not possible to straightforwardly relate these values, this observation well matches Look's consideration [2] that defects "shallower than EL2 can swing the E_F position by large amounts".

To discover defects other than EL2, PICTS and P-DLTS were utilized, and many shallower levels with significant concentration (also on the order of 10^{15}cm^{-3}) and non-negligible capture cross section (i.e. 10^{-14}cm^2) were found [4,5]. Figure 3 shows a comparison of PICTS and P-DLTS spectra relevant to Nippon substrate, pointing out the usefulness of this comparison: the trap at 0.37 eV of the PICTS spectrum lacks in the P-DLTS one, meaning that it is a minority (then a hole) trap. Two P-DLTS spectra relevant to as-received and implanted Hitachi material are shown in Fig. 4 . From the comparison of the two spectra it emerges that the traps at 0.15, 0.24 and 0.37 eV are significantly multiplied in number by the implantation process, while the remaining two traps at 0.52 and 0.79 eV keep constant. These changes modify, in turn, the position of the equilibrium Fermi level E_F and, in turn, the compensation ratio of the material.

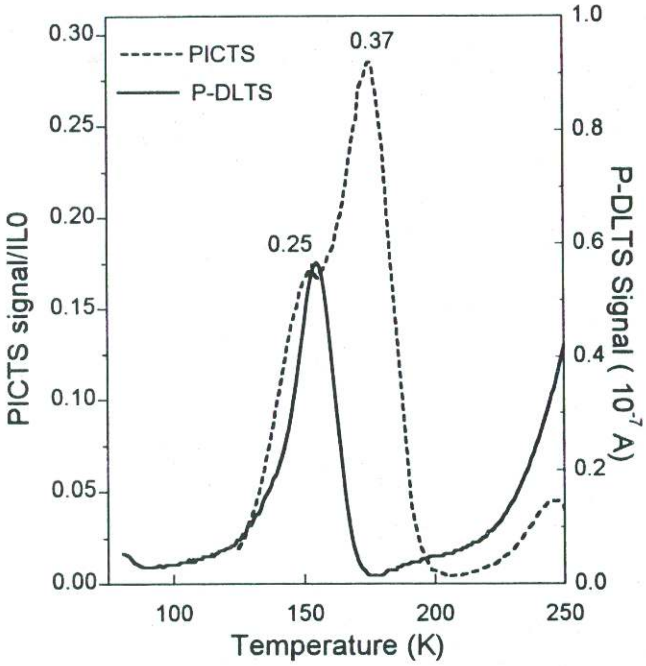

Fig. 3 PICTS (left hand scale) and P-DLTS (right hand scale) spectra relevant to the electron trap at 0.25 eV from the conduction band and to the hole trap at 0.37 eV from the valence band in Nippon substrate.

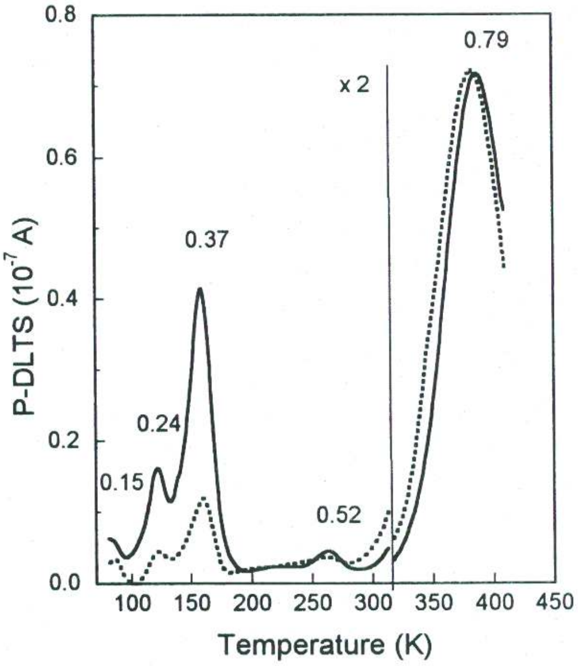

Fig. 4 P-DLTS spectra relevant to Hitachi B (dotted line) and Hitachi A (continuous line) samples.

It is worth noting that the overall comparison of the traps present in all materials investigated puts into evidence that most of them are everywhere present while a few of them are peculiar of specific material. Table I summarizes the results obtained. It can be seen that, for example, the electron trap at 0.18 eV is unique of the Nippon material while the hole trap at 0.41 eV is peculiar of the Hitachi material. At the same time, the hole trap at 0.56 eV, corresponding to the double donor state of the EL2 defect [6], exists in all substrates.

	0.15 *e*	0.18 *e*	0.19 *h*	0.24 *e*	0.25 *e*	0.37 *h*	0.37 *e*	0.41 *h*	0.52 *e*	0.56 *h*	0.79 *e*
Nippon		▒	▨		▒	▨	▒		▒	▨	▒
Freiberger	▒		▨	▒	▒	▨	▒		▒	▨	▒
Hitachi A	▒			▒			▒	▨	▒	▨	▒
Hitachi B	▒			▒			▒	▨	▒	▨	▒

Table I Summary of the traps detected. The shadowed cells signify the presence of the relevant trap and the symbols *e* and *h* mean that the corresponding trap is an electron or hole trap, respectively.

Conclusions

Semi-insulating LEC grown gallium arsenide wafers from different manufacturers, as-received and after ion implantation, has been investigated from a defective point of view by current-voltage and capacitance-voltage characteristics and spectroscopic methods, as well.

It has been found that the content of the charge carrier traps differ depending on the wafer source: most traps are common to all wafers but some of them, shallower than the dominant defect EL2, change from a kind of material to another. This is of major relevance when considering that any electrically active defects of a concentration 10^{15} cm^{-3} and shallower than midgap can produce large swings in the Fermi level E_F [7].

Therefore, it is necessary to include all these levels when it is needed to compare different SI GaAs substrates in view of the device performance and production yields.

References

[1] R. S. Tang, J. S. Blakemore, R. E. Kremer and K. M. Burke, J. Appl. Phys.**66,** 5428 (1989)

[2] D. C. Look, Semiconductors and Semimetals, **38**, 91 (1993)

[3] D. S. McGregor, R. A. Rojeski, G. F. Knoll, F. L. Terry, Jr., J. East and Y. Eisen, J. Appl. Phys. **75**, 7910 (1994)

[4] A. Castaldini, A.Cavallini, C. del Papa, C. Canali, F. Nava and C. Lanzieri, Inst. Phys. Conf. Ser.**149**, 55 (1996)

[5] A. Castaldini, A.Cavallini, C. Canali, C. Chiossi,C. del Papa, F. Nava and C. Lanzieri, Mat. Res. Soc. Symp. Proc. **373**, 523 (1996)

[6] J. Lagowski, D. G. Lin, T-P Chen, M. Skowronski and H. C. Gatos, Appl. Phys. Lett. **47,** 929 (1985)

[7] D. C. Look, *Electrical Characterization of GaAs Material and Devices,* (1989) (John Wiley & Sons, Chichester)