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MULTICHANNELS GaAs MMIC FRONT-ENDS FOR GAS CHAMBER PARTICLE DETECTORS

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Abstract
A front-end circuit composed of a high gain pulse amplifier cascaded by a threshold comparator has been designed for application in readout electronics of particle detectors. A prototype realized with a 8CH full custom chip in GaAs technology by GIGA foundry for application in gas chamber particle detector (RPC) is described. The chip exhibits a 0.2 mV minimum threshold, 150 MHz bandwidth and 50 mW per channel of power consumption.

Introduction
As it is well-known a widely diffused particle detector is the one using a gas chamber embedded between two high resistive electrode plates topped with an array of parallel copper strips, in order to collect the charge released by cosmic rays crossing the detector. The current pulses so generated in each strip is guided towards the front-end electronics. In the standard front end circuit the pick-up system is approximated to a capacitor; this approximation is correct if the collection charge time is larger respect to the propagation time in the pick-up system and the charge amplifier is needed. An RPC operating in avalanche mode produces typically a single signal of 5 ns FWHM and 1.5 ns time jitter, while the pick-up propagation time is 15 ns; in this case the signal has to propagate in the delay line to the front-end electronics located at the edge of the chamber. Since the source impedance is a resistor equivalent the impedance of the delay line, which corresponds to few ohms, the signal processing that minimises the noise source contribution is a voltage amplification.
The good time performance of the RPC detectors, utilized for the bunch crossing identification, required a large bandwidth because the large fluctuation in signal amplitude of the detector (100μV to 0.5 V) imposes a rise time of the order of the jitter RPC time.
The front-end circuit is a 3-stage voltage amplifier connected to a comparator. It is implemented in a full custom VLSI chip in GaAs technology. The amplifying section is composed by three non inverting - inverting - non inverting stages ac coupled through integrated capacitors. This topology was chosen to prevent a multistage amplifier from oscillations. A comparator is cascaded to the amplifying section to enhance the timing performance by decreasing the pulse rise and fall time. Finally an ECL buffer is used as output stage. The block diagram of the circuit is shown in Fig.1.
The amplifier frequency response is optimized for typical time structure of the avalanche signal according to the following conditions: 1) same risetime for the amplifier and input signals, which is nearly 2.5 ns; 2) minimum return-to-zero time for the output signal. The resulting frequency response has a maximum at 100 MHz and a 3dB bandwidth of 160 MHz as shown in Fig.2. The amplifier output is bipolar giving zero integrated charge thus avoidind a possible dependence of steady ouput voltage on the counting rate. The amplifier output signals for an avalanche-like input signal is shown in Fig.3, where the result of the SPICE simulation is reported. The comparator has a variable threshold which can be set at a minimum value of 50 mV giving adequate immunity respect to the noise, while a low percentage of input occurrences will be lost. The ECL output is capable of driving a few metre long 100 ohm flat cable connecting the front-end to the local trigger logic. The minimum comparator threshold combined with the amplifier gain fixes the minimum detectable signal amplitude at 0.17 mV.

Front-end prototype realization

The enormous effort currently invested by the electronic industry in the direction of high frequency technologies suggests that a very fast, high amplification front-end electronics will be easy to serialize, possibly in a custom version, to keep the cost of a large number of channels very low.

A two-channel full custom prototype chip of the front-end circuit has been already realized in GaAs technology, since the minimum serial-parallel noise at the given frequency band is obtained with the GaAs MESFET. This chip, which is a preliminary step before the 8-channel final version, has been already tested on board and mounted on the detector for the test H8 beam. The layout of the two-channel chip is reported in Fig.4, the chip size is 1x1.25 mm^2.

The IC front-end has been fabricated by the Triquint-GIGA foundry in GaAs technology. The MESFET process employed is the Triquint D1SS type with 0.6μm of gate lenght. 20 GHz cutoff frequency MESFETs have been chosen to obtain a high gain-bandwidth product amplifier, even if the bandwidth requirements are much lower. The circuit turned out to be very robust versus both temperature, power supply and processing variations.

Cross talk between channels and oscillations could easily be the result of parasitic couplings between circuit elements as well as package and bonding wires. Both commercially and technically it is a very good solution, if the die turns out to be stable. A great effort was devoted to guarantee stability in spite of a high gain [1,2]. The most important source of instability in a multi-stage high gain amplifier is the positive feedback of the signal through the bias feed lines. Care has been devoted to design the layout topology of the bias feed microstrip lines: each stage has separated feed lines, which are common to the corresponding stages of both the channels. In this way a layout of four-eight channels can be easily attained by top or bottom duplication.

Experimental results

In Fig.5 and Fig.6 the responses of the two channels to phase-shifted input pulses are shown. It can be seen that the outputs are independent from input pulse duration (Fig.5) and amplitude (Fig.6). The autoshaping capability of the circuit has been demonstrated. No cross-talk interference has been observed. The output pulse has a rise/fall time of nearly 300 ps.

In Fig.7 and Fig.8 the output signal delay as a function of the input signal amplitude and the equivalent threshold versus the input pulse width are shown.

The measured power consumption per channel of the prototype chip is 10 mW for the amplifier and 40 mW for the comparator.

References

[1] Y.Akazawa, N.Ishihara, T.Wakimoto, K.Kawarada, and S.Konaka: "A design and packaging technique for a high gain, gigahertz-band single-chip amplifier", IEEE Journal of Solid State Circuits, Vol SC-21, N°3, p.417, June 1986.

[2] R.Cardarelli, A.Di Ciaccio and R.Santonico: "Performance of a resistive plate chamber operating with pure CF_3Br", Nuclear Instruments & Methods in Physics Research, A 333, pp.309, 1993.

[3] F.Giannini, S.Ciorciolini, G.Orengo, "A 40 dB gain single chip pulse amplifier for particle detection", Proceedings of 26th European Microwave Conference, pp.86, Prague, Sept. 1996.

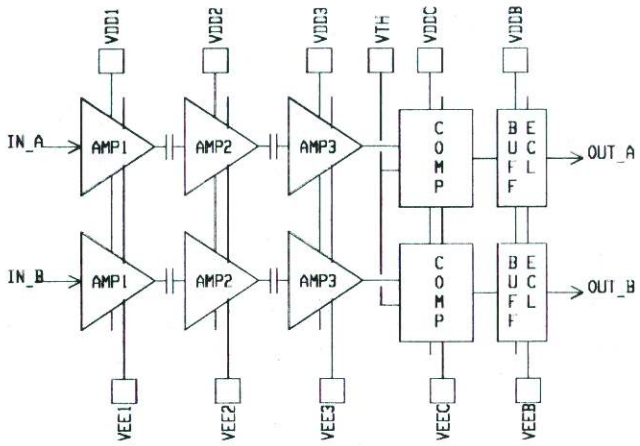

Fig.1. Block diagram of the two channel front-end

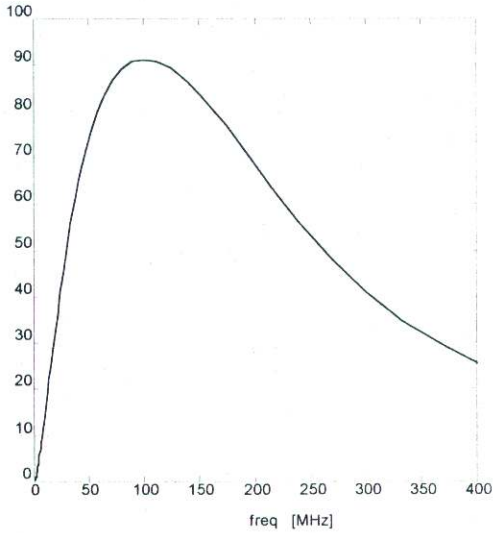

Fig.2. Simulated voltage gain vs frequency of the amplifier section.

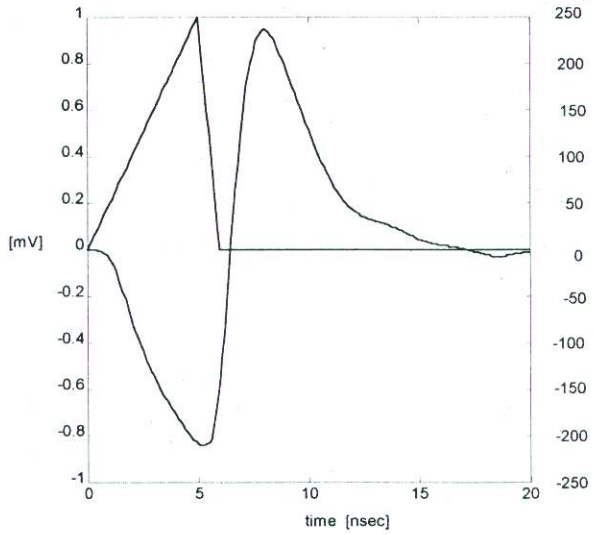

Fig.3. Amplifier response to a triangular-shaped input signal

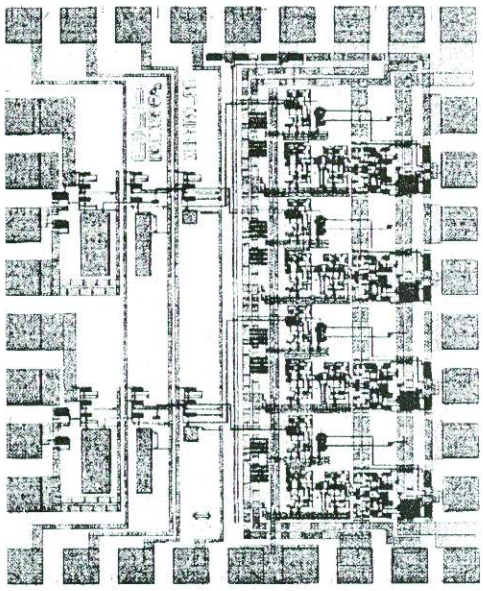

Fig.4. Layout of the monolithic two channel front-end.

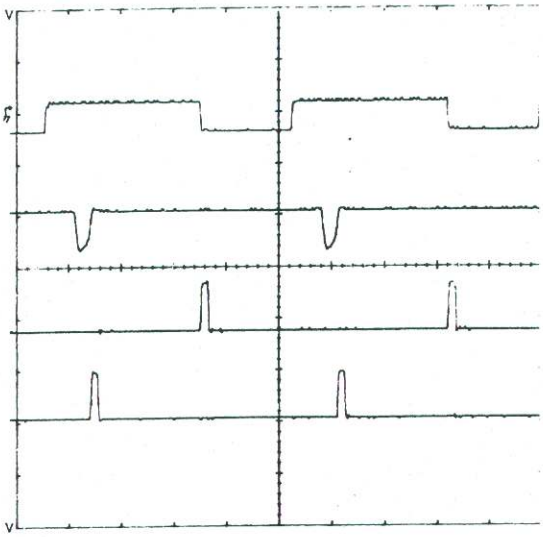

Fig.5. Two channels' response (C,D) to different dutation pulses (A,B)

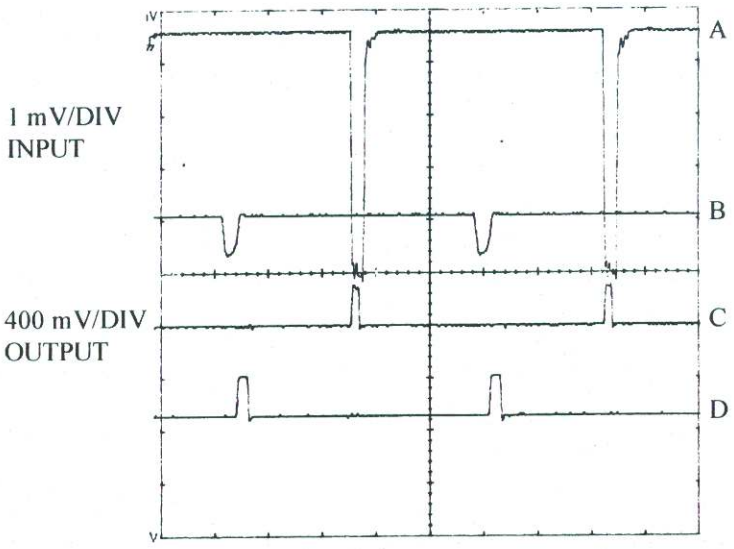

Fig.6. Two channels' response (C,D) to different amplitude pulses (A,B)

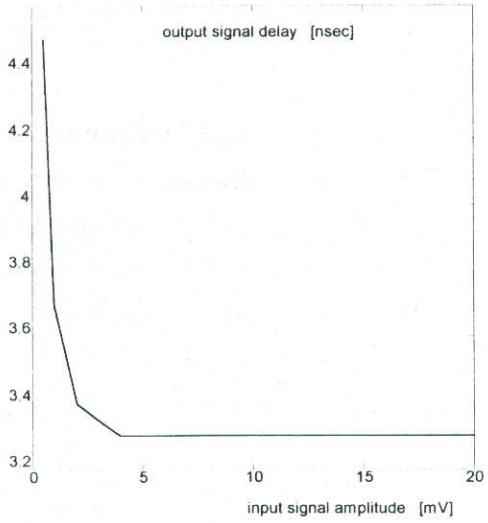

Fig.7. Output delay vs input signal amplitude

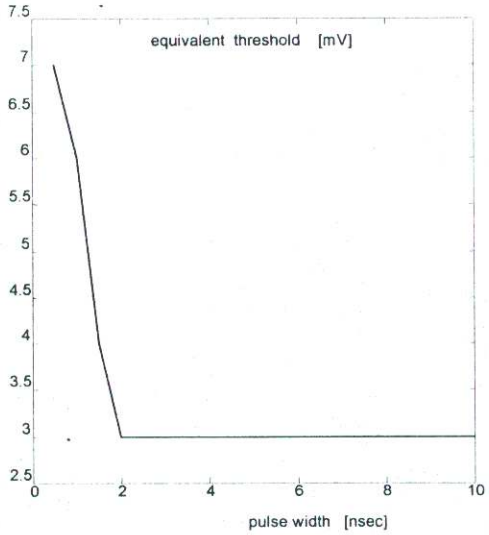

Fig.8. Comparator equivalent threshold vs input signal width