Digital SiGe-Chips for Data Transmission up to 85 Gbit/s

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***Abstract* — Design and performance of a 2:1 multiplexer and 1:2 demultiplexer IC up to 85.4 Gbit/s are presented. The chips are fabricated in an advanced SiGe technology with a cutoff frequency f_t of 200 GHz and a maximum oscillation frequency f_{max} of 275 GHz. With these two chips electrical data transmission at 80 and 85.4 Gbit/s could be achieved. In addition a pseudo random bit sequence (PRBS) generator IC is shown operating up to 80 Gbit/s and generating a 2^{31}-1 or a 2^7-1 pattern.**

I. Introduction

In the past few years first ICs for data transmission over 50 Gbit/s have been published mostly using InP-Technologies [1]. But also the first digital circuits fabricated in a SiGe technology have been published [2, 3]. We show in this paper that with the newest SiGe technologies [4, 5] digital circuits up to data rates of 85 Gbit/s are possible. This will offer new possibilities for increasing the data rate in transmission systems from now 40 Gbit/s to 80 or even 160 Gbit/s.

For demonstrating the capability of the speed up to 85 Gbit/s an 1:2 demultiplexer and a 2:1 multiplexer were designed. To show what kind of complexity can be achieved with this technology a 2^{31}-1 PRBS generator was developed. The circuits were fabricated in an advanced SiGe process with a current gain cutoff frequency f_t of 200 GHz and a maximum oscillation frequency f_{max} of 275 GHz [5]. The advantage of this technology is that it has a higher yield and more metallization layers compared to the most III-V technologies. This was very helpful for designing the 2^{31}-1 PRBS generator. Further SiGe can be integrated with other Si-based technologies as CMOS, leading to very high integration levels.

For packaging the circuits Rogers substrates with a cut out for the chip are used, and the chip is connected with ribbon bond wires to the grounded coplanar lines for the clock and data signals. To avoid additional cables and adapters, semi-rigid cables were directly attached to the Rogers board. This is an easy and cheap mounting technique and allows very short cables for the measurement. All chips have the same size of 1.2 x 1.6 mm^2.

II. 2:1 Multiplexer

Fig. 1 shows the block diagram of the 2:1 multiplexer. It consists of two input buffers, the multiplexer core and an output buffer. It is a straight forward design with no retiming. The power consumption is 690 mW.

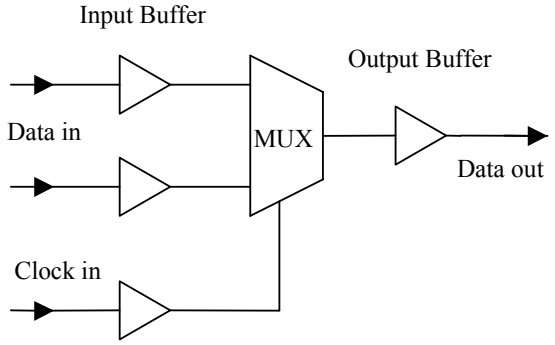

Fig. 1 : Block diagram of the 2:1 multiplexer.

For measurements the two inputs of the multiplexer are driven single ended each with one of the differential signal of a PRBS generator IC published in [3]. At one side a delay line was added. The output signal is measured with an oscilloscope (86110B from Agilent with the 65 GHz sampling unit 86116A and the precision time base unit 86107B). Fig. 2 shows the measured differential output eye diagram at 86 Gbit/s. The output amplitude is about 600 mV$_{pp}$, the RMS-jitter is less than 550 fs and the peak-to-peak jitter is about 4.1 ps. The eye-opening doesn't reach the rails, but this is not surprising, when the mounting with bond wires, the semi-rigid cables, the phase shifters to enable differential measurement and the 65 GHz bandwidth of the oscilloscope are considered.

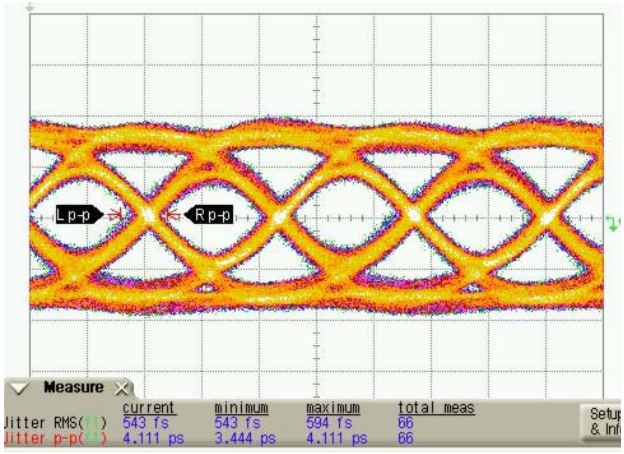

Fig. 2: Measured differential output eye diagram of the 2:1 multiplexer at 86 Gbit/s (scale: 5 ps/div, 200 mV/div).

III. 1:2 DEMULTIPLEXER

The 1:2 demultiplexer operates with a half rate architecture with two flipflops. The block diagram is shown in fig. 3. Each branch contains data input and output buffers. In one branch an additional latch is implemented to achieve the same phase for the two data outputs. The circuit is implemented in ECL and the power consumption is 1025 mW. The output buffers provide a differential signal of 500 mV_{pp}.

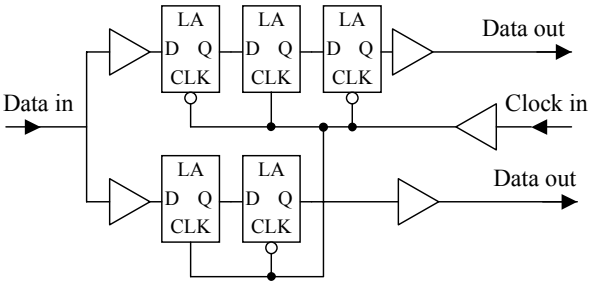

Fig. 3: Block diagram of the 1:2 demultiplexer.

IV. DATA TRANSMISSION

For demonstrating data transmission the output of the 2:1 multiplexer was connected to the input of the 1:2 demultiplexer. Fig. 4 shows the block diagram of the measurement setup. The multiplexer was driven with the two outputs of a 2^7-1 PRBS generator. One output was delayed by several bits. As the PRBS generator operates with the half rate clock, a frequency divider is used. The phase of the clock signal can be changed with the phase shifter optimising the clock to data timing at the multiplexer.

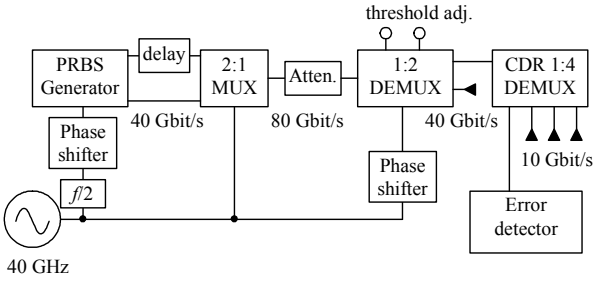

Fig. 4: Block diagram of the measurement setup for 80 Gbit/s data transmission.

As no error detector at 40 and 42.7 Gbit/s was available one output of the 1:2 demultiplexer was connected to a CDR-1:4-demultiplexer. Only two versions operating at 42.7 and 40 Gbit/s were available, thus only the data transmission at 80 and 85.4 Gbit/s could be tested. With the 1:4 demultiplexer the data stream is down converted to 10 Gbit/s (10.7 Gbit/s) where an error detector was available. With this setup error free data transmission at both data rates could be achieved, independent which output of the 1:2 demultiplexer is used.

By changing the phase of the clock signal with the phase shifter driving the 1:2 demultiplexer it is possible to measure the horizontal eye opening and by adjusting the threshold at the offset pins at the 1:2 demultiplexer the vertical eye opening could be measured. This measurement has been done with several attenuators at 80 and 85.4 Gbit/s. The results are shown in fig. 5 for the horizontal and in fig. 6 for the vertical eye opening. For the limit in all measurements a bit error rate of 10^{-9} was used. The figures on the right side of the plots indicate the used attenuator for the measurement.

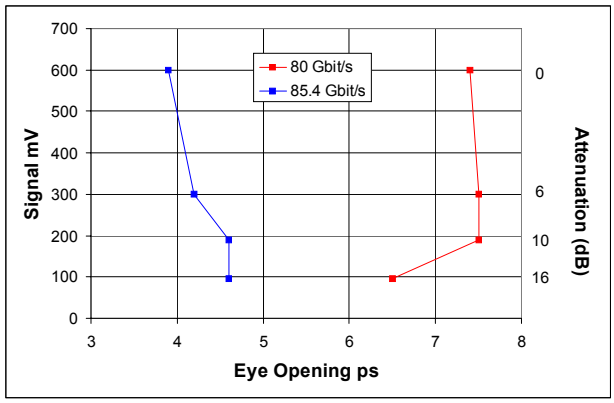

Fig. 5: Measurement of the horizontal eye opening at 80 and 85.4 Gbit/s at a bit error rate of 10^{-9}.

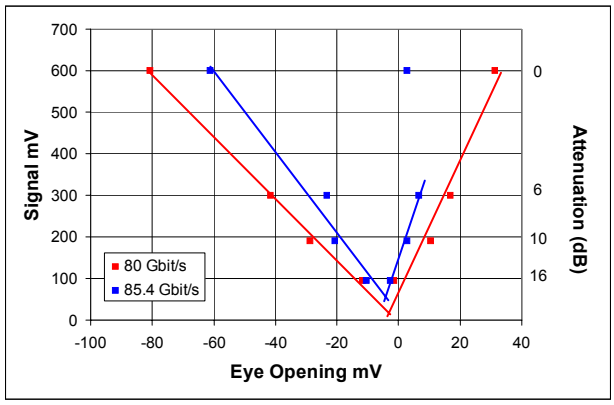

Fig. 6: Measurement of the vertical eye opening at 80 and 85.4 Gbit/s at a bit error rate of 10^{-9}.

The adjustment of the measurement setup at this high speed data transmission is very critical. For example an offset of the applied clock, unbalanced behaviour of the circuit or an unsymmetry in the mounting can lead to two different eye openings. So always at least two eye openings were measured. If there was only a small difference the results are averaged otherwise the setup was readjusted. This also reduces the errors, caused from phase changes through temperature drift from cables and circuits or movements from the setup by changing the phase of the manual phase shifters.

At 80 Gbit/s the horizontal eye opening is 7.4 ps and the vertical eye opening is 111 mV, and at 85.4 Gbit/s 3.9 ps and 64 mV respectively. With adding attenuators the vertical eye opening becomes smaller and can be extrapolated to the sensitivity of the data transmission, which is 40 mV for 80 Gbit/s and 70 mV for 85.4 Gbit/s. Whereas the points at 80 Gbit/s are on a straight line, this

is not the case for 85.4 Gbit/s. Especially the first measured point of the right branch at 85.4 Gbit/s doesn't fit at all and is not considered for extrapolating the sensitivity. In addition the horizontal eye opening in fig. 5 is becoming bigger when adding attenuators. So we assume that there are high reflections caused by the bond wires, which reduce the eye opening. With adding attenuators the reflections are getting smaller and improve the data transmission.

IV. PRBS GENERATOR IC

The circuit is based on a multiplexed linear feedback shift register similar to [3, 6]. Fig. 7 shows the block diagram of the PRBS generator IC. Each loop of the shift registers use 31 latches. The signals after the 28th and the last (31st) latch of the other shift register are fed into an XOR. The output of the XOR is than applied to the first latch. Because of layout constraints the output of the 29th latch is multiplexed to the PRBS output data stream at a bit rate, which is twice the clock frequency. As the latches operate at only half of the speed, the design of the latches, the clock-tree and the clock buffers is less critical and power can be saved. At the power up of the circuit all latches could be in the zero state. So a starter is applied to feed the latches with ones to start the bit sequence.

The use of 31 latches and the feedback after 28th and 31st latch generate a 2^{31}-1 pattern. In order to generate a 2^7-1 pattern switches are included. If the 29th and the 30th latch and 22 latches at the beginning of the shift register are bypassed the resulting shift register has only 7 latches with the feedback over the XOR at the 6th and 7th latch, generating a 2^7-1 pattern. For clearness this is not included in fig 7.

In the layout the placement of the latches has been done very carefully to minimize the line length to the XOR, to the switches for changing the bit pattern and to the multiplexer and optimize the performance of the circuit. The latches driving the XOR, the switches and the multiplexer are modified with a fast data output to increase the speed of the circuit. Also the timing is very critical especially for the clock applied to the multiplexer. Other publications are using a different clock for the multiplexer to adjust the timing [6]. The goal was to design a chip which is easy to use and can operate with only one applied clock signal. The advantage is, that the clock frequency and thus the output data rate can be changed without new clock alignment.

The chip size is 1.2 x 1.6 mm^2 and the power consumption is 1.7 W, resulting in a power density of 0.88 W/mm^2.

For testing only the clock signal has to be applied and the output is measured with an oscilloscope. At 40 Gbit/s a very nice and clean eye diagram is measured and shown in fig. 8 for the 2^{31}-1 pattern. The amplitude is 450 mV$_{pp}$ and the rise and fall time (20 – 80 %) is about 8 ps. A very small RMS Jitter of 380 fs and a peak-to-peak jitter of 2.2 ps was measured. Note that the jitter of the oscilloscope is included in this measurement.

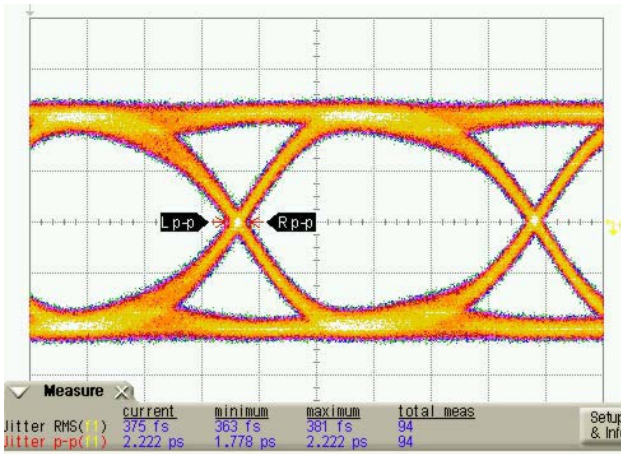

Fig. 8: Measured differential output eye diagram of the PRBS generator at 40 Gbit/s with the 2^{31}-1 pattern (scale: 5 ps/div, 100 mV/div).

Fig. 9 and 10 show the measured differential output eye diagram at 80 Gbit/s of the 2^7-1 pattern and the 2^{31}-1 pattern. The amplitude is about 450 mV$_{pp}$ and the RMS jitter of both patterns is less than 550 fs. The eye opening

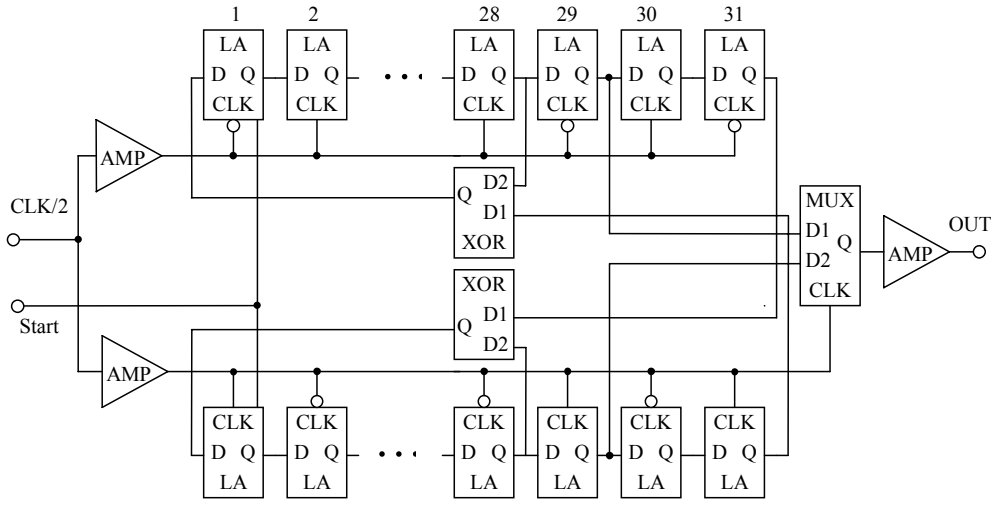

Fig. 7: Block diagram of the PRBS generator IC.

doesn't reach the rails, but also for this measurement the points mentioned earlier have to be considered. There is also nearly no difference of the eye diagram between the two patterns. The 2^7-1 pattern shows some more discrete lines because this pattern has fewer transitions compared to the 2^{31}-1 pattern.

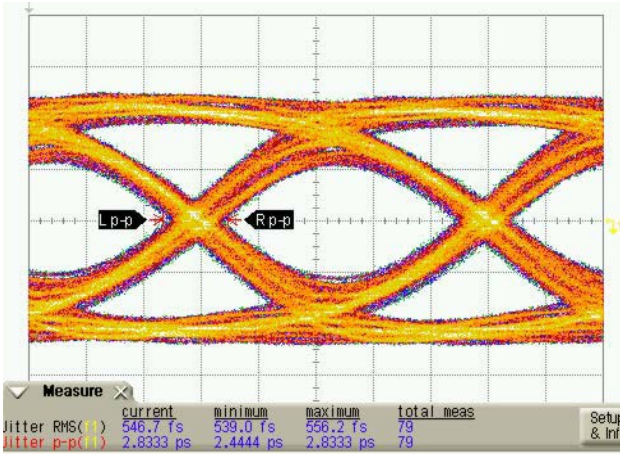

Fig. 9: Measured differential output eye diagram of the PRBS generator at 80 Gbit/s with the 2^7-1 pattern (scale: 2.5 ps/div, 100 mV/div).

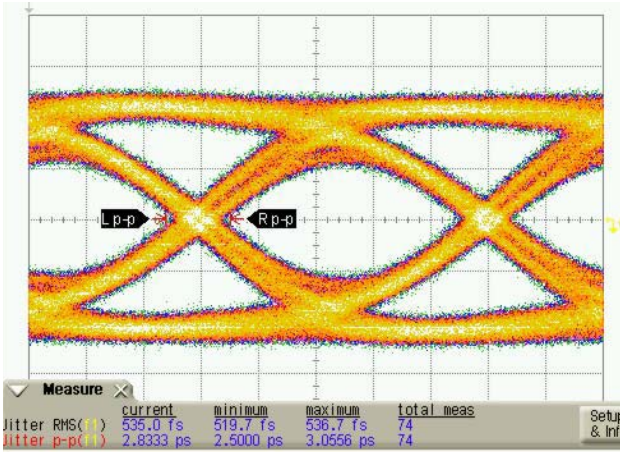

Fig. 10: Measured differential output eye diagram of the PRBS generator at 80 Gbit/s with the 2^{31}-1 pattern (scale: 2.5 ps/div, 100 mV/div).

VI. Conclusion

We have presented a 2:1 multiplexer and an 1:2 demultiplexer fabricated in an advanced SiGe bipolar technology. With these two chips we could build up electrical data transmission at 80 and 85.4 Gbit/s. In addition a PRBS generator IC was introduced operating up to 80 Gbit/s and generating a 2^7-1 and a 2^{31}-1 pattern. This circuit demonstrates not only the speed but also the complexity, which is possible with the new technologies.

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