A Ku Band Monolithic Power Amplifier for TT&C Applications

C.Florian[1-2], R.Cignani[2-3], G.Vannini[3], M.C.Comparini[4]

[1]University of Bologna, DEIS, Bologna, 40136 Viale Risorgimento 2, Italy, cflorian@deis.unibo.it;
[2]MEC s.r.l., Bologna, Viale Pepoli 3/2, Italy, corrado.florian@mec-mmic.com;
[3]University of Ferrara, Department of Engineering, Ferrara, 44100 Via Saragat 1, Italy, rcignani@ing.unife.it, gvannini@ing.unife.it
[4]Alenia Spazio, Roma , 00131 Via Saccomuro 24 , Italy, c.comparini@roma.alespazio.it

Abstract — **The paper describes the design of a 38 dBm monolithic power amplifier at Ku band. The amplifier has to be used as the final stage of the downlink transmitter of a TT&C system. A commercial power p-HEMT process capable of handling a power density higher than 1 W/mm of active area has been selected for the amplifier design. The power capability of this process makes it possible to integrate in a monolithic chip the functionality up today supplied by hybrid modules. Since the circuit is a space product, the attention is focused on reliability issues; therefore performances have to be matched imposing the devices to work at de-rated conditions respect to the process maximum ratings. In this perspective, the device channel temperature becomes a very tight design objective and has to be carefully controlled by means of a thermal simulator. The paper describes the three dimensional thermal model built to predict the devices thermal behavior in the environment of a finite difference thermal simulator. The design of the circuit is also described from the specifications to the final layout.**

I. Introduction

A 38 dBm monolithic power amplifier at Ku band has been designed using a commercial p-HEMT power process. The circuit is the final stage of an on-board transmitter. The application is the downlink of a commercial TT&C system (Tracking Telemetry and Command). This system provides the communication channel for the service commands of geostationary satellites. Up today this function has usually been provided by hybrid pre-matched FET mini-modules [1], delivered in hermetic sealed ceramic packages.

The availability of new p-HEMT and HBT processes [2]-[3] capable of handling very high power densities gives now the opportunity to synthesize those functions in a monolithic die, with obvious advantages in terms of cost, space, reliability and performance reproducibility. The actual maximum power level achievable with the mentioned power technologies for a monolithic amplifier at X and Ku band is around 40 dBm [4]-[5]-[6]: however, when giving those figures it is very important to specify which are the reliability constrains imposed by the application [7]. In our case, being a space product, a special emphasis is put on the reliability issue: the performances have to be reached imposing the devices to operate far from the process maximum ratings. In particular, the constrains that present the bigger challenge when the goal is the highest output power are the V_{DS} breakdown voltage and maximum channel temperature. Indeed, reliability is a function of the channel temperature [8]-[9]-[10]. A proper bias and dynamic load line has to be chosen to optimize circuit performances within the de-rated operating conditions. In this perspective, a simple electrical simulation is not enough and the use of a thermal simulator to control the device channel temperature is really mandatory [11].

II. Technology

The process selected for this application is a 0.35-µm power p-HEMT process from Triquint Semiconductors Texas [12]. This process is capable of handling drain bias voltages up to 12 V and offers more than 1 W/mm power density at 10 GHz. Passives include 3 thick-metal interconnect layers, TaN resistors, GaAs resistors, through-substrate vias and 3 different MIM capacitance densities. Also air bridges with minimal interconnect capacitance are provided. The very high cap densities (1200 pF/mm^2) in addition to the availability of three metal interconnect layers, drive to a very good packing density, that's to say very high RF power per mm^2 of chip area. The thick metal layer used for the signal lines enables low losses in the output combining networks to be achieved, thus enhancing efficiency and output power. A protective overcoat layer over the entire chip provides environmental robustness.

III. Specifications And Amplifier Design

The power amplifier specifications are listed in Tab. 1. There are no requirements on linearity because in this application the amplifier works typically at 1 dB of gain compression in CW.

Four power cells with 1800 µm of active area (12 gate fingers, 150 µm width) have been selected from the large choice of dimensions and patterns offered by the foundry to implement the final stage. The first stage consists of 2 devices of 1440 µm each (12 fingers, 120 µm gate width). The device samples have been measured and the I/V characteristics and S parameters reasonably matched the foundry design-kit model predictions. As described in detail in the next paragraph, a 3-dimensional thermal model of the active devices was developed in order to

Parameter	Design Objective	Unit	Notes
Operating frequency Band	10.7 - 12.7	GHz	full performances
Small Signal Gain (S21)	15	dB	min
Input matching (S11)	<-15	dB	
Output matching (S22)	<-10	dB	
RF output power	>38	dBm	@ 2 dB compression point
Gain Flatness	0.5	dB	
Power Added Efficiency	>35	%	@ 2 dB compression point
Maximum Junction Temperature	120	°C	
Max Operative Temperature at chip backside	70	°C	Self-heating effect is considered

TABLE I
POWER AMPLIFIER SPECIFICATIONS

simulate the operating channel temperature and select the right periphery and pattern to deliver the addressed power within the mentioned constraints.

Under small-signal conditions the gain of the first stage and the final one are 11.5 dB and 7.4 dB, respectively. The relative bandwidth of around 20% posed some challenges to fit the gain flatness specifications of 0.5 dB considering the little small-signal gain margin. Indeed, it has been necessary to introduce some lossy elements in the input and inter-stage networks to obtain a flat gain response across the bandwidth. For such a reason we have almost 2.4 dB losses in the inter-stage network. In the first stage a 3 dB resistor attenuator has been added in series with the input RF pad in order to improve the return loss value. This choice is useful also to guarantee the gain flatness requirement. In such a condition the desired small signal gain of 15 dB has not been achieved with a 2 stage topology. In fact, as depicted in Figure 1, S(2,1) is around 13dB. The output combining network introduces a 0.5 dB loss thanks to the thick process interconnect layer. In this way the efficiency was not affected too much.

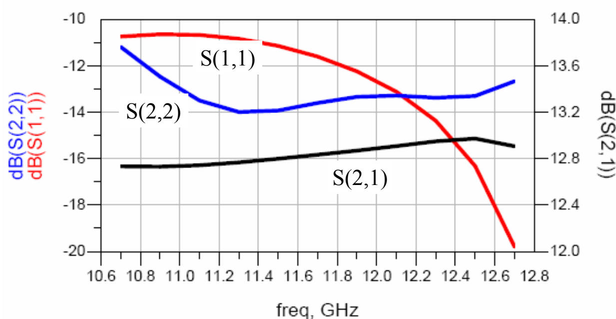

Fig. 1. Small Signal performances. S(1,1) and S(2,2) are lower than 10dB over all the band while the gain flatness is better than 0.3 dB. The S(2,1) degradation (only 13 dB) derives from a trade-off between the gain flatness and S(1,1) requirements.

The combining/splitting networks are simple tree binary structures and provide also the required matching. The matching is obtained with a combination of distributed (the combiner microstrip lines) and lumped (lumped capacitors) elements. The collector bias networks are λ/4 high impedance lines followed by decoupling capacitors. The gates are biased with 1 kOhm GaAs resistors.

Each cell has been stabilized for potential low-frequency instability with a lumped RC network in series with the gate [13]. The devices are unconditionally stable from 200 MHz upward.

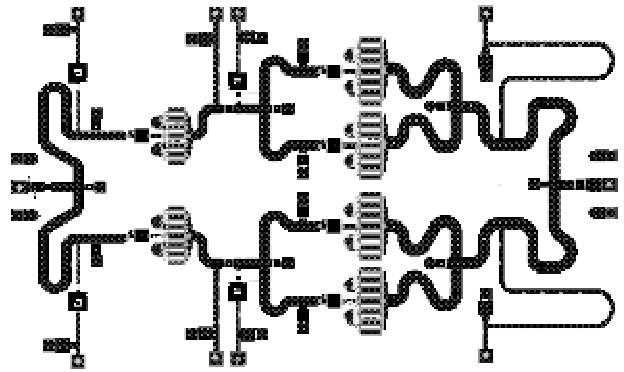

Fig. 2. Final Layout of the High Power Amplifier. Dimensions: 4.2 mm X 2.5 mm

Under compressed operating conditions each power cell of the final stage delivers 32.7 dBm for a total output power of 38.2 dBm (in fact 0.5 dB are lost in the output combining network). The devices are biased in class AB and the final stage exhibits a PAE of 54%.

The bias point is V_{DS}=8V and I_{DS}=167mA (Idss/3) for the final stage devices and V_{DS}=8V and I_{DS}=133mA for the driver ones. The good efficiency, along with the AB-class bias point, are chosen also to maintain a low channel temperature and match the constrains of de-rated operating conditions. Indeed, the process offers the possibility to bias with 12 V drain voltage and obtain in this way up to 1.2 W/mm power density, while for this amplifier the power density of the final stage cells is about 0.89 W/mm. However, under these constrains, we where able to keep the channel temperature under 130°, a value that doesn't perfectly match the starting specifications, but that guarantees a MTTF considered satisfactory (foundry reliability data).

The final HPA layout is depicted in Figure 2. The chip dimensions are: 4.2 mm X 2.5 mm and so the final power packing density is 0.62 W/mm^2.

In figure 3 the dynamic load line presented at the intrinsic device of each final stage cell is shown superimposed on the pulsed I/V device characteristic. The load line as well as the AB-class bias point have been chosen as a trade off between power, efficiency, channel temperature and de-rated electrical constrains.

In figure 4, the output power and the PAE of the overall amplifier at the frequency of 10.7 GHz, while figure 5 represents the final stage device junction temperatures at three different frequencies as a function of the input power.

In figure 6, the output power and efficiency of the amplifier are plotted as a function of the frequency at 1 dB compression point.

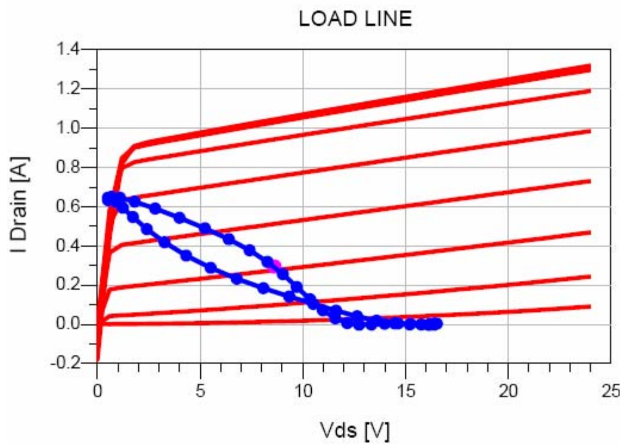

Fig. 3. Dynamic load line to obtain the addressed trade off between power, PAE, channel temperature. Quiescent point is highlighted.

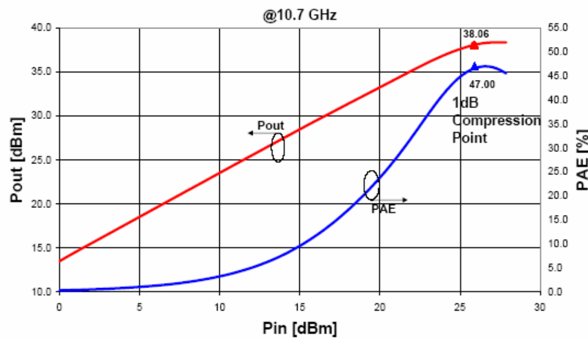

Fig. 4. HPA output power (dBm) and efficiency (%) at 10.7 GHz.

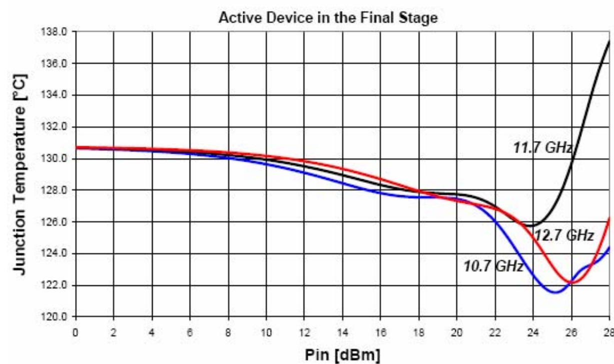

Fig. 5. Junction Temperature of the final stage devices as a function of the input power.

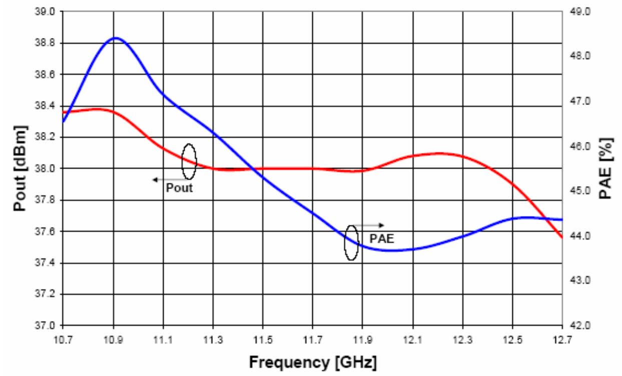

Fig. 6. HPA output power (dBm) and PAE (%) over the bandwidth of interests.

IV. 3D THERMAL MODEL

To accurately simulate the thermal behavior of the active device a thermal simulator based on a finite difference solver has been used (Harvard Thermal TAS, [14]). The three dimensional structure of the device has been defined as pictured in figure 7.

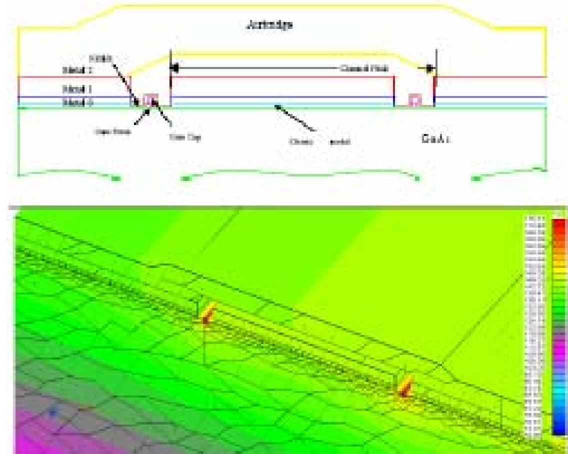

Fig. 7. Device structure defined for the implementations of the 3-D thermal model (up): for every layer, physical dimensions and thermal conductivity properties have been defined. Thermal simulation results (down): the refined temperature contours show a large temperature gradient localized in just under the gate area.

All the information about the detailed cross section dimensions have been provided by the foundry. The model takes into account the geometrical dimensions of all the process layers along with their non-isotropic thermal conductivities. The 100µm thick GaAs substrate thermal conductivity is also nonlinearly temperature dependent [15]. Air-bridges, surface metallizations, three different metal layers, T-structure gate material and GaAs substrate are included in the device model.

The model is completed defining also the Au/Sn 25µm thick solder and a 1.6mm thick Cu/W carrier. Once the 3D model is defined, volumetric heat sources are placed under each gate. Each final stage power cell has got 12 fingers with a gate width of 150µm: since each cell delivers 1.86 Watt with 54% PAE, the total dissipated power per cell is 1.19W, hence 0.1W per gate finger.

The volumetric heat source dimensions are: 0.35µm width (gate length), 0.06 µm thick and 150µm length (gate length); its position is 0.1 µm in the GaAs substrate under the gate. These information were provided by the foundry [16].

It is important to underline that the modeling of a submicron device poses a challenge because the power is dissipated very locally under the gate. Hence a suitable adaptive mashing of the 3D structure has to be chosen in order to have small size mesh elements under the gate, where submicron precision is required, and larger meshing in the GaAs substrate or at the carrier interface.

The simulations put in evidence a very local power dissipation with a large temperature gradient in the gate area. The final thermal resistance of the 12 finger x 150 um device has been simulated to be 56 °C/W (70 °C/W has been found out for the devices used in the driver stage).

The junction temperatures plotted in figure 5 have been evaluated by means of a suitable equivalent electro-thermal circuit for the modeling of the heat removal process. It consists of an electrical admittance modeling thermal conductivity and heat accumulation (resistance shunted with a capacitor): the current flowing in the circuit represents the rate of generated heat (dissipated power), while the voltage drop represents the rise between junction and backside temperature [17].

For such an application it is not useful to identify a correct value of the capacitor, since the amplifier works under CW.

V. CONCLUSIONS

The design of a monolithic power amplifier for TT&C applications has been described. The use of a new p-HEMT process, specifically tailored to achieve high power density and efficiency at X and Ku band, made it possible the design of a component that can replace the functionality of big and expensive hybrid modules based on the use of pre-matched FET chip coupled and matched by means of alumina hybrid combiners and wire bonding/chip capacitor technology.

A special emphasis has been given on the thermal characterization of the active devices for the control of the operating channel temperature, that is mandatory when space applications are addressed. A detailed thermal model of the power cells has been identified and a thermal simulator based on a finite difference solver has been used to simulate the maximum channel temperature.

The simulated results testify that some specifications have not been completely fulfilled. In particular, the input matching and the small-signal gain have been traded off for the gain flatness that is considered more important for the application. The design put in evidence the need for a third stage if one wants to obtain gain level, matching and gain flatness across the 2 GHz bandwidth.

As far as regarding the maximum channel temperature it is important to underline that if on one side we didn't perfectly match the 120° specification, the reliability data provided by the foundry guarantee the effectiveness of this amplifier for the addressed application.

This project has been founded by Alenia Spazio, Rome, Italy. We are waiting for the power amplifier foundry run.

REFERENCES

[1] J. Fukaya, M. Ishii, M. Matsumoto and Y. Hirano, "A C-Band 10 Watt GaAs Power FET", *1984 MTT-S International Microwave Symposium Digest*.

[2] H. Blank, K.J. Riepe, W. Doser, P. Auxemery and D. Pons, "Industrial GaInP/GaAs Power HBT MMIC Process" *GAAS2000 Symposium Digest*, pp.113-116, October 2000.

[3] A.P. de Hek and P.A.H. Hunneman, "Small sized high-gain pHEMT high-power amplifiers for x-band applications" *TNO-FEL* online database.

[4] United Monolithic Semiconductors, "X-band GaInP HBT 10 W high power amplifier including on-chip bias control circuit", *Microwave Symposium Digest, 2003 IEEE MTT-S International.*

[5] Qi Zhang, Steven A. Brown, "Fully Monolithic 8 Watts Ku-Band High Power Amplifier", *2004 MTT-S International Microwave Symposium Digest.*

[6] F. Murgadella, P. Coulon, C. Moreau, "Comparisons of technologies and MMICs results for military needs" - *23rd Annual Technical Digest of Gallium Arsenide Integrated Circuit (GaAs IC) Symposium, 2001*

[7] N. Le Gallou, J.Y. Touchais, J.F.Villemazet, "High Efficiency 45W HPA for space Application", *34th European Microwave Conference,Amsterdam, 2004.*

[8] William J. Roesch, "Thermo-Reliability Relationships of GaAs ICs", *GaAs IC Symposium Technical Digest 1988*

[9] H.S. Blanks, "The Temperature Dependence Of Compound Failure Rate" Microelectronics and Reliability, Vol 20, 1980, pp 297-307.

[10] W.J. Roesch, M.F. Peters, " Depletion Model GaAs IC Reliability" IEEE GaAs IC Symposium 1987.

[11] Jim Wilson, Ken Decker, "GaAs MMIC Thermal Modeling for Channel Temperatures in Accelerated Life test Fixtures and Microwave Modules", Semiconductor Thermal Measurement and Management Symposium, 1994. Proceedings of 1994 IEEE/CPMT 10th , 1-3 Feb. 1994

[12] "0.35µm power pHEMT 3MI" Triquint Semiconductor, http://www.triquint.com/prodserv/divisions/foundry/new/process_info.cfm

[13] A.P. de Hek, A. de Boer, T. Svensson, "C-band 10-Watt HBT High-power Amplifier with 50% PAE", *GAAS'01 Symposium Digest*, 2001.

[14] Harvard Thermal TAS, "Thermal Analysis Software", www.harvardthermal.com

[15] "Cindas Semiconductor Properties Report", Purdue University, 1988.

[16] "Thermal Characterization of Gallium Arsenide FETs" www.harvardthermal.com/products/TAS/papers/HTITriQuint/HTITriQuint.htm

[17] A. Samelis, D. Pavlidis, "Analysis of the large-Signal Characteristics of Power Heterojunction Bipolar Transistors Exhibiting Self-Heating Effects," IEEE Trans. on Microwave Theory and Techniques, vol. 45, no. 4, pp. 534-542, Apr. 1997.