OPTIMIZATION OF MILLIMETER FREQUENCY MULTIPLIERS BY INCORPORATION OF NUMERICAL MODELLING INTO CIRCUIT SIMULATORS.

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ABSTRACT

An integrated design philosophy which combines physical device modelling and circuit simulation is applied for the design of Schottky-diode frequency multipliers for millimeter-wave applications. The physical model is based on the drift-diffudion theory. It also includes self-consistently image force lowering, tunnelling transport, current dependent recombination velocity at the Schottky contact and impact-ionization. This coupling enables to concurrently optimize the device electrical and geometrical parameters together with achievable output power, conversion efficiency and the required loads at the specific harmonics.

INTRODUCTION

Varactor frequency multipliers play a vital role in developing all-solid-state power sources at terahertz frequencies. The key points in the progress in Schottky varactor frequency multipliers have been the enhanced physical insight into and optimization of Schottky diode varactor operation, Kollberg et al [1], the improvement in frequency multiplier analysis methods, Lipsey et al [2], Louhi and Räisänen [3], and in physical analytical Schottky diode models, Louhi and Räisänen [3, 4], Jelenski et al [5], as well as numerical physical device models, Lipsey et al [2], Grajal et al [6, 7]. In this paper we focus on the circuital aspects of Schottky-diode frequency doublers for millimeter bands. We employ the harmonic-balance method together with a physics-based drift-diffusion numerical device simulator. In contrast to previously published attempts, our simulator incorporates accurate boundary conditions for high forward as well as reverse bias, including impact-ionization, non-constant recombination velocity, tunnelling effects and image-force lowering [6]. The validation of the numerical simulator has been performed by comparison with experimental results obtained from submm-wave Schottky diodes fabricated at the University of Darmstadt, Krozer et al [8].

Performances of active devices are defined not only by their inherent characteristics but also for the circuits where they are embedded. Therefore, this coupling can be taken into account by including the numerical physical model into a circuit simulator [6], Zybura et al [9]. The integration of numerical simulators for active devices into circuit simulators will avoid the need of equivalent circuit model extraction or tedious measurements. This new philosophy accounts for the device-circuit interaction and provides another degree of freedom to improve the performance of circuits because they can be designed from both a device and a circuit point of view.

The influence of bias, input power level, loads at diferent harmonics, and impact ionization on the efficiency and output power of a $2 \times 50\ GHz$ doubler is discussed in detail. This doubler utilizes a Schottky varactor diode *D734* from the TU Darmstadt. The diode diameter is $\phi = 6.7\,\mu m$, the epi-layer doping is $N_D = 1 \cdot 10^{17}/cm^3$ and the epi-layer thickness is $t_{epi} = 350\,\eta m$ and its DC-breakdown

voltage is $V_{bd-DC} \approx -10V$.

The schematic circuit used for the analysis of multiplier operation is described in figure 1. Six harmonics are considered in these simulations, and the impedances of the higher harmonics (4th-6th) have been set to 0.0 Ω for both the resistive and the reactive components. The diode is always matched at the fundamental frequency.

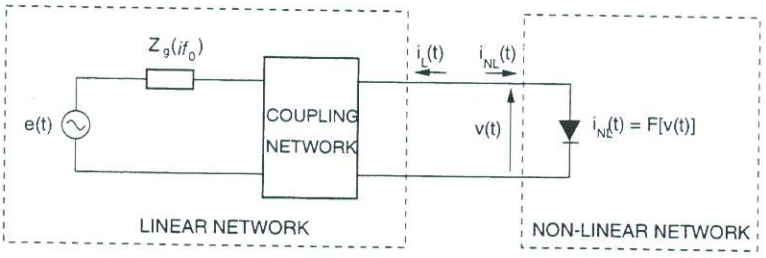


Figure 1: Physical Modelling and Harmonic Balance.

BIAS AND INPUT POWER LEVEL

Maximization of conversion efficiency in a doubler is obtained by selecting the bias and the input power level in order to provide maximum signal swing (maximum capacitance modulation) between the breakdown voltage V_{bd} and a forward voltage approaching the barrier height Φ_b. If the device is driven harder (mixed varactor-varistor operation), the output power increases but a resistive component of current (forward or reversed) will cause an increase of losses and the decrease in the efficiency. Figures 2 and 3 show the conversion efficiency, output power at the second harmonic, and DC current for $V_{bias} = -3, -7\ V$. Two different behaviours can be observed from these simulations. For $V_{bias} = -3\ V$ and increasing input power levels, positive voltage swings cause rectification, figure 6, and therefore positive DC current ($I_o > 0$). For $V_{bias} = -7\ V$, the rectified DC current arises as a consequence of impact ionization produced by negative semicycles, figure 7, and thus the DC current is negative. In both cases, the onset of the rectified DC current determines the maximum of the efficiency.

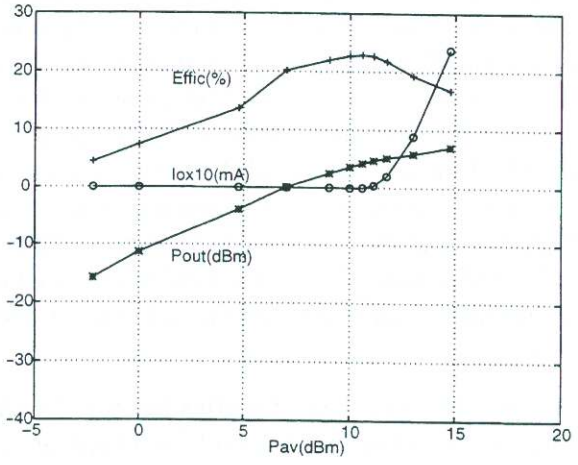


Figure 2: Efficiency, output power and DC current at $V_{bias} = -3V$.

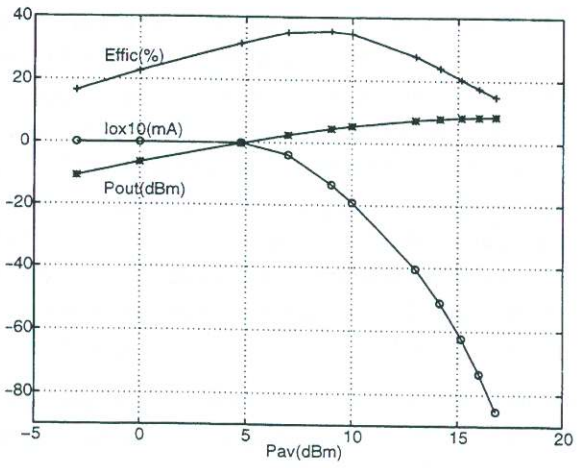


Figure 3: Efficiency, output power and DC current at $V_{bias} = -7V$.

A comparison among some characteristics for this doubler at $V_{bias} = -3, -5, -7\ V$ and different power levels appears in figures 4-5. The basic conclusions are:

- The input power level for maximum efficiency does not coincide with the power level for maximum output power.

- Both the output power and conversion efficiency increase with the input power level. Above the input power level which causes the onset of the rectified DC current, the output power level continues to rise, but the conversion loss also increases.
- The efficiency for $V_{bias} = -5, -7\ V$ is nearly the same for low input powers. The reason is that the capacitance for *D734* is nearly constant for voltages lower than $-5\ V$: no effective capacitance modulation takes place for the negative semicycles.
- Independence of the maximum output power with respect to the bias point and external loads. Therefore, if the available power is enough, the optimization for maximum output power must be the main goal. However, at increasing frequencies with limited power for pumping the diode, it is desirable to improve the conversion efficiency.
- Matching of the diode at the fundamental frequency is sensitive to changes with power, frequency and bias voltage at low input powers due to the high quality factor $Q(f_0) = Im[Z_g(f_0)]/Re[Z_g(f_0)] \approx 10 \ldots 20$. For high input power levels, the variation of the loads in weak ($Q \approx 4$) and our simulations show a strong increase of $Re[Z_g(f_0)]$ in accordance with [1, 3].

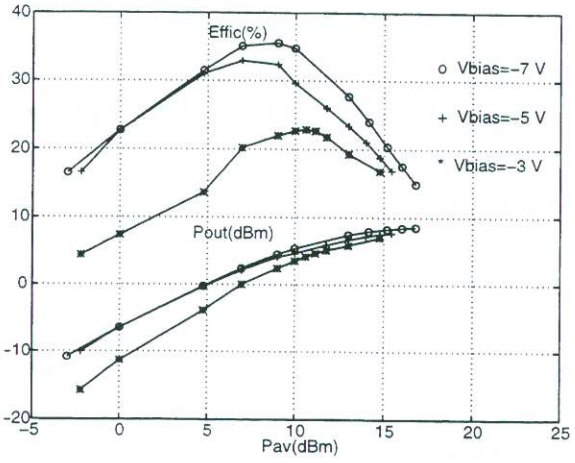


Figure 4: Efficiency and output power for different bias points at $2 \times 50\ GHz$.

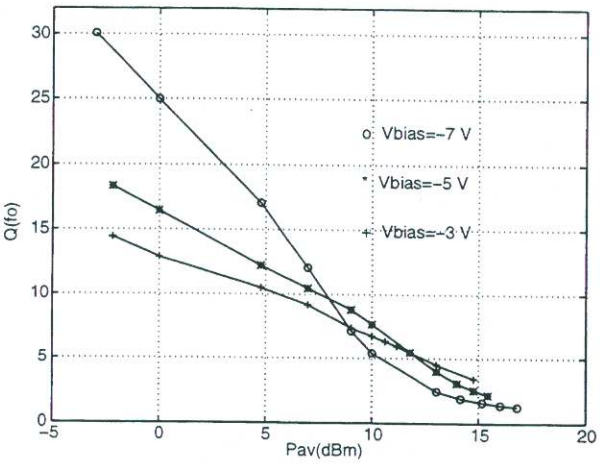


Figure 5: Quality factor (Q) vs. input power for different bias.

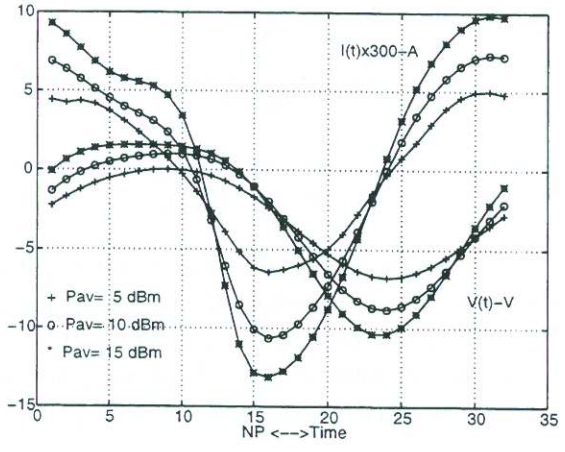


Figure 6: $v_D(t)$ and $i_D(t)$ for $V_{bias} = -3\ V$. 32 points per period (NP)

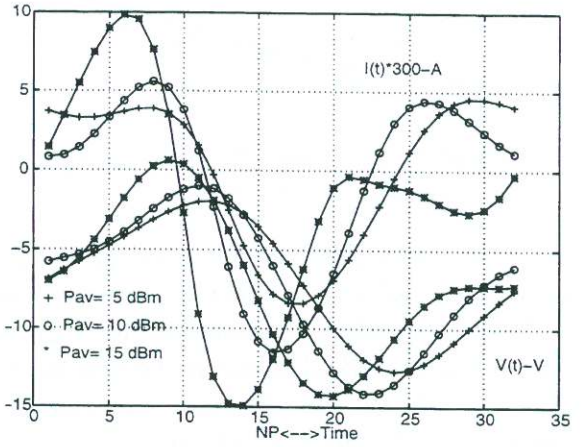


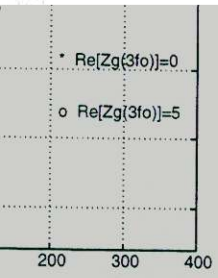
Figure 7: $v_D(t)$ and $i_D(t)$ for $V_{bias} = -7\ V$.

SENSITIVITY OF DOUBLER PERFORMANCE TO THE LOADS AT DIFFERENT HARMONICS

Table 1 shows the loads for the fundamental and second harmonic for maximum of efficiency at three bias points and an available input power of $P_{av} = 7\ dBm$.

Table 1: Maximum Conversion Efficiency for $P_{av} = 7\ dBm$

$V_{bias}\ (V)$	$\eta\ (\%)$	$P_o[2f_0]\ (mW)$	$Z_g[2f_0]\ \Omega$	$Z_g[f_0]\ \Omega$
-3	22.5	1.12	$25 + j100$	$26.9 + j185.3$
-5	31.2	1.56	$25 + j125$	$22.0 + j226.8$
-7	37.2	1.86	$25 + j150$	$23.0 + j275.5$



ficiency to $Z_g(3f_0)$
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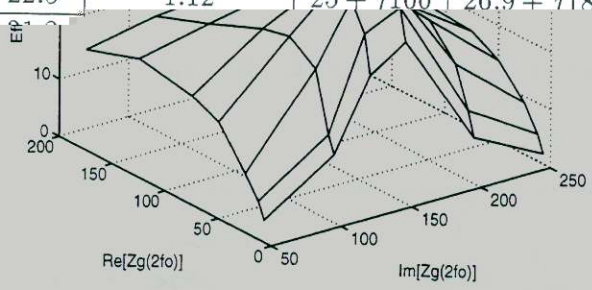


Figure 8: Sensitivity of the efficiency to $Z_g(2f_0)$ for $V_{bias} = -7\ V$ and $P_{av} = 7\ dBm$.

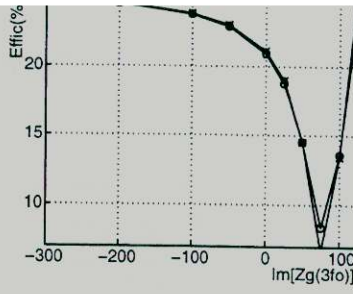
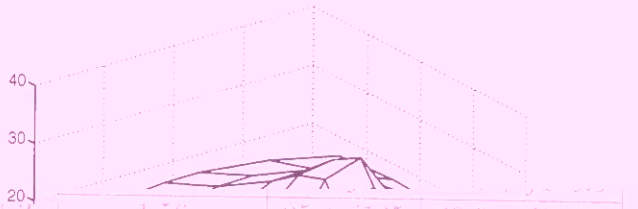
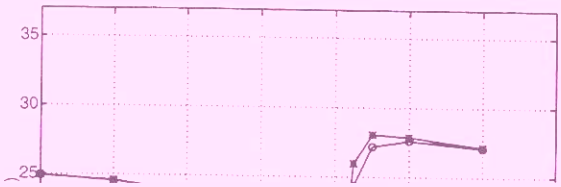


Figure 9: Sensitivity of the e for $V_{bias} = -5\ V$ and $P_{av} = 1$

The selected impedance of the diode is capacitive. The load at the third harmonic is a shortcircuit and the bias voltage is $V_{bias} = -7\ V$. The main conclusions are:

- When $Z_g(2f_0)$ differs from the optimum load $Z_{g-opt}(2f_0)$, the efficiency and the output power drops to very low values.
- Decreasing $Re[R_g(2f_0)]$ has a stronger effect than increasing it.





-5	31.2	1.56	$25 + j125$	$22.0 + j226.8$
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for the RF signal is considerably higher: $V_{bd-RF} \approx -15\ V$ at $f_0 = 50\ GHz$. This can be deduced from figure 7 where the voltage and current waveforms for $V_{bias} = -7\ V$ and $P_{av} = 5, 10, 13$ dBm are displayed. Therefore, the optimum bias point cannot be calculated only from DC considerations.

Some comments on the different operation regimes can be extracted from the results presented in the last sections. At low input power levels the operation of a varactor doubler is mainly determined by the embedding circuit and the choice for the DC operating point of the diode. In contrast, at high power levels the embedding circuit exhibits only minor contribution to the overall performance of the multiplier. Rectification by conduction ($V_{bias} = -3\ V$) or impact ionization ($V_{bias} = -5, -7\ V$) is responsible for output power saturation and conversion efficiency decrease at high output powers, figure 4. The highest efficiency of frequency multipliers is obtained in the transition region between low and high power regime [7].

VALIDATION OF THE SIMULATOR

We have selected two different Schottky varactor frequency multipliers for which measured and simulated data are available. A frequency doubler fabricated with a diode from the University of Virginia (*UVA6P4*) working at a fundamental frequency of 100 GHz [2] has been analysed with our simulator and the results are depicted in figure 10 (*Num. mod:* solid line with "+" symbols) [7]. They are compared with measurements (*Experimental*) and with simulated results from other simulators developed at the same University: *DDHB-fdm*, similar to the one developed by the authors *D*rift *D*iffuson simulator with *f*ield-*d*ependent *m*obility coupled to a circuit simulator based on *H*armonic *B*alance, *MCHB*, a Monte Carlo simulator for the device, *DDHB-am*, similar to *DDHB-fdm* but with the mobility calculated from Monte Carlo simulation. The diode parameters were taken from [2], the bias voltage has been set to $V_{bias} = -10\,V$, the loads at harmonic frequencies were set to $Z(nf_0) = (0 + j0)\,\Omega$ for $n > 2$, the diode is matched at the fundamental frequency, and $Z_g(2f_0)$ is optimized for maximum output power at each input power level.

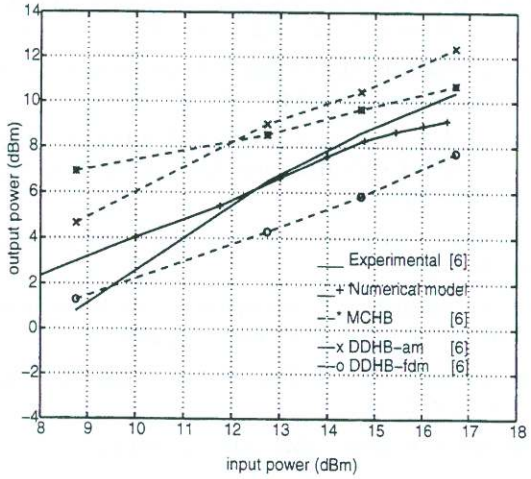

Figure 10: Validation: a 2×100 GHz doubler [2].

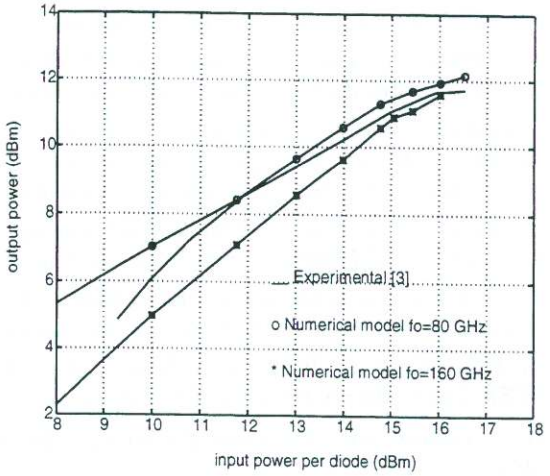

Figure 11: Validation: a 2×80 GHz doubler [3].

All simulators overestimate the output power and hence the efficiency of the doubler at power levels $P_{in} \leq 10\ dBm$ because of the perfect match of the diode at each power level in contrast to the experimental set-up, where the loads have been optimized for high power levels. Interestingly the Monte-Carlo harmonic-balance code *MCHB* [2] performs worst. In fact none of the simulations from [2] is able to simulate the correct power slope. Our model performs well for input powers above $P_{in} \geq 12\,dBm$ and is able to follow the slope of the measured results.

We have also compared our simulations with the measured data for a frequency multiplier using a similar diode at $f_0 = 80\,GHz$ [3], figure 11. This is a balanced-configutation doubler and it has been simulated as a direct parallel connection of two identical diodes. The agreement with measured data is very good. Simulations of the same arrangement at $f_0 = 160\,GHz$ also agree well at high

input power levels. The simulations presented in figures 10-11 for different frequencies and circuit structures have achieved very good agreement at large power levels, which demonstrates that the diode performance is the determining factor while the embedding circuit plays only a minor role in these operating conditions.

CONCLUSION

The developed device-circuit simulator has proved to be a very useful tool for the optimization of varactor frequency multipliers. It enables to account for the device-circuit interaction to improve the global circuit performances. It has also allowed to clarify the influence of impact ionization on output power saturation and conversion efficiency decrease at high input power levels.

ACKNOWLEDGEMENT

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