On-Chip GaAs-HBT Broadband-Coupled High-Bitrate Modulator Driver TWAs

C. Meliani, M. Rudolph, and W. Heinrich

Ferdinand-Braun-Institut für Hoechstfrequenztechnik (FBH), 12489 Berlin / Germany

Email: meliani@fbh-berlin.de

***Abstract* — A technique to connect two broadband GaAs HBT TWAs is presented. It covers the full range from DC to high frequency and is suitable for high bitrate (40 Gb/s) transmission circuits. This behavior is achieved by modifying the response of one TWA so that it compensates the low-frequency losses. This technique is truly broadband because it uses only elements which are directly connected, and thus is not limited at very low frequencies. Each single TWA delivers 8 dB of broadband gain at a 3dB cut-off-frequency of 26 GHz. Using this interconnect technique, a total broadband gain of 14.5 dB is obtained.**

I. Introduction

Without any doubt, distributed amplifiers show the best results for broadband-amplification building blocks. Such amplifiers are mostly based on cascode structures [1]-[2]-[3], which are very sensitive to ground paths and DC decoupling. As a consequence, DC input and output levels do not have many degrees of freedom and are almost fixed (e.g., to around 2 V and 6 V, respectively, for our GaAs HBT TWAs). Therefore, connecting two TWAs in series requires appropriate DC decoupling or level-shifting.

This is an important issue since, for a modulator driver module, one commonly needs at least two distributed amplifiers in series to provide the necessary gain [4]-[5]. Commonly, two amplifiers are connected with hybrid by-pass capacitors. In the broadband case, however, this does not work since a low series impedance has to be realized over the entire bandwidth down to very low frequencies. On the other hand, at 40 Gbps (and beyond) off-chip solutions are difficult because of the high frequencies at the upper end of the band. This is the problem addressed by this paper. The 40 Gb/s high output voltage capabilities of GaAs-HBT-based TWAs have already been demonstrated [6]. Amplifiers with 4 Vpp output swing and 12 dB gain have been realized. This paper presents results on the on-chip broadband coupling for modulator driver modules at 40 Gb/s and beyond. It focuses on HBT cascode based TWAs realized using the FBH GaAs coplanar MMIC process. However, the results can be applied to other technologies and concepts as well.

Our target was to connect two distributed amplifiers on-chip and over the whole bandwidth, each of them with around 8 dB gain and 26 GHz cut-off-frequency. The goal was to obtain double the amount of gain, and at least the same bandwidth. A gain of 15 dB with 29 GHz cut-off-frequency is finally demonstrated using a lumped diode shifting structure.

The paper is organized as follows: First, the process and modeling tools are described, which is followed by the sections on amplifier design, experimental results, and the discussion.

II. Process and Modeling Tools

In this section, the technology used and the transistor CAD model are described briefly. The HBT MMICs are fabricated on the FBH 4" process line. The epitaxial layers are grown by Metalorganic Vapor-Phase Epitaxy (MOVPE). For further details see [7]. Excessively high f_{max} values (beyond 170 GHz at V_{CE} =3 V) are achieved as compared to the more standard f_T values (36 GHz at V_{CE} =3 V). While f_T is mainly determined by the layer structure, f_{max} can be increased by optimizing the process. In our case, mainly base resistance R_B and base-collector capacitance C_{bc} are modified.

A customized CAD library containing both passive and active devices is used for circuit simulation. Key part is the FBH HBT model [8]-[9]. It includes partition of intrinsic and extrinsic base-collector diode, non-ideal base currents, self-heating, base-emitter and base-collector break-down, current-dependence of base-collector capacitance $C_{bc,intr}$, and collector transit time τ_c (i.e., velocity modulation and Kirk effect, which are responsible for the f_T and f_{max} peaking to be seen in Fig. 1).

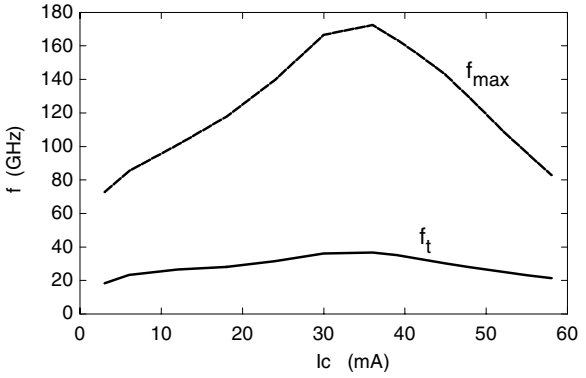

Fig. 1. Extracted values of f_T and f_{max} against collector current for a 3x30 μm^2 HBT at V_{CE}=3 V.

III. Circuit Design

A. *Single distributed amplifier*

The schematic diagram of the circuit is shown in Fig. 2. It consists of a five cascode-cell distributed

amplifier, which provides wide bandwidth and good isolation by canceling the Miller effect.

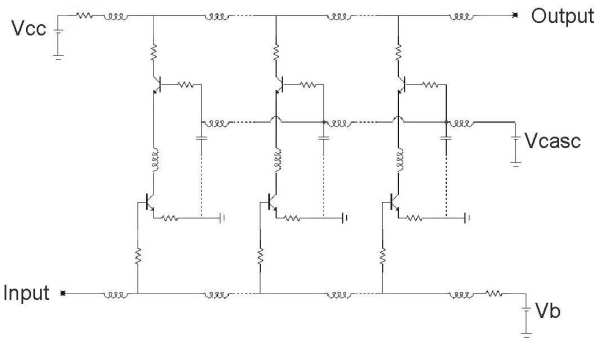

Fig. 2. Schematic diagram of a single TWA.

According to the principle of distributed amplification, equivalent transmission lines are formed using the transistor-capacitances at input and output plus the coplanar lines for the inductive part. The collector line is terminated by a 45 Ohm load, which is designed in such a way that it provides DC bias power without significant thermal effects. The backward waves on the input transmission line are absorbed in a 30 Ohm resistor, which also feeds the base bias of the transistors. The ground areas are interconnected along the transmission lines and around discontinuities to suppress parasitic modes and to ensure correct ground-current flowing.

Two points are extremely critical for the cascode structure: On the one hand, the decoupling of the base of the top transistor of each cell must be carefully designed because it can be responsible for instabilities on the output transmission line. On the other hand, the emitter-to-ground path is a key element for the broadband operation of the circuit. This length must be designed as short as possible. Because TWAs are physically long, the solutions is to favour the local loop (Fig. 2) so that the decoupling of each base of the top transistor is connected as shortly as possible to the emitter of the bottom transistor of the same cell, and then connected to the other cells. Thus, high frequency response can be improved.

B. DC level considerations

Because of the TWA topology described above the input and output DC levels are relatively fixed:

On the input, due to the short emitter-to-ground path, the DC level is fixed to a value around the knee voltage of the transistor plus the feed-back resistor voltage. In our case, the collector current of each transistor is between 20 and 40 mA, for feed-back resistor values around 20 Ohms. This leads to a mean base DC level between ~1.84V (1.44V+0.4V) and ~2.24V (1.44V+0.8V).

On the output line, the mean DC level is given as the bottom transistor emitter level + $2xV_{ce}$, in our case between 2 and 3V. This leads to a collector line voltage level between 4.4 and 6.8 V.

Thus, when connecting two TWAs in series, one needs to shift the base line level of the second TWA to around 6V, because of the very broadband operation (50 kHz at the low frequency to more than 20 GHz at the high end), the capacitors required for the decoupling of the emitter of the bottom transistor in each cascode cell will be too large to be realized on chip.

C. DC level shifter

The solution is to shift the DC level of the first TWA down to around 2 V with diodes. Using our approach, five diodes at least are needed which have a relatively high series resistance value at 40 mA bias current. At high frequencies, this is short-circuited by the junction capacitances (some 100 fF), and by an additional parallel capacitor of 10 pF (Fig. 3.).

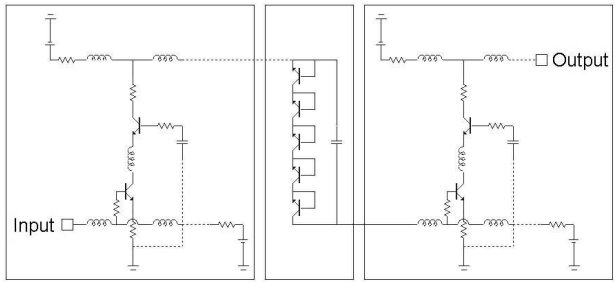

Fig. 3. Schematic diagram of the two TWAs and the shifting diode structure.

However, the series impedance of this structure shows high values at low frequencies (below 500 MHz), which decreases the total gain at these frequencies thus degrading the output eye-diagram. Exactly as for the decoupling of the bottom transistor's emitter, the value of the capacitor required to overcome this issue is too large to be feasible on-chip.

What is new about our approach is that we solve this problem by adjusting the low-frequency gain of the first TWA properly (increased by 4dB at low frequencies). The base-line termination resistor and the collector series resistance of each cell are modified such that the lack of gain at low frequencies is compensated.

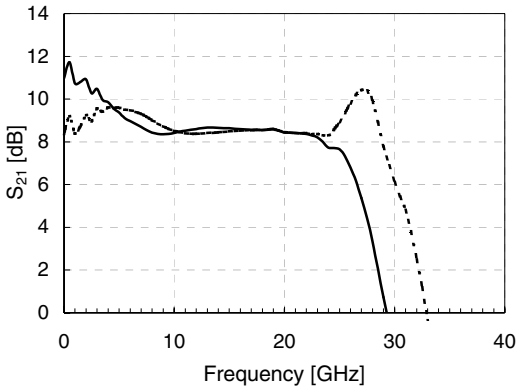

Fig. 5. Simulated S-parameters for the two TWAs. (--) with flat response, (-) with modified gain

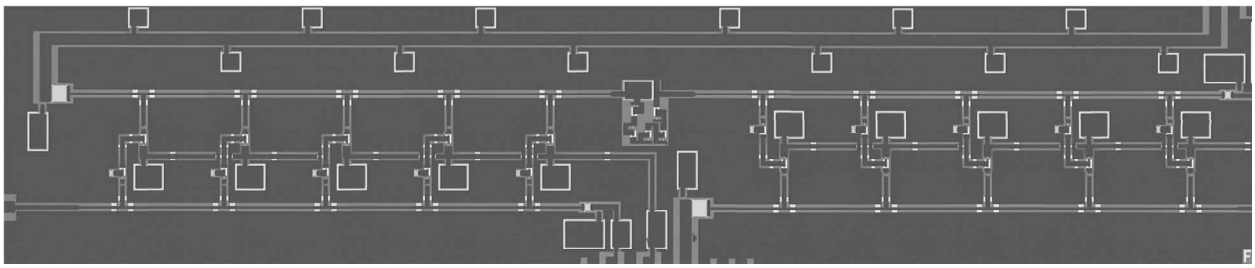

Fig. 6. Chip photo.

This solution is ideal in this case because it is a low frequency (to DC) concept. Thus it is effective over the entire bandwidth and especially at very low frequencies. Fig. 5 presents the gain of the modified TWA with around 50 Ohms base-line termination resistor and 20 Ohms collector resistance, and the initial version with 30 and 5 Ohms respectively.
A chip photo of the two-stage TWA realized is shown in Fig. 6. The long collector feeding line was carefully simulated and then decoupling capacitors were added all along up to the DC pad in order to keep its characteristic impedance low.

IV. Experimental results

The DC consumption of the circuit is 1400 mW for each TWA plus 250 mW for the shifter structure. The transistors are biased in their optimal regions around 35mA and 3V for collector current and V_{ce}, respectively. The collector voltage of the pre-amplifier is higher than for the output amplifier to provide the extra-current needed for biasing the diodes.

On-wafer small signal measurements show 15 dB gain and a 3 dB cut-off-frequency of 29 GHz (Fig. 7.). The two connected TWAs have around 8 dB gain and 26 GHz bandwidth each. The slight degradation in total gain (14.5 dB) compared with the sum of the gains of the two single TWAs (8 dB each) is due to the losses of the diodes. But a satisfactory flat gain is obtained using this structure, and the cut-off-frequency is even improved by the gain modification of the first TWA.

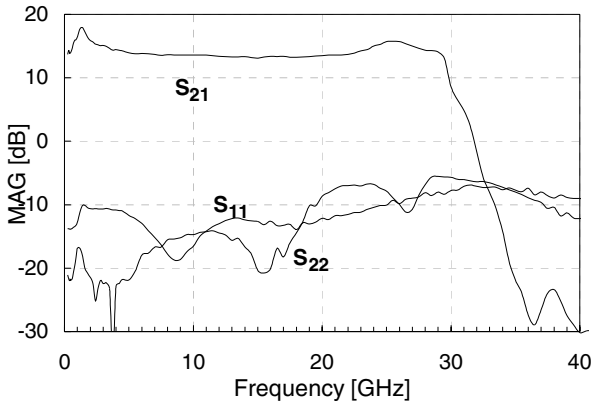

Fig. 7. Measured S parameters of the amplifier..

Input and output matching is better than -6 dB within the bandwidth. Under these measurement conditions, the f_T of the transistor was 36 GHz. Thus, the -3dB cut-off frequency of the amplifier reaches 78 % of f_T, which is a promising high value. This is mainly attributed to the exceptionally large ratio between f_{max} and f_T.

VI. Conclusions

A solution for the DC level-shifting problem in distributed cascode structures is proposed, using a diode shifter. The problems of low frequency losses and of unrealistically large on-chip capacitors is overcome by means of the base-line termination resistor and the collector series resistances. This seems to be the most realistic solution for such low frequency issues. Employing this approach, two cascode distributed amplifiers with 8 dB gain each and 26 GHz 3dB cut-off-frequency were successfully connected in series on a single chip.

Thanks to the gain modification of the first TWA, the cut-off-frequency is slightly improved. Thus, we obtain a broadband amplifier suitable for high-bitrate modulator drivers, using a standard GaAs HBT technology. Measured results demonstrate baseband operation with a 3dB cut-off-frequency of 29 GHz, and a broadband gain of 14.5 dB. This is a promising result for the design of monolithic modulator driver amplifiers for high-bitrate transmissions since it provides such a high gain on a single chip. Moreover, and even for such a gain value, a high ratio of 78% between -3dB cut-off frequency and transistor f_T is obtained.

Acknowledgement

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