Noise Assessment of AlGaN/GaN HEMTs on Si or SiC Substrates: Application to X-band Low Noise Amplifiers

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***Abstract* — This study regards the low noise properties of X-band GaN-based LNAs as well as its associated robustness. Devices are processed on epilayers grown on SiC or Si substrates. The HEMTs present very low noise properties with NF_{min} and G_{ass} close to 1 dB and 13 dB at 12 GHz. The robustness tests show that the component withstands power level up to 34 dBm. A two-stages X-band LNA is fabricated showing a noise figure of 1.7 dB with a gain of 20 dB at 10 GHz.**

I. INTRODUCTION

This paper describes the capability of AlGaN/GaN HEMTs for low noise applications. GaN-based devices constitute a suitable solution for low noise receivers without a limiter stage due to the GaN wide gap material properties and its HF low noise capabilities. In the first part, the growth process and the device fabrication are detailed. Then the high frequency characterizations main aspects are done as well as the device robustness tests. At last, the performance of X-band GaN-based LNAs are shown.

II. GROWTH PROCESS

In this work, we report on the use of GaAlN/GaN heterostructures grown respectively on silicon carbide[1] and silicon substrates for HEMT applications**.**

The GaAlN/GaN/SiC HEMT heterostructures were grown by Low Pressure Metalorganic Vapor Phase Epitaxy (MOVPE). They consisted of a GaN nucleation layer, followed by a 1 µm thick insulating GaN buffer layer, then a 27 nm Si doped GaAlN layer with 22% Al content, and finally a 3nm thick undoped GaN cap layer. The thickness of the high band gap layer of such HEMT structures, is lower than the observed critical thickness, leading to a pseudomorphic growth which was confirmed by a "mirror like" surface morphology and, at the atomic level, by high resolution X-Ray diffraction and TEM. AFM images of the surface of such layers revealed a RMS close to 0.3 nm associated with a defect density of $2.10^9 cm^{-2}$, and thus confirms the very good crystalline quality of the epilayers (fig. 1). The transport properties of such heterostructures were studied as a function of temperature from 100 K to 500 K. Hall mobility about 1700 cm^2/Vs at 300 K was obtained, associated with a sheet carrier density of 7.5 $x10^{12}$ $/cm^2$ and a sheet square resistance of about 600Ω. As observed for GaAlN/GaN HEMT structures grown on sapphire, increasing temperature from room temperature to 500 K reduces the electron mobility by a factor 2. Such dependence of the electron mobility with the temperature can explain the limitation in power and efficiency of the HEMT devices at large drain bias.

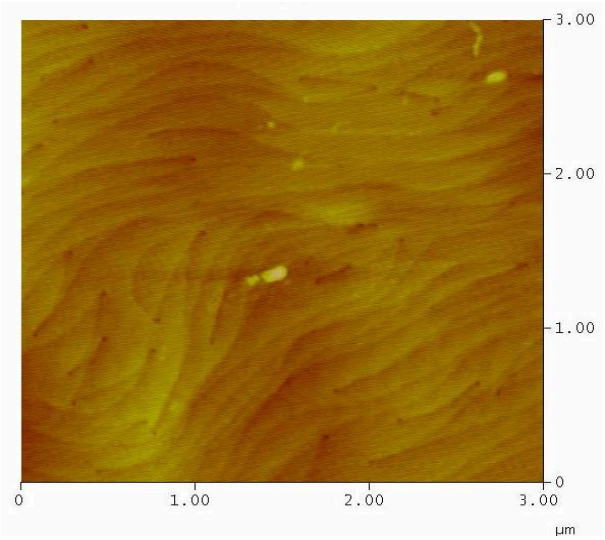

Fig.1 : AFM image of the HEMT structure

The layers on high-resistivity silicon (111) substrate are grown in a reactive molecular beam epitaxy system. The resistivity of the Si substrate is about 20kΩ.cm. The epilayer consists of a 50 nm AlN nucleation layer, a 0.5 µm GaN-AlN sequence and the HEMT structure with a 1.5 µm thick GaN buffer, a 30 nm $Al_{0.26}$ $Ga_{0.74}$ N barrier and a 1 nm GaN cap, these layers being undoped. The strain in the upper AlN layer is almost totally relaxed and the thick GaN buffer is grown compressively strained. This scheme reduces the extensive stress appearing during the cooling of the sample and permits the crack-free 1.5 µm thick GaN buffer layer to be grown. The

density of threading dislocations is in the range of 5-7 x 10^9 cm^{-2} as measured by plan view transmission election microscopy [2]. Hall measurement shows a sheet carrier density of 8 x 10^{12} cm^{-2} , an electron mobility of 1600 cm^2/V.s and a sheet square resistance of about 500 Ω/□ at room temperature.

III. DEVICE PROCESSING

The AlGaN/GaN HEMT processing begins by the alignment marks based on the Molibdenum metallization. Then, the ohmic contacts are formed from rapid thermal annealing of evaporated Ti/Al/Ni/Au (12/200/40/100 nm) metallization at 900 °C for 30s under nitrogen atmosphere. Typical results are commonly a contact resistance of 0.2-0.3 Ω.mm. The device isolation is performed even from mesa structures or ionic implantation. In the case of mesa, the active zone is defined from reactive ion etching using eight SCCMs of $SiCl_4$ gas, a radio-frequency power of 200 W and a pressure of 40 m torr. This operating procedure results in an etch rate of 20 nm/min. In recent TIGER laboratory processes, the device isolation is obtained from ionic implantation. The advantage is a planar structure which involves a easier interconnection processing. The process is based on helium multiple implantations at room temperature at different energies (30 to 190 KeV) based on different doses (10^{14} ; 5 x 10^{14} ; 10^{15} cm^{-2}). This operating procedure is efficient on HEMT structures. It was shown a temperature stability up to 700 °C involving a good isolation at high temperature when operating at high voltage. The T-shaped gate, based even on Pt/Ti/Pt/Au (20/25/25/300 nm) or Mo/Au (50/300 nm) metallization is defined using electron-beam lithography.

The gate lithography is based on a bi-layer resist process followed by a germanium evaporation (5nm) making it possible an improvement of the charge flow and involving a good e-beam focus. Gate lengths of 0.15 µm and 0.25 µm are available. Fig. 2 shows the T-gate cross section obtained using a focus ion beam.

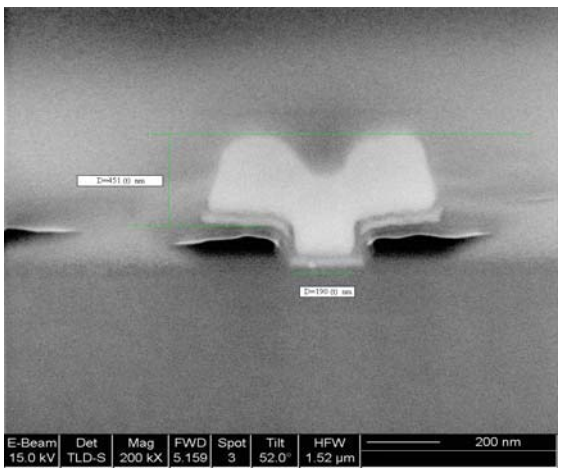

Fig 2 : T Gate profile obtained from FIB

Good Schottky contacts are usually obtained with a barrier height Φ_B = 1 ± 0.1eV associated to an ideally factor η = 1.5 ± 0.2 (Fig.3). Typical reverse current is 100 µA /mm at 50 V.

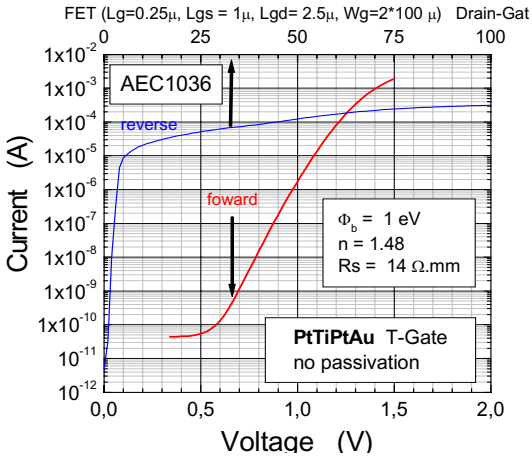

Fig. 3 : Schottky contact characterization

The device passivation is performed from SiO_2/SiNx deposition (100/50 nm) at 340°C. The device interconnection is based on Ti/Pt/Au (50/50/1200 nm) metallization and the last step is the fabrication of BCB air bridges.

IV. HIGH FREQUENCY NOISE CHRACTERIZATION

The main characteristics of the devices under investigation are summarized in table 1.

Subst.	gm_DC (mS/mm)	f_t (GHz)	f_{max} (GHz)	NF_{min} [(1)] (dB)	G_{ass} [(1)] (dB)
Si	257	46	100	0.93	13.7
SiC	230	47	102	1.1	13.0

Table 1. Main performance of 2x50x0.15µm² AlGaN/GaN HEMTs (Vds=10V, Ids =127 mA/mm for Si-based HEMT; Vds=10V, Ids=134 mA/mm for SiC-based devices). [(1)] @ 12 GHz

The noise parameters are extracted from noise figure measurement in the 6 – 20 GHz frequency range using the F50 method [3].

Figure 4 represents the minimum noise figure and available associated gain as function of the frequency. These devices present very low noise properties at the state-of-the-art level in term of NF_{min} and G_{ass} [4] for AlGaN/GaN on Silicon device. It should be noted that the NF_{min} in the case of GaN on SiC presents atypical variations in the GHz range due to trap mechanisms.

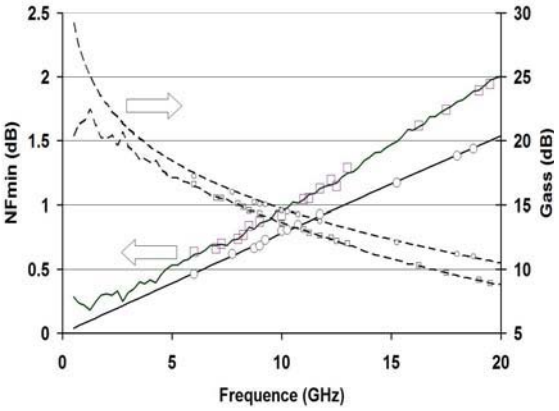

Fig. 4: Measured and simulated NF_{min} and G_{ass} versus the frequency. Circle: AlGaN/GaN on Si; Square: AlGaN/GaN on SiC; Lines: simulated data. (Vds=10V, Ids =127 mA/mm for Si-based HEMT; Vds=10V, Ids=134 mA/mm for SiC-based device).

A CAD-based linear model including the high frequency noise parameters is developed to design the one-stage X-band LNA. The validity of this model is demonstrated in Fig. 5 by comparing the calculated and measured S-parameters up to 50 GHz in a large range of bias conditions.

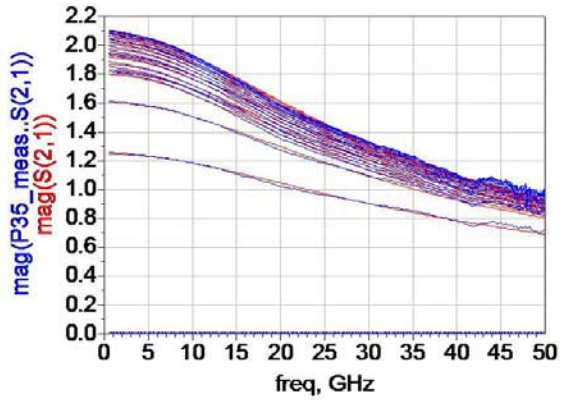

Fig. 5: Measured and simulated $|S_{21}|$ (in linear) of AlGaN/GaN on SiC HEMT; Vds=10V; Ids from 30 to 500 mA/mm

V. TRANSISTOR ROBUSTNESS TEST

GaN semiconductors provide many potential advantages for power microwave applications, for example increased input power level capability. Modules used in radar applications could benefit of this new technology in their Transmit and Receive path thanks to high power and low noise expected performances of GaN semi-conductors by suppressing the input protection circuit. The behavior of power handling of GaN should allow a reception amplifier to face high power electromagnetic aggression.

The robustness test is done on GaN transistors (SiC substrate) developed by TIGER laboratory for 3 different bias conditions: low noise 134mA/mm, switched OFF, 1dB gain compression. Input signal is made of a nominal CW X Band input signal (-10dBm) and a CW high power stress input signal. The step stress signal level is increased from 1dB to 1dB until device is break down (Fig. 6).

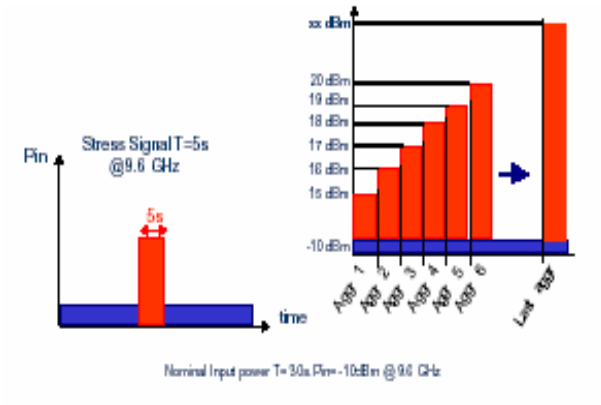

Fig. 6 : Input signal during Robustness test

While steps stress are performed, the more the input power level increases, the longer it takes to S parameters transistor to recover its original value. Time recovery is getting longer as input power increases.

Fig. 7 shows S_{21} parameter of SiC A1036 2423A prototype at low noise bias conditions during step stress performing:

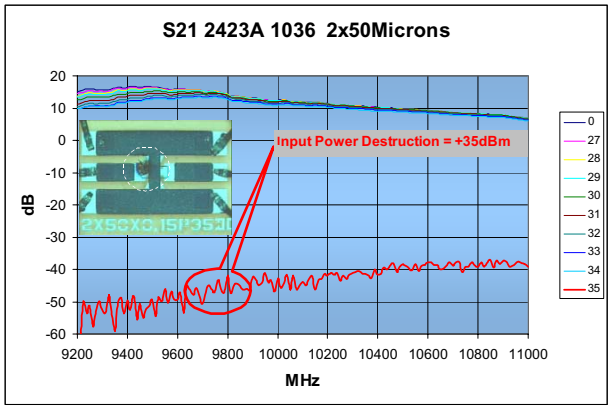

Fig 7 : S_{21} parameter for SiC 2423A dice 134mA/mm

Input power destruction for this 2x50 microns gate length dice is +35dBm. Damages are made of the blow of the gate metal and gate's finger destruction. (Fig.8) The transistor (4x75microns) was submitted to 1ms-1/1000 duty cycle for 5 seconds to evaluate the thermal effect contribution in the collapse. Measurements put on show that input power destruction is the same whether step stress is CW or pulsed: thermal has no effect.

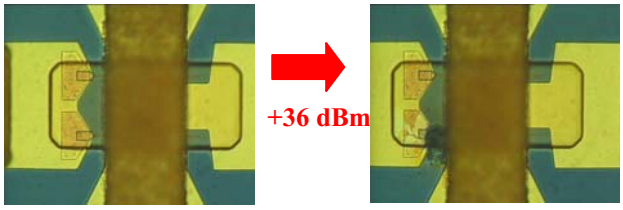

Fig 8 : Damaged after aggression on SiC GaN dice

For different gate developments, power aggression robustness increases for larger device periphery, as gain compression decreases. Time recovery is getting longer as input power increases. The following table is a synthesis of test aggression on GaN dices (Table.2):

Gate dvpt	Polarization	Power Destruction	W/mm
2x50	Minimum Noise	32,2	**17**
	Minimum Noise	36	**40**
	Compression 1dB	33	**20**
	OFF	35	**32**
2x100	Minimum Noise	32	**8**
	Compression 1dB	34	**13**
	OFF	36	**20**
2x150	Minimum Noise	36	**13**
	Minimum Noise	36,5	**15**
4x75	Minimum Noise	37	**17**
	Compression 1dB	33	**7**
	OFF	35	**11**
2x250	Minimum Noise	38,5	**14**

Table. 2: Synthesis of aggression test on GaN dices

VI. X-BAND LOW NOISE AMPLIFIER

Hybrid 1 stage and 2 stages X-band LNAs were simulated and fabricated using 4x50 µm GaN / SiC chips. The simulation is carried out using a table-based noise model issued from HF noise measurements. For the HEMT on SiC, the X-band minimum noise is reached at V_{ds}=10V and I_{ds}=28 mA for a single stage. The design is performed using ADS software. Fig. 9 represents the performance of this amplifier from 6 to 14 GHz. At 9.6 GHz, the noise figure is close to 1.25 dB with an associated gain of 10 dB. It is important to point out that at 7 GHz the noise figure is below 1 dB. Furthermore, it withstands a maximum input power of 37 dBm in the same operating conditions described in paragraph V.

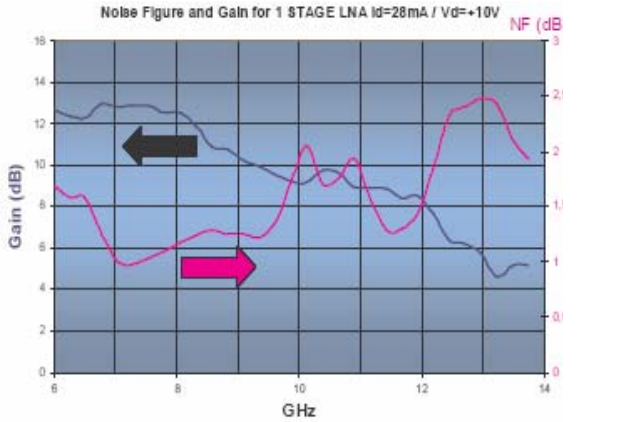

Fig. 9 : One-stage X-band GaN-based LNA, gain and noise figure measurements (V_{ds}=10V and I_{ds}=28 mA).

A two stages amplifier was also designed and fabricated. In the frequency range between 9.4 – 9.9 GHz, the noise figure is of 1.7 dB with an associated gain of 20 dB.

VI. CONCLUSION

This paper shows the very low noise capability for robust GaN-based LNAs operating in X-band from the fabrication of a two-stage hybrid demonstrator presenting a NF_{min} close to 1.7 dB with an associated gain of 20 dB at 10 GHz. Moreover, the maximum withstand input power on a one stage amplifier is 37 dBm. This shows clearly that the GaN-based is the material suitable for low noise receivers without limiter.

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