Thermal design of power GaN FETs in microstrip and coplanar MMICs

A.Angelini, M.Furno, F.Cappelluti, F.Bonani, M.Pirola and G.Ghione
Politecnico di Torino, Dipartimento di Elettronica, Corso Duca degli Abruzzi 24,
10129 Torino, Italy, +390161226405, annamaria.angelini@polito.it

***Abstract*— The paper presents a discussion on the thermal design of integrated power GaN devices. After a short outline of some critical thermal modelling issues, design guidelines are proposed on the basis of thermal simulations; the results presented suggest that for room temperature applications SiC substrate thinning (thus implying a microstrip process) is not mandatory from a thermal standpoint. This would open the possibility for coplanar GaN MMICs, already exploited for low-noise amplifiers, also in power circuits.**

I. Introduction

During the last few years, AlGaN/GaN HEMTs have been steadily increasing their RF power density, which is now above 20 W/mm and 30 W/mm for field-plate devices. Thermal management issues are therefore a key point in the development of power GaN FETs not only in sapphire-grown backside-mounted (BS) devices (whose dissipation capabilities are intrinsically inferior), but also in SiC-based FETs. Flip-chip solutions on AlN substrates have shown satisfactory thermal performances but are unsuited to monolithic integration [1].

An important issue concerns the viability of 6H-SiC as a heat sink material for high-power application. The room temperature thermal characteristics of SiC are better, or comparable, to those of many metals; however, the SiC conductivity is known to severely drop at even moderately high temperatures. Substrate thinning (i.e., replacing layers of SiC with layers of metal), presently seems to be the only solution to the problem. In the present paper, we exploit thermal simulation tools to show that the thermal behaviour of BS devices on comparatively thick SiC substrates is similar to the one of thinned devices (with realistic power density levels), unless the heat sink temperature is much higher than the room temperature. For room temperature devices a coplanar integrated process would be therefore thermally acceptable. High-temperature applications, on the other hand, would likely require substrate thinning or flip-chip mounting.

II. Integrated GaN FET thermal modelling issues

The thermal modelling of GaN FETs is not in principle different from FET modelling on other semiconductor substrates. A variety of numerical (Finite Element, Green's function based (GF) [2]) or analytical (see e.g. [3], [4]) models have been widely exploited to this aim. Closed-form thermal resistance (R_{th}) expressions for an infinite array of gate fingers on a multilayered GaN-SiC or GaN-sapphire substrate have been presented in [5], based on previous work [6] by the same authors. On the other hand, experimental data on the thermal resistance of GaN-based devices have been derived from electrical [7], [8] or thermal [9] measurements, carried out through different techniques by several groups. More recently, photocurrent spectrum-based (PHB) temperature measurements

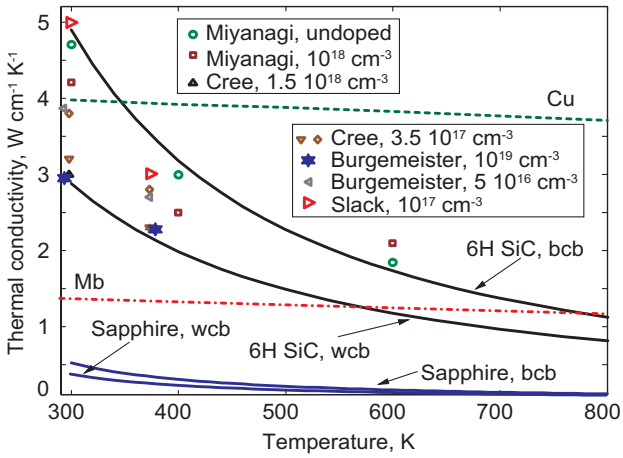

Fig. 1. Experimental thermal conductivity data and worst- and best-case models for 6H-SiC and sapphire; Cu and Mo mobility models are also shown.

have been proposed by Regoliosi et al. [10], and applied to the thermal characterization of GaN devices [11].

As well known, comparing thermal measurements and simulations is a difficult task. On the one side, measurements can provide detailed surface temperature maps, but are affected by a certain amount of spatial filtering, and sometimes by emittivity-related calibration problems (IR techniques); PHB methods should roughly provide information on the maximum temperature T_{max}, but also in this case some averaging is involved. The resulting thermal resistance is therefore defined either with respect to T_{max} or to some average temperature T_{ave}, the exact averaging area and weight not being precisely known. On the other hand, numerical simulation methods usually assume a known, often constant, dissipated power distribution typically located close or below the gate fingers [4], which leads to a non-uniform T distribution on the device active area; furthermore, analytical R_{th} evaluations almost invariably exploit solutions where the power injection area is isothermal, thus forcing the temperature profile on the gate fingers to be constant, and therefore the dissipated power to be more or less non-uniform. Several slightly different R_{th} values can thus be extracted from simulations according to whether this parameter is defined vs. the maximum temperature (R_{thM}), the average temperature on the power injection region (R_{tha}), or an imposed constant temperature on the active region (R_{thc}). In what follows, we will exploit Green's function based 3D simulations to evaluate R_{thM} and R_{tha}, while R_{thc} will be computed by the techniques in [5] which, for a single-layer substrate, provide results in fair agreement with the analytical approach in [4].

A further problem concerns the thermal nonlinearity of many substrate materials (namely SiC and sapphire). This

can be included in the thermal simulations through a post-processing stage based on the so-called Kirchhoff transformation, with some caveats on its use in non-uniform (e.g. layered) media, see [12].

Last but not least, a precise knowledge of the thermal properties of the material involved would be needed in order to carry out reliable measurements. In fact, the uncertainty introduced by this cause turns out to be significant, as the following review points out. Often, wide variations in thermal parameters observed by different authors could be traced back to material rather than characterization issues. Seen from a different standpoint, thermal conductivities can possibly be improved by material optimization.

Silicon carbide, which we will consider in the 6H polytype, exhibits exceptionally high room temperature thermal conductivity ($3 \div 5$ $\mathrm{Wcm^{-1}K^{-1}}$), higher than that of other semiconductor materials and comparable to those of some metals, as Cu, for example. The very early measurements of the high temperature 6H silicon carbide thermal conductivity are reported in [13], [14]. More recent 6H-SiC thermal conductivity experimental data are reported in [15], [16], [17] (CREE Research Inc.), and [18]. Experimental results point out a marked decrease of the conductivity with temperature, as well as with increasing doping impurity concentration. Anisotropy effects, amounting to a 10% increase in thermal conductivity perpendicular to the *c*-direction, are also observed on CREE samples at room temperature. The temperature dependence of the thermal conductivity was compared with theoretical models in [19] and [20]. Heat transport in silicon carbide is shown to occur through phonons, while electronic contributions are negligible. In this sense, SiC is equivalent to many metals at room temperature, but those are less affected by the temperature increase, since heat transport in metals is dominated by the electron rather than the lattice thermal conductivity. The main scattering processes responsible for the diminution of 6H-SiC thermal conductivity at high temperatures should be a combination of four-phonon and Umklapp processes. Such phonon scattering processes exhibit a temperature dependence of the form $T^{-\beta}$, with $1 < \beta < 2$.

Various models for the temperature behaviour of 6H-SiC have been proposed in the literature [15], [19], [21], [22], [23]; due to the spread of available experimental data, we decided to introduce a worst- and best-case bound model (wcb and bcb, respectively) for the 6H-SiC $k_{\mathrm{SiC}}(T)$, to be exploited in simulations. The model from Müller *et al.* [15] is used as wcb:

$$k_{\mathrm{SiC,wcb}}(T) = 4.517 \cdot 10^3 \cdot T^{-1.29} \ \mathrm{Wcm^{-1}K^{-1}}. \qquad (1)$$

The bcb model is taken from Ref. [23], and reads:

$$k_{\mathrm{SiC,bcb}}(T) = 4.9 \cdot \left(\frac{T}{300}\right)^{-1.5} \mathrm{Wcm^{-1}K^{-1}}. \qquad (2)$$

The related Kirchhoff transformations are:

$$T_{\mathrm{SiC,wcb}} = \left[\frac{-0.29 \cdot \theta + 1.29 \cdot T_0}{T_0^{1.29}}\right]^{-1/0.29}, \qquad (3)$$

and:

$$T_{\mathrm{SiC,bcb}} = \left[\frac{-0.5 \cdot \theta + 1.5 \cdot T_0}{T_0^{1.5}}\right]^{-2}, \qquad (4)$$

where θ is the apparent temperature, and T_0 is the reference one (in K).

Mounting	Substrate thickness, micron	GaN thickness, micron	Carrier	Lg, micron	Wg, micron	Gate spacing, micron	Gate periphery, mm	Thermal resistance, 300 K heat sink, C/W						
								Measured (device + carrier) [11]	Simulated (GF, R_{ma}) [2]		Simulated (GF, R_{mA}) [2]		Simulated analytical (R_{mc}) [5]	
									bcb	*wcb*	*bcb*	*wcb*	*bcb*	*wcb*
BS on SiC	400	3	MicroX II	1	100	55	1	20	8.9	11.5	9.5	12.4	8.8	12.7
BS on sapphire	330	3	MicroX II	1	100	55	1	65	34.5	46.4	39.1	53.1	45.9	59.5

TABLE I

DEVICE PARAMETERS AND MEASURED AND SIMULATED THERMAL RESISTANCE FOR SIC AND SAPPHIRE-BASED GAN DEVICES [11].

The same uncertainty affects measured thermal data for sapphire. Also in this case, a bcb and wcb model was extracted on the basis of the data in [24], [25], with room temperature thermal conductivities ranging from 0.35 (wcb) to 0.52 (bcb) $\mathrm{Wcm^{-1}K^{-1}}$; $(T-T_r)^{-1}$ ($T_r = 159$ K) temperature dependencies where exploited. Due to the small thickness of the GaN layer, the accurate value of k_{GaN} and its temperature behaviour turns out to be less critical (although a noticeable uncertainty also exists for this parameter, above all for thin epilayers); a commonly exploited value of 1.49 $\mathrm{Wcm^{-1}K^{-1}}$ was used (see e.g. [26], [27]). Models for the temperature dependence of copper (Cu) and molybdenum (Mb) thermal conductivities were also developed, with room temperature values of $k_{\mathrm{Cu}} = 4$ $\mathrm{Wcm^{-1}K^{-1}}$, $k_{\mathrm{Mb}} = 1.4$ $\mathrm{Wcm^{-1}K^{-1}}$; however, the conductivity variation is found to be almost negligible on a wide temperature range. Cu and Mb were selected as limiting cases of representative compound metal heatsinks, although other materials are available.

Conductivity models for 6H-SiC, sapphire, Cu and Mb are plotted together with available SiC experimental data in Fig. 1. We clearly notice that the metal thermal conductivity is almost T-independent; k_{Cu} is almost always larger than k_{SiC} for any possible model, while for Mb $k_{\mathrm{SiC}} > k_{\mathrm{Mb}}$ for $T < 570$ K (wcb) or $T < 770$ K (bcb). We would therefore expect that, for increasing channel temperature, the heat dissipation performances of SiC would drastically degrade, and, in particular, that dissipation through Cu were largely superior to dissipation through SiC for almost any channel temperature. Such conclusion would point out the need for substrate thinning. As discussed in the next section, simulated data provide a viewpoint not necessarily in agreement with such conclusions.

A possible way to gain better insight on the actual conductivity values of SiC and sapphire substrates is the comparison with experimental data. Some attempts to fit k_{SiC} values on thermal measurements were done e.g. in [5], with a best-fit value of 4.08 $\mathrm{Wcm^{-1}K^{-1}}$. Some data derived from PHB measurements by the Roma Tor Vergata research group [11] are presented in Table I. In Table I, W_g is the gate width, L_g the width of the thermal source; references for simulations are to the computational technique exploited. In the two cases considered, temperature measurements reveal a linear trend vs. power, thus suggesting an almost constant k. Assuming a mounting R_{th} approximately equal in both cases to 10 K/W, we could surmise a sapphire conductivity close to the wcb while the SiC conductivity is halfway between the worst and best case bounds, as in [5]. The considerable spread

of simulated data according to the simulation technique has to be remarked. Furthermore, trying to establish a typical value for k may be questionable if this parameter turns out to be technology-dependent. We therefore conclude that, despite the fair agreement achieved between measurements and simulations in the literature, model-based design criteria should allow for a considerable spread of R_{th} absolute values, while relative trends on the effect of physical parameters on R_{th} are probably easier to identify.

III. Thermal design guidelines of integrated GaN FETs

Optimum thermal design of integrated microwave FETs is based on well-known recipes, such as substrate thinning and increasing the gate-to-gate spacing. Increasing the gate width improves R_{th} only if the power density is decreased, but in what follows we will consider design at constant dissipated power density. At any rate, the layout degrees of freedom are indeed scanty for a given frequency range, since the total device width has to be small with respect to the operating wavelength and the gate width should be less than 100 μm in the X band (for a discussion, see e.g. [28, p.23]). In X-band applications typical gate-to-gate spacings are of the order of 50 μm. Therefore, only substrate thinning remains as a tool to reduce R_{th}; this also implies the impossibility to design power coplanar circuits owing to the resulting parasitic coupling with a closely spaced lower ground plane.

In what follows we consider a simple case study: a 10-finger GaN HEMT with a GaN epilayer of 2.5 μm on top of a 6H-SiC substrate. The gate width is 100 μm and the gate-to-gate spacing 50 μm. We analyze three possibilities:

1) the 400 μm substrate is backside-mounted on an ideal heat sink;
2) the substrate is thinned down to 50 μm and the etched SiC is replaced by a Mb layer;
3) same as in (2) but with a Cu layer.

For each case, we evaluate the average temperature of the central (hottest) fingers through the bcb and wcb approaches for dissipated power densities up to 20 W/mm. The results are shown in Fig. 2 while the related thermal resistances are shown in Fig. 3. The heat sink temperature is $T_0 = 300$ K.

From the above results we see that the BS mounted device with unthinned substrate is equivalent or even superior to the Cu-mounted thinned device up to 20 W/mm dissipated power if the bcb model holds, and much better than the Mb mounted device. In the wcb case, however, the thermal resistance is increasingly larger than in the Cu-mounted case, while is always lower than in the Mb-mounted cases. This result, apparently in contrast with the k values vs. T already considered, originates from the temperature disuniformity along the substrate depth, and to the fact that the lowest conductivity is found in the top SiC layers, always present also with thinned substrates. Clearly, a break-even point exists between pure SiC and Cu-mounted devices; this happens, with ambient temperature heat sink, for power densities of the order of 20 W/mm; if the heat sink is brought up to e.g. 80 °C this reduces to 10 W/mm approximately. Such results seem to suggest that, in ideal conditions, substrate thinning could not be as effective in reducing R_{th} as in other III-V compounds. This in turn would allow, at least up to a certain power density and heat sink temperature, to manufacture power coplanar (rather than

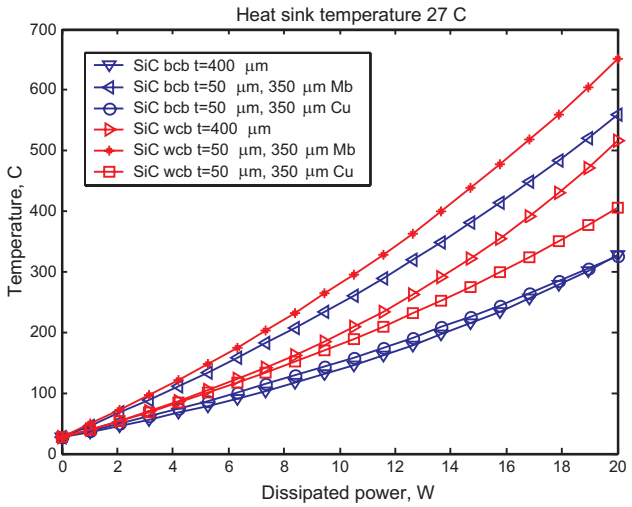

Fig. 2. Active region temperature for several GaN FET on SiC BS mountings and k models as a function of dissipated power.

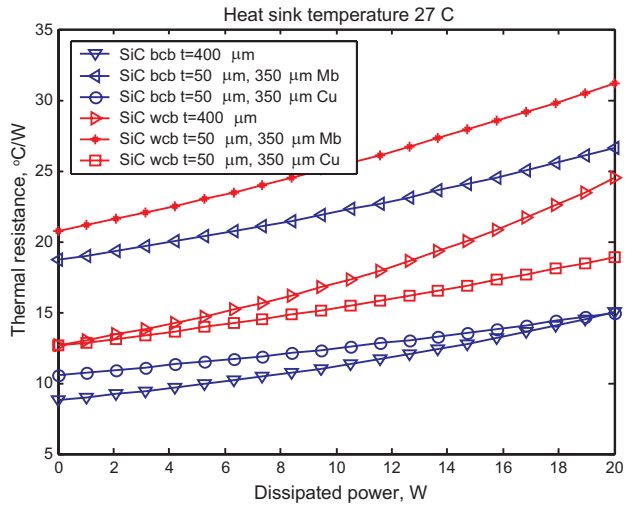

Fig. 3. Thermal resistance for several GaN FET on SiC BS mountings and k models as a function of dissipated power.

microstrip) MMICs. If the heat sink temperature is greatly increased, substrate thinning will become mandatory; e.g. for $T_0 = 300$ °C (573 K) and 20 W/mm power density, the simulated channel temperature with unthinned SiC substrate is as high as about 1200 °C (wcb) or 900 °C (bcb), against 700 °C for the Cu-mounted device.

The above picture is completely different for sapphire substrates; in this case the bcb and wcb temperature for a room temperature and 80 °C heat sink are shown in Fig. 4. The device parameters are the same as in the SiC case. Assuming a maximum active region temperature around 350 °C, the resulting maximumu acceptable power density would be of the order of 2-3 W/mm.

It is worth noticing that SiC substrates allow a fair amount of thermal decoupling between gate fingers already for gate spacings as small as 50 μm, as clearly seen from Fig. 5. Increasing the gate spacing would of course further reduce coupling but the asymptotic value of R_{th} so obtained is expected to be decreased no more than $\approx 30\%$. On the other hand, care should be taken in reducing the spacing since a large increase of R_{th} is expected. For sapphire, however, a

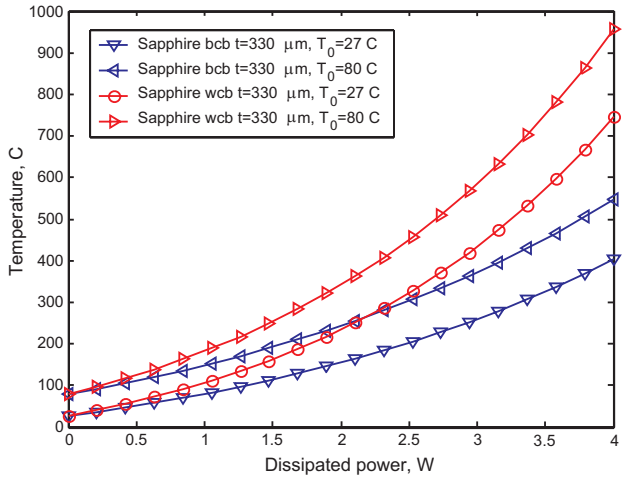

Fig. 4. Active region temperature for FET on sapphire BS mountings, bcb and wcb k models, as a function of dissipated power.

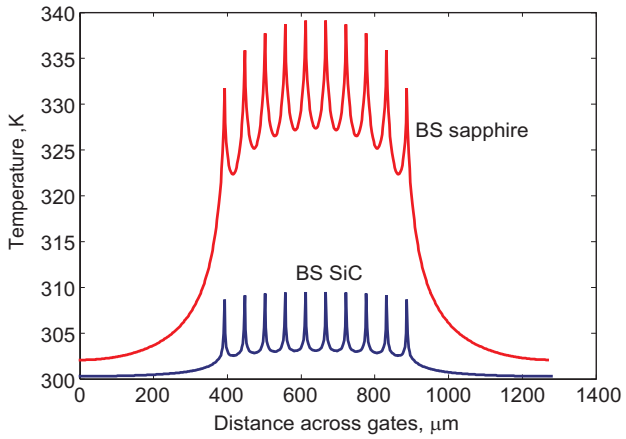

Fig. 5. Temperature distribution across gates for 6H-SiC and sapphire BS-mounted devices; the input power density is 1 W/mm and the heat sink temperature is 300 K.

very significant thermal coupling is observed, which could be greatly reduced by increasing the gate spacing, at least if the operating RF frequency is low enough not to conflict with electrical requirements.

IV. Acknowledgements

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